Memory Products
1987

Data Book

CONTENTS

Quality and Reliability

Introduction

NEC has adopted Total Quality Control (TQC) to ensure the highest quality and reliability of its state-of-the-art memory products. With TQC, excellence is built into the product at every phase of production.
As large-scale integration reaches higher density levels, simple quality inspections cannot ensure adequate levels of excellence. Only with TQC during every stage of production, can NEC maintain its total product superiority in the semiconductor industry.

Approaches to Total Quality Control

Total Quality Control enables early detection of possible failures in memory products, so that problems in design may be prevented. Immediate action can be taken before a problem occurs.
At NEC, all employees are involved with the concept and methodology of TQC. This quality insurance policy is an integral part of the entire organization.
NEC's research and development constantly strives to achieve higher standards. This on-going process reduces extensive failure analysis and corrective actions taken as preventative measures.
Our goals are to upgrade quality standards and to further improve the superior product that has become synonymous with the NEC name.

Implementations of Distributed Quality Control

Building excellence into a product requires the earliest possible detection of failure in each phase. Immediate action is taken to remove the cause of failure. Because fixed-station quality inspection often precludes the ability to take immediate action, it is necessary to perform quality control functions at each step - especially at the conceptual stage.
Here are the significant stages

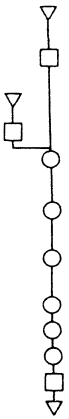
- ☐ Product development
- ☐ Wafer processing
- ☐ Assembly
- ☐ Electrical testing and screening
- ☐ Pre-inventory inspection
- ☐ Reliability assurance test

Product Development

The product development phase includes product **conception**, review of the device proposal, organization and physical element design, **engineering** evaluations, and transfer of the product to manufacturing.
In every step of the product development phase, quality and reliability requirements **must** be satisfied. Utilizing the TQC approach has shortened the product development cycles by two to three months. Building superiority into the product cannot be sacrificed - TQC is a way of life at NEC.

Wafer Fabrication Process Flow

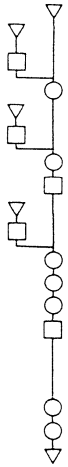
The in-process quality inspections (frequency) that occurs at the wafer fabrication stage are as follows:

Flow	Process	Typical Item	Frequency
	(Wafers)		
	Incoming inspection	Dimension	Every lot
	(Masks)	Resistivity	Every lot
	Incoming inspection	Appearance	Every lot
	Photo lithography	Alignment accuracy	Every lot
		Etching accuracy	Every lot
	Diffuse and oxidize	Oxide thickness	Every lot
		Sheet resistivity	Every lot
	Metalize	Aluminum thickness	Every run
		Electrical parameters	Every lot
	Passivation	CVD thickness	Every run
	Wafer sort	Electrical characteristics	100% chips
	Dicing		
	Chip visual	Appearance	100% chips
	To assembly		

Note: The wafer fabrication steps repeated in the actual flow, which complies with our manufacturing specification, are eliminated in this diagram.

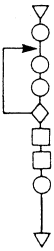
Assembly Process Flow of Plastic Memories

The in-process inspections (frequency) that are done during the assembly process are as follows:

Flow	Process	Typical Item	Frequency
	Chip (Lead frame, solder) Incoming inspection		
	Chip mounting	Appearance	Every lot
	(Fine Wire) Incoming inspection		
	Wire bonding	Bond strength	Every shift
	Pre-seal visual	Appearance	100% IC's
	(Molding compound) Incoming inspection		
	Molding	Appearance	100% IC's
	Thermal aging		
	Plating		
	Plating inspection	Appearance	Every lot
		Solderability	Every day
		Thickness	Every day
	Lead cut and bending		
	Marking	Marking permanency	Every run
	To test		

Electrical Testing and Screening

Electrical testing and infant mortality screening are performed at this stage. The flow chart below depicts the process.

Flow	Process	Freqency
	Assembly	
	1st electrical test	100%
	Burn-in	100%
	2nd electrical test	100%
	PDA	
	Pre-inventory inspection	Every lot
	Reliability assurance test	Every lot or every month
	Warehouse/finished goods	
	Customer	

In the first electrical test, DC parameters are tested, in accordance with electrical specifications, on 100% of each lot. This prescreen performance is completed prior to the infant mortality testing. 100%burn-in, as an integral part of the standard production process, is the most significant preventative measure NEC has implemented.
In the second electrical test, AC functional as well as DC parameter tests are performed. If the percentage of defective units exceeds a set limit, the lot is subject to an additional burn-in. During this second burn-in, the defective units undergo a failure analysis. The results of this analysis are then fed back into the process for corrective action.

Pre-Inventory Inspection

Prior to warehouse storage, lots are subject to an incoming inspection according to the following sampling plan:

- ☐ Electrical Test - DC parameters LTPD 3%
  Function test LTPD 3%
- ☐ Appearance - LTPD 3%

Reliability Assurance Test

The reliability assurance tests performed by NEC consist of high temperature operating life (HTOL), high temperature storage life (HTSL), high humidity storage life (HHSL), and high humidity operating life (HHOL). In addition, various environmental and mechanical tests are also performed. Table 1 shows test conditions of various life tests, environmental tests, and mechanical tests performed on samples taken from similar process families on a monthly basis.

Test Item	Symbol	MIL-STD 883 B Method, Condition	Remarks
High temperature operating life	HTOL	1005D ($T_A = 125°C$) V_{DD} as specified	Note 1
High temperature storage life	HTSL	1008 ($T_A = 150°C$)	Note 1
High humidity operating life	HHOL	$T_A = 85°C$ at 85%RH V_{DD} as specified	Note 1
High humidity storage life	HHSL	$T_A = 85°C$ at 85% RH	Note 1
Pressure cooker test	PCT	125°C (2.5 atm)	Note 1
Lead Fatigue	C3	2004B2	Broken lead is considered to be a reject
Solderability	C4	$T_A = 230°C$, 5 sec Use resin base flux	Less than 95 % coverage is considered to be a reject
Soldering heat	C6	260°C, 10 sec w/out flux - Note 2	Note 1
Temperature cycle	C6	1010C; 10 Cycles; -65°C to 150°C	Note 1
Thermal shock	C6	1011A; 15 cycles 0°C to 100°C	Note 1

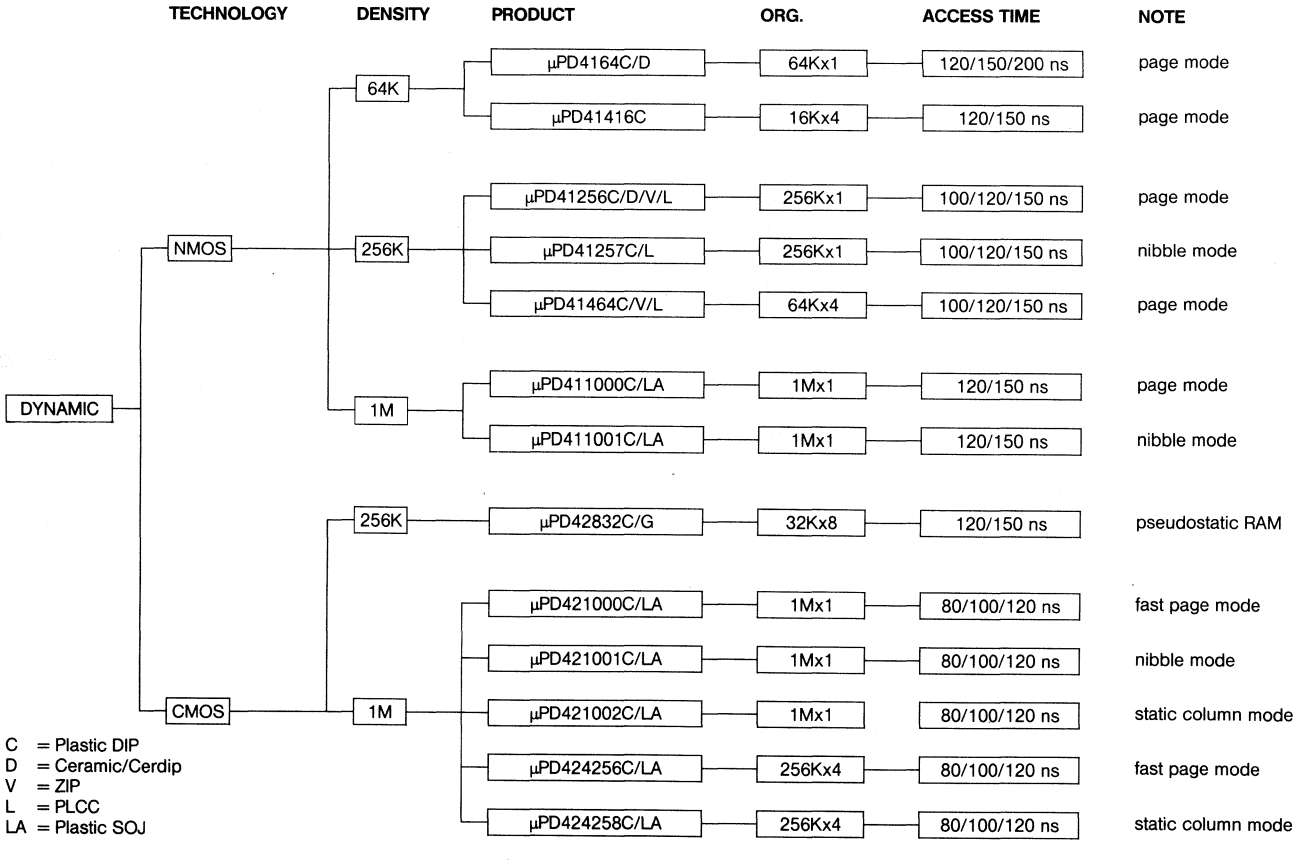
Notes: 1. Electrical test per data sheet is performed. Devices that exceed these data sheet limits are considered to be rejects.
2. MIL-STD-750A Method 2031.

Summary

Building quality and reliability into products is the most efficient way to ensure product excellence. NEC's TQC process steps form a consolidated quality control system and guarantees a superior product.
The introduction of 100% burn-in and the performance of monthly reliability assurance tests, have established a singularly high standard of excellence for NEC's large-scale integrated circuits.
With total commitment to Total Quality Control, NEC is committed to producing superior products. Through continuous research and development, extensive failure analysis and process improvements, NEC continues to set and maintain the highest standards of quality and reliability.

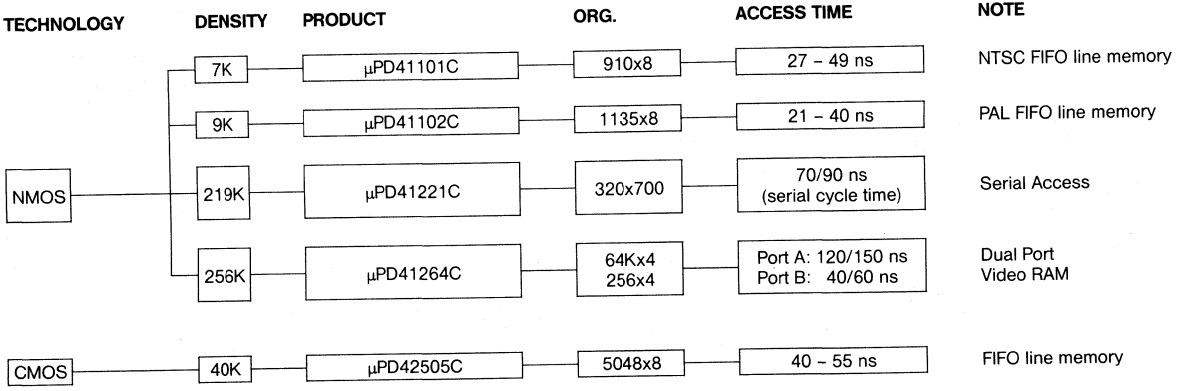
Memory Products

Dynamic RAM



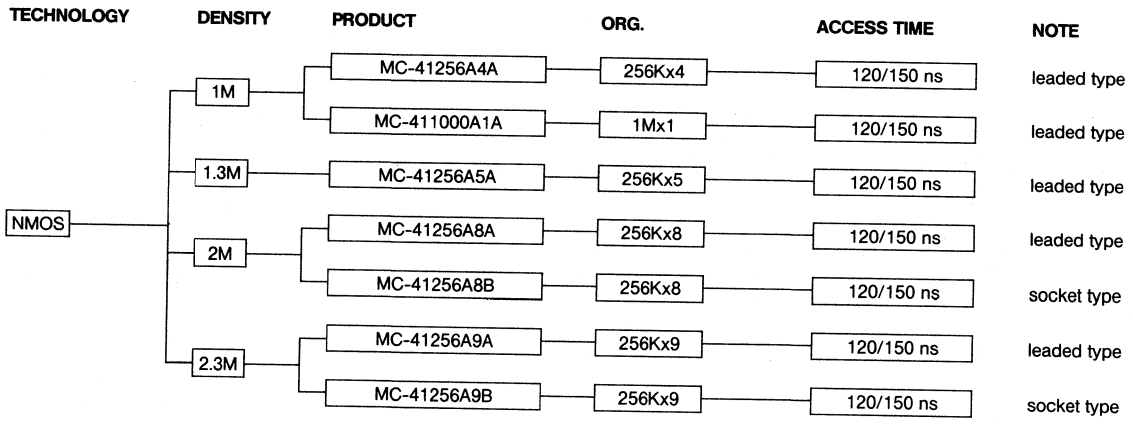
NEC

Application Specific Memories



C = Plastic DIP

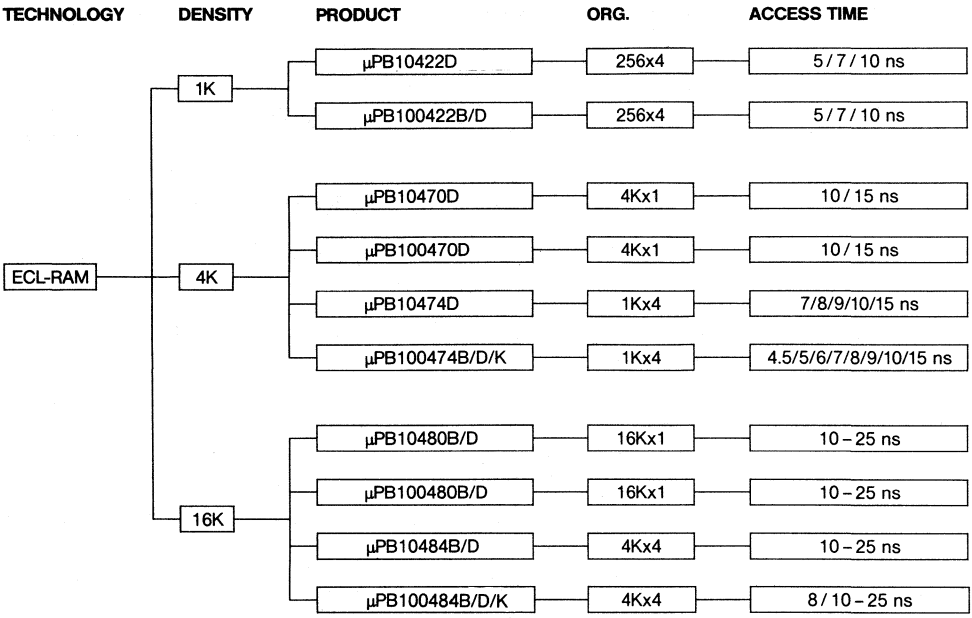
DYNAMIC SINGLE-IN-LINE MODULES



A = glass epoxy substrate, leaded type module
B = glass epoxy substrate, socket type module

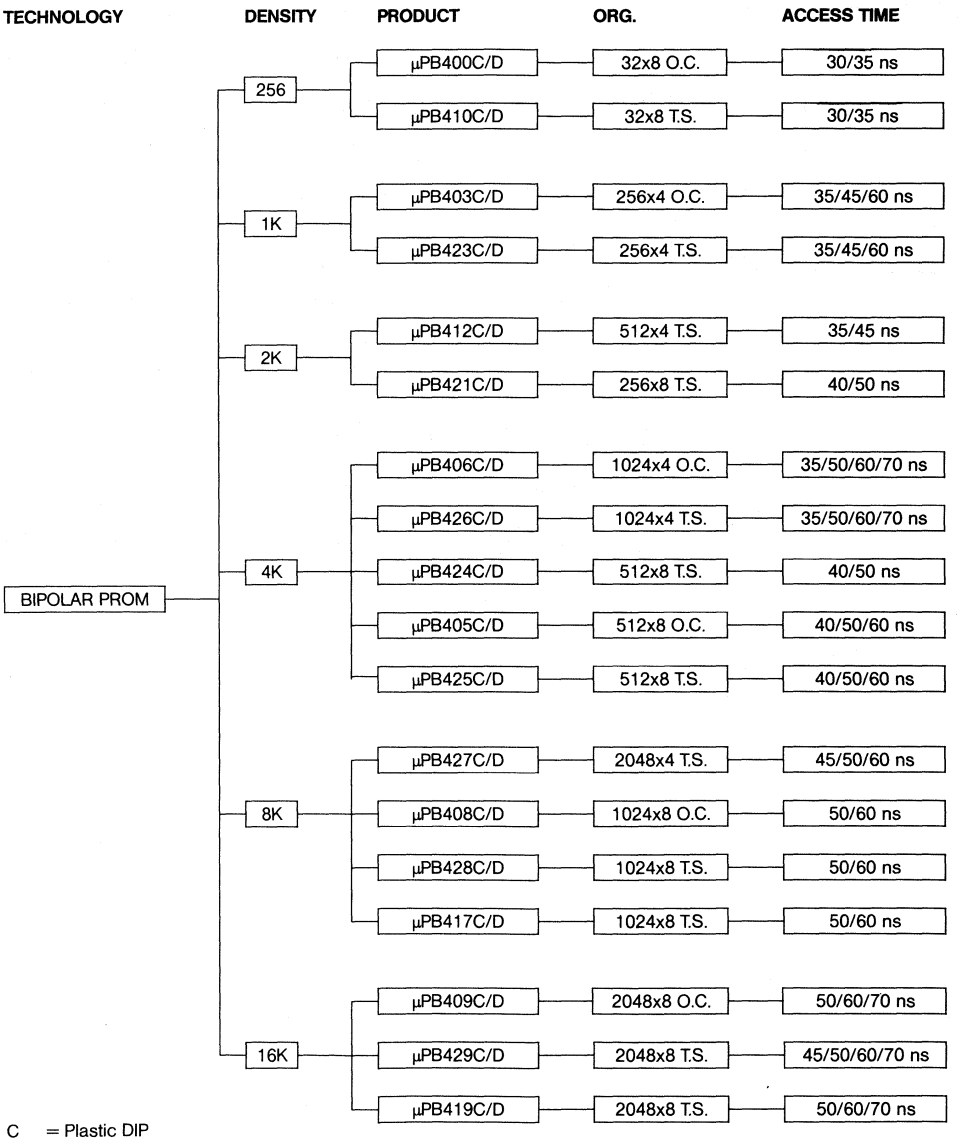
NEC

ECL RAM



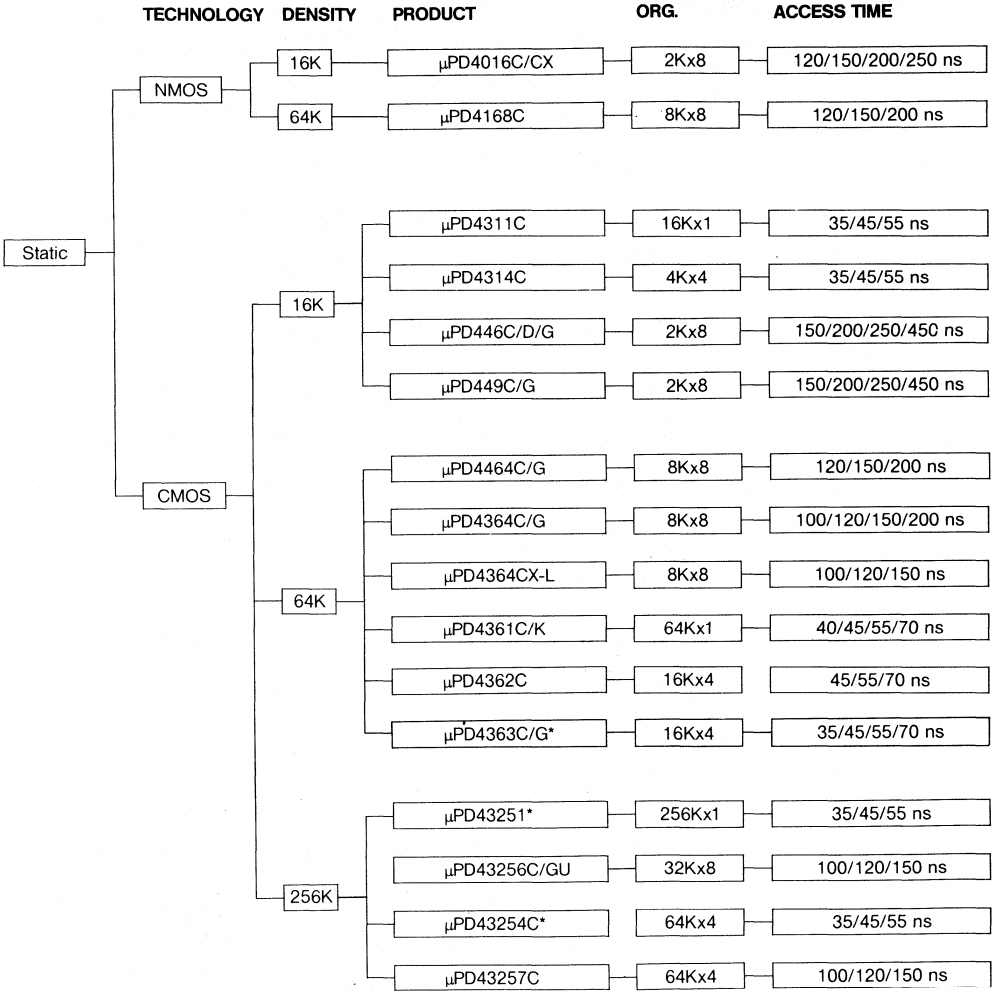
D = Hermetic DIP
B = Ceramic flat package
K = LCC

BIPOLAR PROM



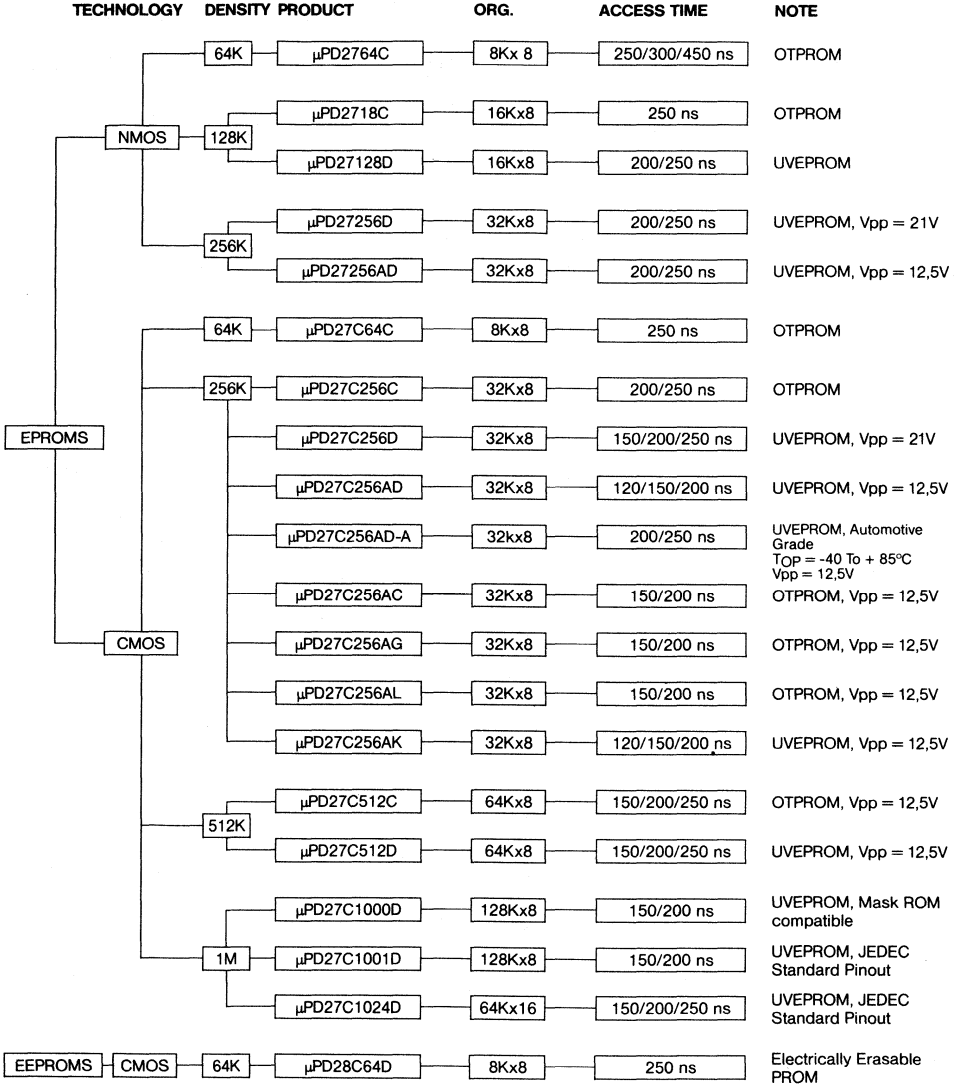
C = Plastic DIP
D = Hermetic DIP
O.C. = Open-collector-output
T.S. = Three-state-output

STATIC RAM

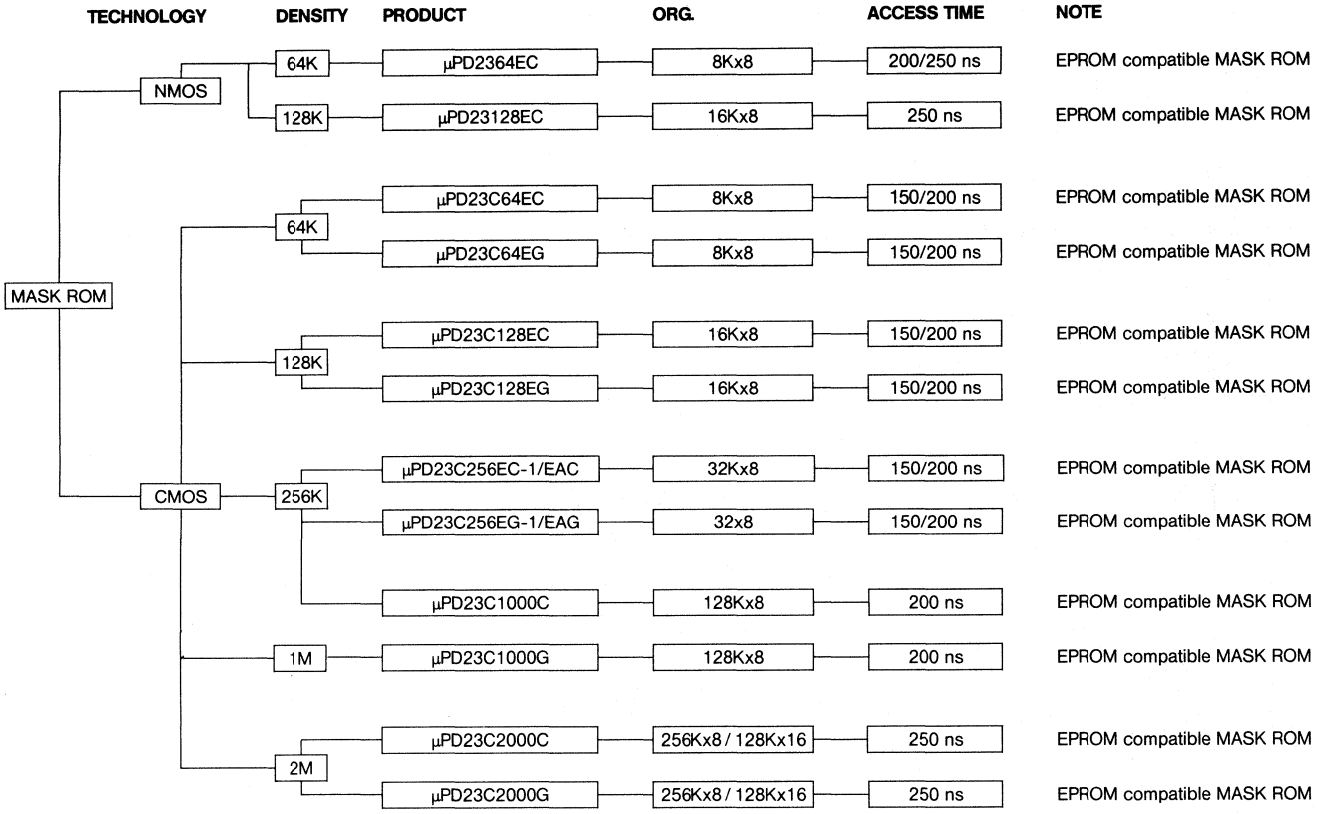


* Under development

ERASABLE PROGRAMMABLE ROM



MASK ROM


TECHNOLOGY
DENSITY
PRODUCT
ORG.
ACCESS TIME
NOTE
MASK ROM
NMOS
CMOS
64K
128K
256K
1M
2M
µPD2364EC
µPD23128EC
µPD23C64EC
µPD23C64EG
µPD23C128EC
µPD23C128EG
µPD23C256EC-1/EAC
µPD23C256EG-1/EAG
µPD23C1000C
µPD23C1000G
µPD23C2000C
µPD23C2000G
8Kx8
16Kx8
32Kx8
32x8
128Kx8
256Kx8 / 128Kx16
200/250 ns
250 ns
150/200 ns
200 ns
EPROM compatible MASK ROM

NEC

DYNAMIC RAM

Density (Bit)	Part No.	Process	Organi-zation	Pin Number/ Package	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
64K	μPD4164-12	NMOS	64Kx1	16 – DIP	120	+5	303
	μPD4164-3				150		275
	μPD4164-2				200		250
	μPD41416-12	NMOS	16Kx4	18 – DIP	120	+5	303
	μPD41416-15				150		275
256K	μPD41256-10	NMOS	256Kx1 (page mode)	16 – DIP/ZIP 18 – PLCC	100	+5	457
	μPD41256-12				120		457
	μPD41256-15				150		385
	μPD41257-10	NMOS	256Kx1 (nibble mode	16 – DIP	100	+5	440
	μPD41257-12			18 – PLCC	120		413
	μPD41257-15				150		385
	μPD41464-10	NMOS	64Kx4	18 – DIP/ PLCC 20 – ZIP	100	+5	440
	μPD41464-12				120		413
	μPD41464-15				150		385
	μPD42832-12	CMOS	32Kx8	28 – DIP/SO	120	+5	275
	μPD42832-15				150		220
1 M	μPD411000-12	NMOS	1Mx1 (page mode)	18 – DIP	120	+5	550
	μPD411000-15			26 – SOJ	150		495
	μPD411001-12	NMOS	1Mx1 (nibble mode)	18 – DIP	120	+5	550
	μPD411001-15			26 – SOJ	150		495

Density (Bit)	Part No.	Process	Organi-zation	Pin Number/ Package	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
1M	μPD421000-8	CMOS	1Mx1 (fast page mode)	18 – DIP 26 – SOJ	80	+5	385
	μPD421000-10				100		330
	μPD421000-12				120		275
	μPD421001-8	CMOS	1Mx1 (nibble mode)	18 – DIP 26 – SOJ	80	+5	385
	μPD421001-10				100		330
	μPD421001-12				120		275
	μPD421002-8	CMOS	1Mx1 (static column mode)	18 – DIP 26 – SOJ	80	+5	385
	μPD421002-10				100		330
	μPD421002-12				120		275
	μPD424256-8**	CMOS	256Kx4 (fast page mode)	20 – DIP 26 – SOJ	80	+5	385
	μPD424256-10**				100		330
	μPD424256-12**				120		275
	μPD424258-8**	CMOS	256Kx4 (static column mode)	20 – DIP 26 – SOJ	80	+5	385
	μPD424258-10**				100		330
	μPD424258-12**				120		275

Note: DIP = Dual-In-Line Package (plastic/hermetic)
ZIP = Zig-Zag package (plastic)
PLCC = Plastic leaded Chip Carrier
SO = Small Outline Package (Mini-Flat) (plastic)
SOJ = Small Outline J-Lead Package (plastic)
** = available beginning of 1987

APPLICATION SPECIFIC MEMORIES

Density (Bit)	Part No.	Process	Organi-zation	Pin Number/ Package	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
7K	μPD41101 FIFO Biport Line Memory	NMOS	910x8 (NTSC)	24 – DIP	27 – 49	+5	495
9K	μPD41102 FIFO Biport Line Memory	NMOS	1135x8 (PAL)	24 – DIP	21 – 40	+5	495
40K	μPD42505 Line/FIFO Memory	CMOS	5048x8	24 – DIP	40 – 55	+5	660
219K	μPD41221 Serial Access Memory	NMOS	320x700	24 – DIP	70 / 90	+5	303/248
256K	μPD41264 Dual Port Memory	NMOS	Port A: 64Kx4	24 – DIP 26 – SOJ**	Port A: 120 Port B: 40	+5	835
			Port B: 256x4		Port A: 150 Port B: 60		715

Note: DIP = Dual-In-Line Package
SOJ = Small Outline J-Lead package
** = available beginning of 1987

DYNAMIC SINGLE-IN-LINE-MODULES

Density (Bit)	Part No. **	Process	Organi-zation	Pin Number	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
1M	MC-41256A4A-12/15	NMOS	256Kx4	22	120/150	+5	1826/1540
	MC-411000A1A-12/15	NMOS	1Mx1	22	120/150	+5	539/468
1.3M	MC-41256A5A-12/15	NMOS	256Kx5	24	120/150	+5	2283/1925
2M	MC-41256A8A-12/15	NMOS	256Kx8	30	120/150	+5	3652/3080
	MC-41256A8B-12/15						
2.3M	MC-41256A9A-12/15	NMOS	256Kx9	30	120/150	+5	4109/3465
	MC-41256A9B-12/15						

Note: ** A = glass epoxy substrate, leaded type module
B = glass epoxy substrate, socket type module

ECL RAM

Density (Bit)	Part No.	Process	Organi-zation	Pin Number/ Package	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
1K	μPB10422-5	ECL 10K	256x4	24 – D	5	–5.2	1.3
	μPB10422-7				7		1.2
	μPB10422-10				10		1.2
	μPB100422-5	ECL 100K	256x4	24 – D/B	5	–4.5	1.1
	μPB100422-7				7		1
	μPB100422-10				10		1
4K	μPB10470-10	ECL 10K	4Kx1	18 – D	10	–5.2	1.2
	μPB10470-15				15		1.2
	μPB100470-10	ECL 100K	4Kx1	18 – D	10	–4.5	1
	μPB100470-15				15		1
	μPB10474-7	ECL 10K	1Kx4	24 – D	7	–5.2	1.3
	μPB10474-8				8		1.2
	μPB10474-9				9		1.2
	μPB10474-10				10		1.2
	μPB10474-15				15		1.2
	μPB100474-45	ECL 100K	1Kx4	24 – K	4.5	–4.5	2
	μPB100474-50				5		2
	μPB100474-60				6		2
	μPB100474-7			24 – D/B	7		1.1
	μPB100474-8				8		1
	μPB100474-9				9		1
	μPB100474-10				10		1
	μPB100474-15				15		1
16K	μPB10480	ECL 10K	16Kx1	20 – D/B	10 – 25	–5.2	1.2
	μPB100480	ECL 100K	16Kx1	20 – D/B	10 – 25	–4.5	1.2
	μPB10484	ECL 10K	4Kx4	28 – D/B	10 – 25	–5.2	1.2
	μPB100484	ECL 100K	4Kx4	28 – K	8	–4.5	2
				28 – D/B	10 – 25		1.2

Note: D = Ceramic/Cerdip DIP
B = Flat Pack
K = LCC

BIPOLAR PROM

Density (Bit)	Part No.	Organization	Package Pins	(DIP) Width	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
256	μPB400-0	32 x 8 O.C.	16	300 Mil.	35	+5	550
	μPB400-1				30		
	μPB410-0	32 x 8 T.S.	16	300 Mil.	35	+5	550
	μPB410-1				30		
1K	μPB403-0	256 x 4 O.C.	16	300 Mil.	60	+5	715
	μPB403-1				45		
	μPB403-2				35		
	μPB423-0	256 x 4 T.S.	16	300 Mil.	60	+5	715
	μPB423-1				45		
	μPB423-2				35		
2K	μPB412-0	512 x 4 T.S.	16	300 Mil.	45	+5	715
	μPB412-1				35		
	μPB421-0	256 x 8 T.S.	20	300 Mil.	50	+5	770
	μPB421-1				40		
4K	μPB406-0	1024 x 4 O.C.	18	300 Mil.	70	+5	825
	μPB406-1				60		
	μPB406-2				50		
	μPB406-3				35		
	μPB426-0	1024 x 4 T.S.	18	300 Mil.	70	+5	825
	μPB426-1				60		
	μPB426-2				50		
	μPB426-3				35		
	μPB424-0	512 x 8 T.S.	20	300 Mil.	50	+5	825
	μPB424-1				40		
	μPB405-0	512 x 8 O.C.	24	600 Mil.	60	+5	880
	μPB405-1				50		
	μPB405-2				40		
	μPB425-0	512 x 8 T.S.	24	600 Mil.	60	+5	880
	μPB425-1				50		
	μPB425-2				40		

Density (Bit)	Part No.	Organization	Package Pins	(DIP) Width	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)
8K	μPB427-0	2048 x 4 T.S.	18	300 Mil.	60	+5	770
	μPB427-1				50		
	μPB427-2				45		
	μPB408-0	1024 x 8 O.C.	24	600 Mil.	60	+5	880
	μPB408-1				50		
	μPB428-0	1024 x 8 T.S.	24	600 Mil.	60	+5	880
	μPB428-1				50		
	μPB417-0	1024 x 8 T.S.	24	600 Mil.	60	+5	880
	μPB417-1				50		
16K	μPB409-0	2048 x 8 O.C.	24	600 Mil.	70	+5	880
	μPB409-1				60		
	μPB409-2				50		
	μPB409-3				45		
	μPB429-0	2048 x 8 T.S.	24	600 Mil.	70	+5	880
	μPB429-1				60		
	μPB429-2				50		
	μPB429-3				45		
	μPB419-0	2048 x 8 T.S.	24	600 Mil.	70	+5	880
	μPB419-1				60		
	μPB419-2				50		

Note: O.C. = Open-Collector Output
T.S. = Three-State-Output
available in plastic and hermetic packages

FPLA (FIELD PROGRAMMABLE LOGIC ARRAY)

Density (Bit)	Part No.	Organization	Package Pins	(DIP) Width	T (PIO)	Power Supply (V)	Active Power Dissipation (mW max.)
9K	μPB450B	AND-Array 80 x 72	48	600 Mil.	70ns Typ	+5	1313
	μPB450B-1	OR-Array 72 x 48	48	600 Mil.	50ns Typ	+5	1313

Note: t (PIO) = propagation delay from inputs to outputs
available in plastic and ceramic packages

STATIC RAM

Density (Bit)	Part No.	Process	Organi-zation	Pin Number/ Package	Access Time (ns max.)	Power Supply (V)	Active Power Dissipation (mW max.)	Note
16K	μPD4016-5	NMOS	2Kx8	24/C	120	+5	330	$\overline{WE}$, $\overline{CS}$, $\overline{OE}$ inputs Plastic DIP, 600 mil
	μPD4016-3				150		330	
	μPD4016-2				200		330	
	μPD4016-1				250		330	
	μPB4016-0				450		330	
	μPD4016-12	NMOS	2Kx8	24/CX	120	+5	330	$\overline{WE}$, $\overline{CS}$, $\overline{OE}$ inputs Plastic shrink DIP, 300 mil
	μPD4016-15				150		330	
	μPD4311-35	CMOS	16Kx1	20/C	35	+5	440	$\overline{CS}$, $\overline{WE}$ inputs Replacement of 2167 Plastic DIP, 300 mil
	μPD4311-45				45		440	
	μPD4311-55				55		440	
	μPD4314-35	CMOS	4Kx4	20/C	35	+5	440	$\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil
	μPD4314-45				45		440	
	μPD4314-55				55		440	
	μPD446-3/3L	CMOS	2Kx8	24/C/D	150	+5	209	CS, OE, WE inputs Plastic DIP Cerdip, 600 mil
	μPD446-2/2L				200		165	
	μPD446-1/1L				250		143	
	μPD446-0/0L				450		154	
	μPD446-15/15L	CMOS	2Kx8	24/G	150	+5	209	$\overline{CS}$, $\overline{OE}$, $\overline{WE}$ inputs Plastic SOP
	μPD446-20/20L				200		165	
	μPD446-25/25L				250		143	
	μPD449-3/3L	CMOS	2Kx8	24/C	150	+5	209	$\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$ inputs Plastic DIP
	μPD449-2/2L				200		165	
	μPD449-1/1L				250		143	
	μPD449-0/0L				450		99	
	μPD449-15/15L	CMOS	2Kx8	24/G	150	+5	209	$\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$ inputs Plastic SOP
	μPD449-20/20L				200		165	
	μPD449-25/25L				250		143	
64K	μPD4361-25*	CMOS	64Kx1	22/C/K	25	+5	660	$\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil Ceramic LCC
	μPD4361-40				40		660	
	μPD4361-45				45		660	
	μPD4361-55				55		660	
	μPD4361-70				70		660	
	μPD4362-25*	CMOS	16Kx4	22/C	25	+5	t.b.a.	
	μPD4362-35				35		t.b.a.	
	μPD4362-45				45		495	$\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil
	μPD4362-55				55		495	
	μPD4362-70				70		495	
	μPD4363-25*	CMOS	16Kx4	24/C/G	25	+5	t.b.a.	$\overline{OE}$, $\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil
	μPD4363-35*				35		t.b.a.	
	μPD4363-45*				45		495	
	μPD4363-55*				55		495	
	μPD4363-70*				70		495	

* Under Development

Density	Part No.	Process	Organi-zation	Pin/ Package	Acess Time (ns max.)	Power Supply	Active Power Dissipation	Notes
64K	μPD4364-10L/10LL	CMOS	8Kx8	28/C/G	100	+5	249	$\overline{CE1}$, CE2, $\overline{OE}$, $\overline{WE}$ inputs Plastic Dip, 600 mil Plastic SOP
	μPD4364-12L/12LL				120		220	
	μPD4364-15L/15LL				150		193	
	μPD4364-20L/20LL				200		165	
	μPD4364-10L	CMOS	8Kx8	28/CX	100	+5	248	$\overline{CE1}$, CE2, $\overline{OE}$, $\overline{WE}$ inputs Plastic shrink DIP, 300 mil
	μPD4364-12L				120		220	
	μPD4364-15L				150		193	
	μPD4464-12L	CMOS	8Kx8	28/C/G	120	+5	220	$\overline{CE1}$, CE2, $\overline{OE}$, $\overline{WE}$ inputs Plastic DIP, 600 mil Plastic SOP
	μPD4464-15L				150		220	
	μPD4464-20L				200		193	
	μPD4168-12	NMOS	8Kx8	28/C	120	+5	358	CS, $\overline{CE}$, $\overline{WE}$ Inputs Pseudo static Plastic DIP, 600 mil
	μPD4168-15				150		330	
	μPD4168-20				250		303	
256K	μPD43256-10L	CMOS	32Kx8	28/C/GU	100	+5	385	$\overline{CS}$, $\overline{WE}$, $\overline{OE}$ Inputs Plastic DIP, 600 mil Plastic SOP
	μPD43256-12L				120		385	
	μPD43256-15L				150		385	
	μPD43251-35 *	CMOS	256Kx1	24/C	35	+5	495	$\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil
	μPD43251-45 *				45		495	
	μPD43251-55 *				55		495	
	μPD43254-35 *	CMOS	64Kx4	24/C	35	+5	660	$\overline{CS}$, $\overline{WE}$ inputs Plastic DIP, 300 mil
	μPD43254-45 *				45		660	
	μPD43254-55 *				55		660	
	μPD43257-10/10L *	CMOS	32Kx8	28/C	100	+5	385	$\overline{CE1}$, CE2, $\overline{WE}$ Inputs Plastic DIP, 600 mil
	μPD43257-12/12L *				120		385	
	μPD43257-15/15L *				150		385	

* Under Development

EPROM

Density (Bit)	Part No.	Process	Organi-zation	Pin. No./ Package	Access Time (ns max.)	Power Supply VCC (V)	Programming Voltage VPP (V)	Power Dissipation (mW)	Note
64K	μPD2764C	NMOS	8Kx8	28/PLASTIC DIP	250	+5	21V	420	OTPROM
	μPD2764C-3			28/PLASTIC DIP	300				OTPROM
	μPD2764C-4			28/PLASTIC DIP	450				OTPROM
	μPD27C64C-25	CMOS	8Kx8	28/PLASTIC DIP	250	+5	21V	165	OTPROM
128K	μPD27128D-2	NMOS	16Kx8	28/CERDIP	200	+5	21V	525	UVEPROM
	μPD27128D			28/CERDIP	250				UVEPROM
	μPD27128C			28/PLASTIC DIP	250				OTPROM
256K	μPD27256D-2	NMOS	32Kx8	28/CERDIP	200	+5	21V	525	UVEPROM
	μPD27256D			28/CERDIP	250	+5	21V	525	UVEPROM
	μPD27256AD-2			28/CERDIP	200	+5	12.5V	525	UVEPROM
	μPD27256AD			28/CERDIP	250	+5	12.5V	525	UVEPROM
	μPD27C256D-15	CMOS	32Kx8	28/CERDIP	150	+5	21V	165	UVEPROM
	μPD27C256D-20			28/CERDIP	200				UVEPROM
	μPD27C256D-25			28/CERDIP	250				UVEPROM
	μPD27C256C-20			28/PLASTIC DIP	200				OTPROM
	μPD27C256C-25			28/PLASTIC DIP	250				OTPROM
	μPD27C256AD-12	CMOS	32Kx8	28/CERDIP	120	+5	12.5V	165	UVEPROM
	μPD27C256AD-15			28/CERDIP	150				UVEPROM
	μPD27C256AD-20			28/CERDIP	200				UVEPROM
	μPD27C256AD-A-20			28/CERDIP	200				UVEPROM, Automotive Grade
	μPD27C256AD-A-25			28/CERDIP	250				TOP = −40 to +85°C
	μPD27C256AC-15			28/PLASTIC DIP	150				TOP = −40 to +85°C
	μPD27C256AC-20			28/PLASTIC DIP	200				OTPROM
	μPD27C256AG-15			28/PLASTIC	150				OTPROM
	μPD27C256AG-20			28/MINIFLAT	200				OTPROM
	μPD27C256AL-15 *			32/PLASTIC LCC	150				OTPROM
	μPD27C256AL-20 *			32/PLASTIC LCC	200				OTPROM
	μPD27C256AK-12			32/CERDIP LCC	120				UVEPROM
	μPD27C256AK-15			32/CERDIP LCC	150				UVEPROM
	μPD27C256AK-20			32/CERDIP LCC	200				UVEPROM
512K	μPD27C512C-15	CMOS	64Kx8		150	+5	12.5V	165	OTPROM
	μPD27C512C-20			28/PLASTIC DIP	200				OTPROM
	μPD27C512C-25			28/PLASTIC DIP	250				OTPROM
	μPD27C512D-15			28/CERDIP	150				UVEPROM
	μPD27C512D-20			28/CERDIP	200				UVEPROM
	μPD27C512D-25			28/CERDIP	250				UVEPROM

* Under Development

Density (Bit)	Part No.	Process	Organi-zation	Pin. No./ Package	Access Time (ns max.)	Power Supply VCC (V)	Programming Voltage VPP (V)	Power Dissipation (mW)	Note
1M	μPD27C1000D-15	CMOS	128Kx8	40/CERDIP	150	+5	12.5V	275	UVEPROM, MASK ROM COMPATIBLE
	μPD27C1000D-20			40/CERDIP	200				UVEPROM, MASK ROM COMPATIBLE
	μPD27C1001D-15			40/CERDIP	150				UVEPROM, JEDEC STAND. PIN OUT
	μPD27C1001D-20			40/CERDIP	200	+5	12.5V	275	UVEPROM, JEDEC STAND. PIN OUT
	μPD27C1024D-15		64Kx16	40/CERDIP	150				UVEPROM, JEDEC STAND. PIN OUT
	μPD27C1024D-20			40/CERDIP	200				UVEPROM, JEDEC STAND. PIN OUT
	μPD27C1024D-25			40/CERDIP	250				UVEPROM, JEDEC STAND. PIN OUT

EEPROM

Density (Bit)	Part No.	Process	Organi-zation	Pin No. Package	Access Time (ns max.)	Power Supply VCC (V)	Programming Voltage VPP (V)	Power Dissipation (mW)	Note
64K	μPD28C64D-25	CMOS	8Kx8	28/CERDIP	250	+5	–	275	ELECTRICALLY ERASABLE PROM

MASKROM

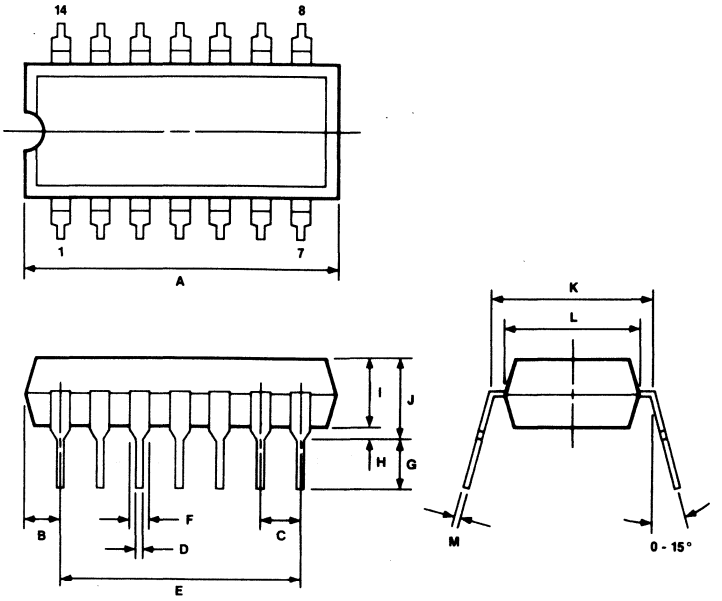
Density (Bit)	Part No.	Process	Organi-zation	Pin No./ Package	Access Time (ns max.)	Power Supply VCC (V)	Operation	Power Dissipation (mW)	Note
64K	μPD2364EC	NMOS	8Kx8	28/PLASTIC DIP	250	+5	STATIC	420	EPROM COMPATIBLE MASKROM
	μPD2364EC-1	NMOS		28/PLASTIC DIP	200			420	EPROM COMPATIBLE MASKROM
	μPD23C64EC	CMOS		28/PLASTIC DIP	200			138	EPROM COMPATIBLE MASKROM
	μPD23C64EC-1	CMOS		28/PLASTIC DIP	150			165	EPROM COMPATIBLE MASKROM
	μPD23C64EG	CMOS		28/MINIFLAT	200			138	EPROM COMPATIBLE MASKROM
	μPD23C64EG-1	CMOS		28/MINIFLAT	150			165	EPROM COMPATIBLE MASKROM
128K	μPD23128EC	NMOS	16Kx8	28/PLASTIC DIP	250	+5	STATIC	630	EPROM COMPATIBLE MASKROM
	μPD23C128EC	CMOS		28/PLASTIC DIP	200			175	EPROM COMPATIBLE MASKROM
	μPD23C128EC-1	CMOS		28/PLASTIC DIP	150			210	EPROM COMPATIBLE MASKROM
	μPD23C128EG	CMOS		28/PLASTIC	200			175	EPROM COMPATIBLE MASKROM
	μPD23C128EG-1	CMOS		28/MINIFLAT	150			210	EPROM COMPATIBLE MASKROM
256K	μPD23C256EC-1	CMOS	32Kx8	28/PLASTIC DIP	150	+5	STATIC	210	EPROM COMPATIBLE MASKROM
	μPD23C256EG-1			28/MINIFLAT	150			210	EPROM COMPATIBLE MASKROM
	μPD23C256EAC			28/PLASTIC DIP	200			175	EPROM COMPATIBLE MASKROM
	μPD23C256EAG			28/MINIFLAT	200			175	EPROM COMPATIBLE MASKROM
1M	μPD23C1000C/G	CMOS	128Kx8	28/PLASTIC DIP/ MINIFLAT	200	+5	STATIC	280	EPROM COMPATIBLE MASKROM
2M	μPD23C2000C/G	CMOS	256Kx8 128Kx16	40/PLASTIC DIP/ MINIFLAT	250	+5	STATIC	280	EPROM COMPATIBLE MASKROM

Package Information

14 PIN Plastic DIP (400 mil)

μPD41221C

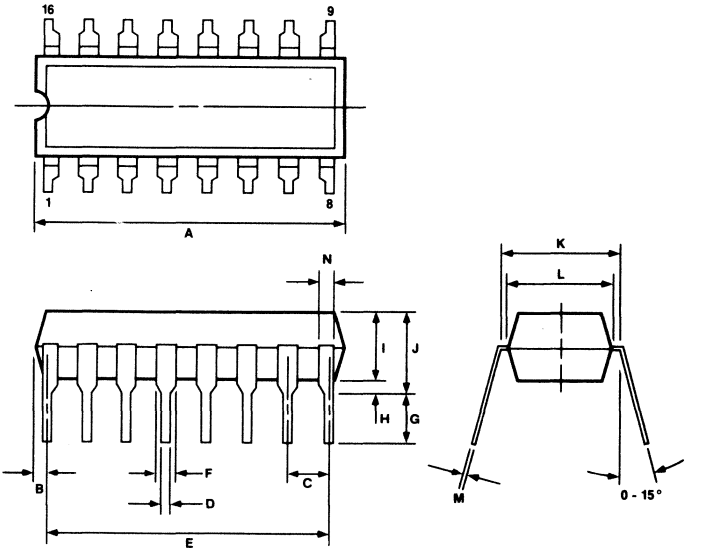
Item	Millimeters
A	20.32 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	15.24
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	10.16 [TP]
L	8.6
M	$.25^{+.10}_{-.05}$



16 PIN Plastic DIP (300 mil)

μPD4164C
μPB400C
μPB410C
μPB403C
μPB423C
μPB412C

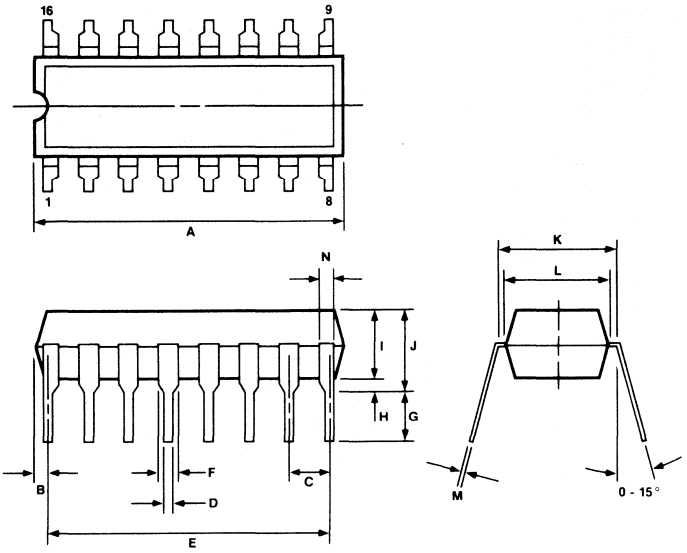
Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.5 ± .03
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



16 PIN Plastic DIP (300 mil, Semiwide Body)

μPD41256C
μPD41257C

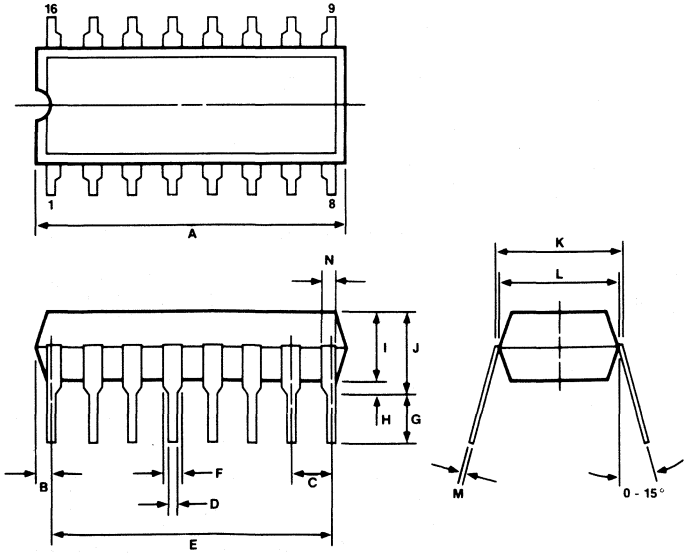
Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.7
M	$.25^{+.10}_{-.05}$
N	1.0 min



16 PIN Plastic DIP (300 mil, Wide Body)

μPD41256C

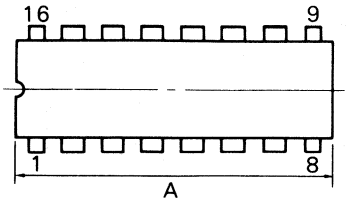
Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.4
M	$.25^{+.10}_{-.05}$
N	1.0 min

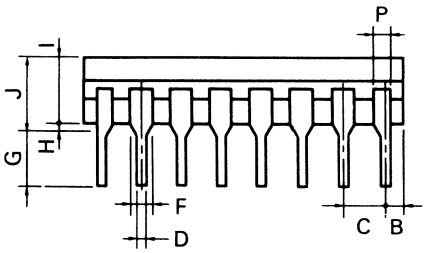


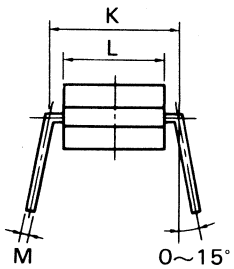
16-PIN CERDIP (300 mil)

μPB400D
μPB410D
μPB403D
μPB423D
μPB412D

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 (T. P.)
D	0.46 ± 0.05
F	1.42 min
G	3.5 ± 0.3
H	0.51 min
I	3.70
J	5.08 max
K	7.62 (T. P.)
L	6.75
M	0.25 ± 0.05
N	0.25
P	0.89 min



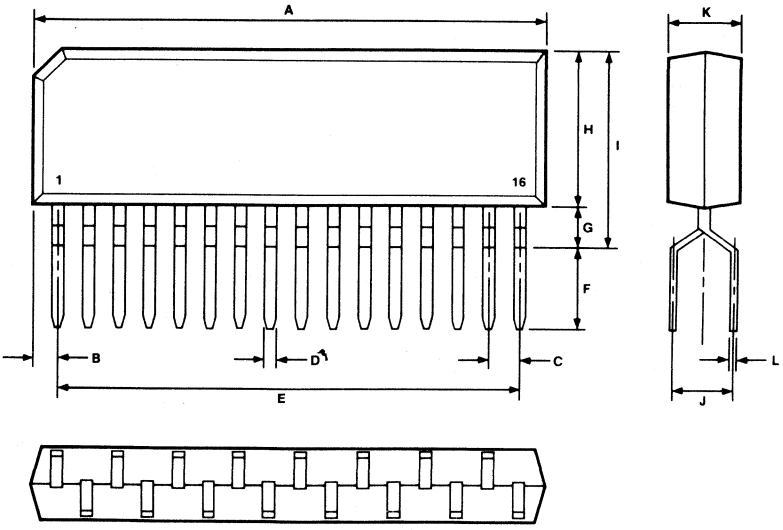




16 PIN Plastic ZIP

μPD41256V

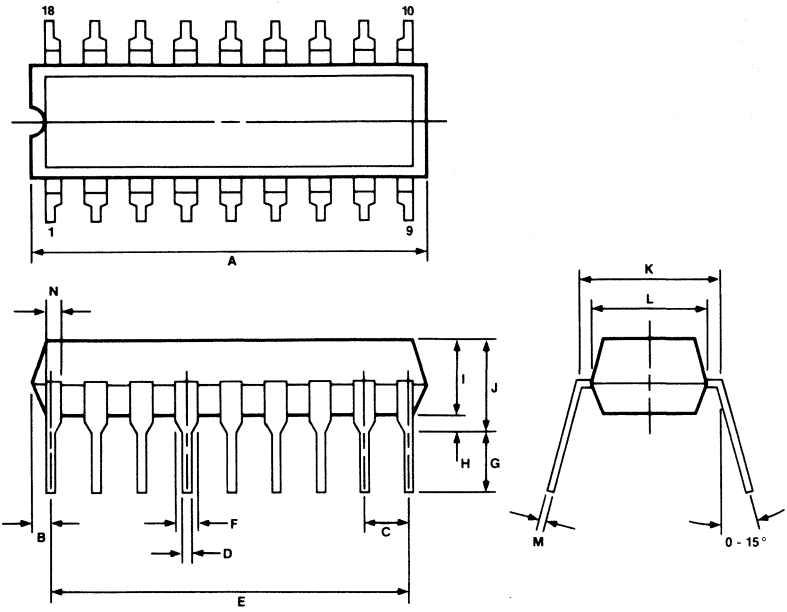
Item	Millimeters
A	21.59 max
B	1.27 max
C	1.27 [TP]
D	.50 ± .10
E	19.05
F	3.5 ± .3
G	.9 min
H	6.6
I	8.3 max
J	2.54 [TP]
K	2.8 ± .2
L	.25 $^{+.10}_{-.05}$



18 PIN Plastic DIP (300 mil)

μPD41416C
μPB426C
μPB427C

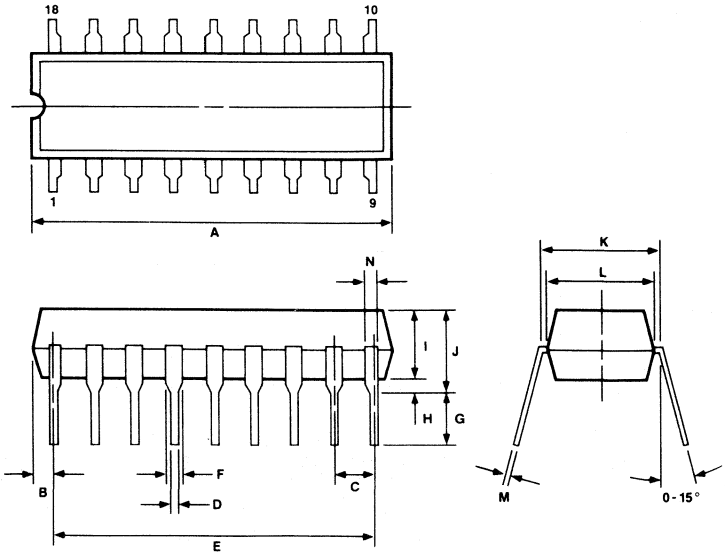
Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.5 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



18 PIN Plastic DIP (300 mil, Semiwide Body)

μPD41464C

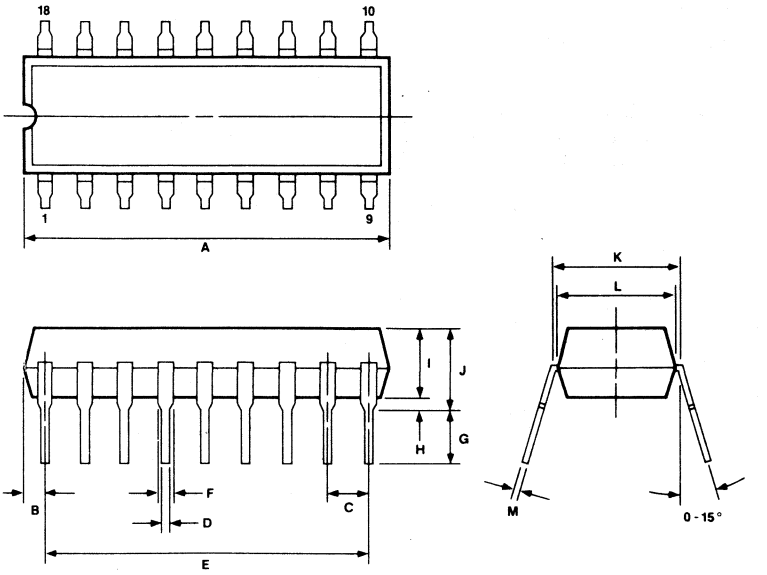
Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.7
M	$.25^{+.10}_{-.05}$
N	1.0 min



18 PIN Plastic DIP (300 mil, Wide Body)

μPD411000C
μPD411001C
μPD421000C
μPD421001C
μPD421002C

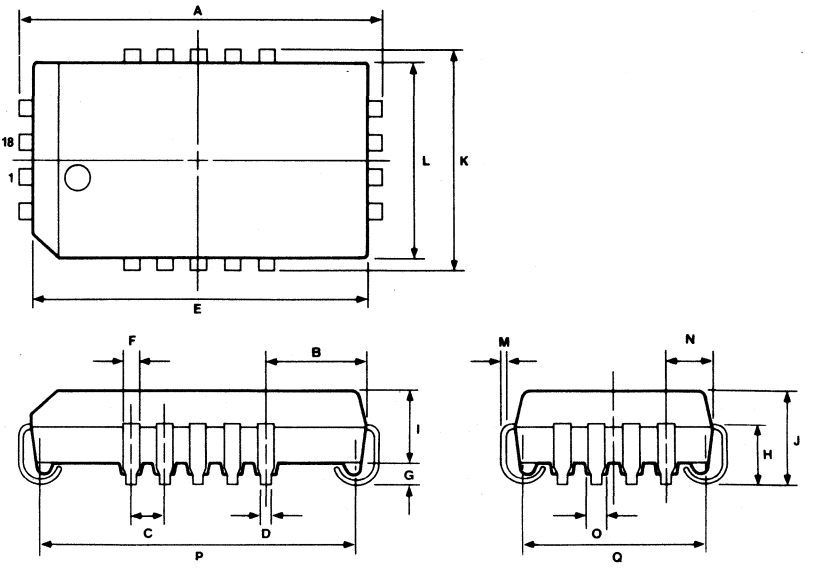
Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



18 PIN Plastic Leaded Chip Carrier

μPD41256L
μPD41257L
μPD41464L

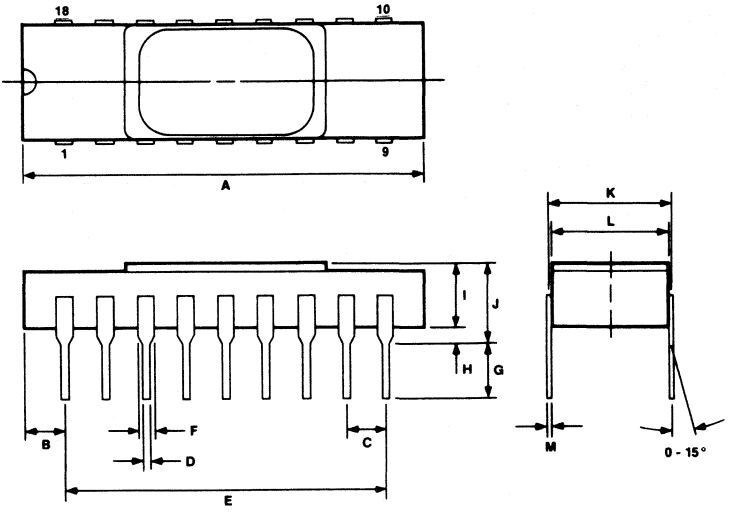
Item	Millimeters
A	13.4 ± .20
B	3.71 ± .15
C	1.27
D	.40 ± .10
E	12.5
F	.60
G	.8 min
H	2.40 ± .20
I	2.6
J	3.50 ± .20
K	8.30 ± .20
L	7.40
M	$.20^{+.10}_{-.05}$
N	1.80 ± .20
O	.70
P	11.68 ± .20
Q	6.6 ± .20



18 PIN Ceramic DIP (300 mil)

μPB10470D
μPB100470D

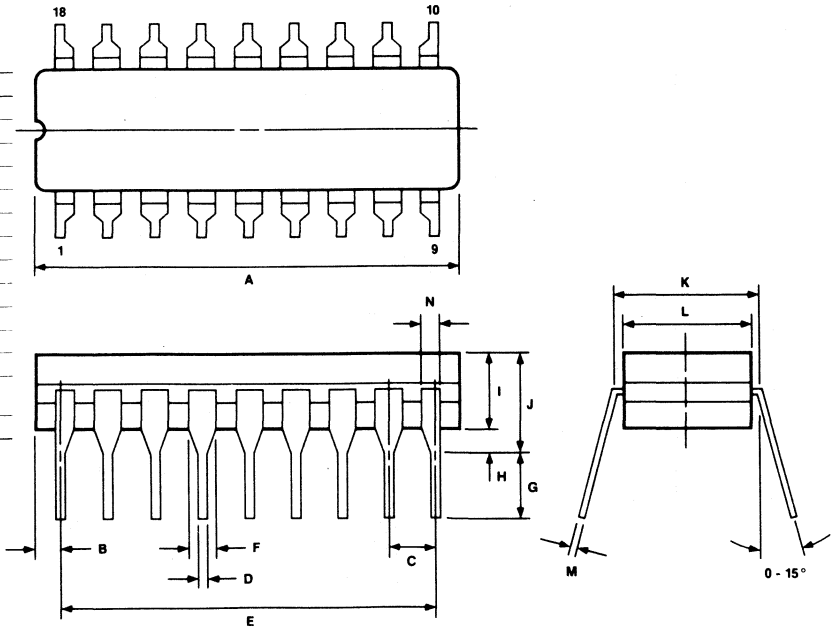
Item	Millimeters
A	25.40 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.90
J	4.57 max
K	7.62 [TP]
L	7.32
M	.25 ± .05



18 PIN Cerdip (300 mil)

μPB426D
μPB427D

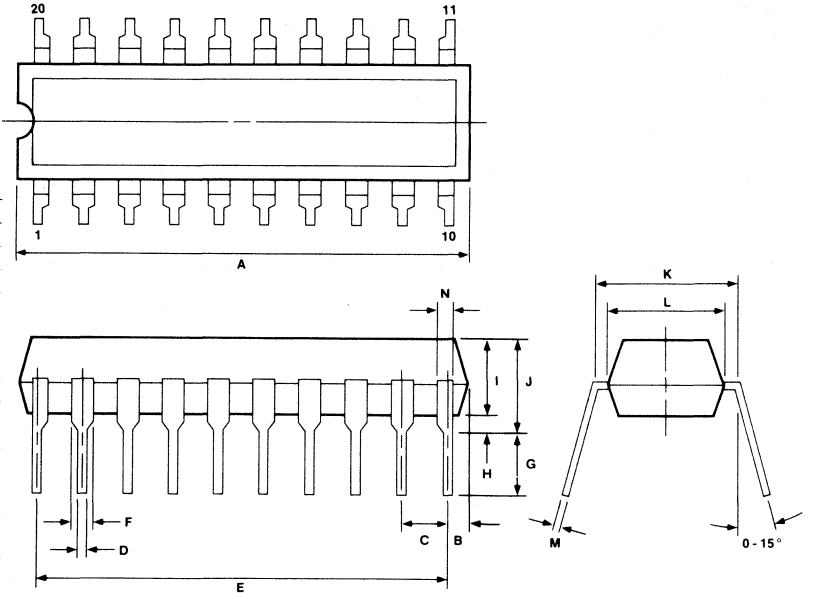
Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.42 min
G	3.5 ± .3
H	.51 min
I	3.95
J	5.08 max
K	7.62 [TP]
L	6.60
M	.25 ± .05
N	.89 min



20 PIN Plastic DIP (300 mil)

μPB421D
μPB424D
μPD4311C
μPD4314C
μPD43254C*

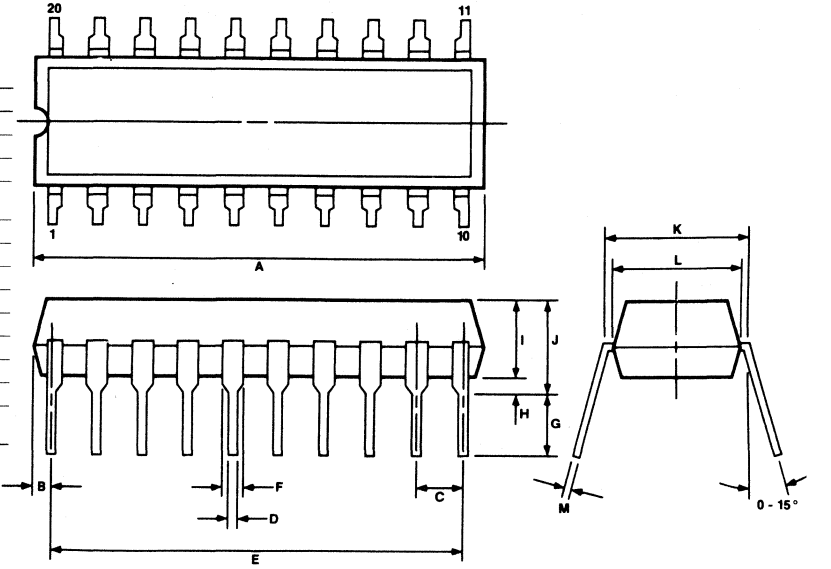
*under development



Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.1 min
G	3.5 ± .30
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	.9 min

20 PIN Plastic DIP (300 mil, Wide Body)

μPD424256C
μPD424258C

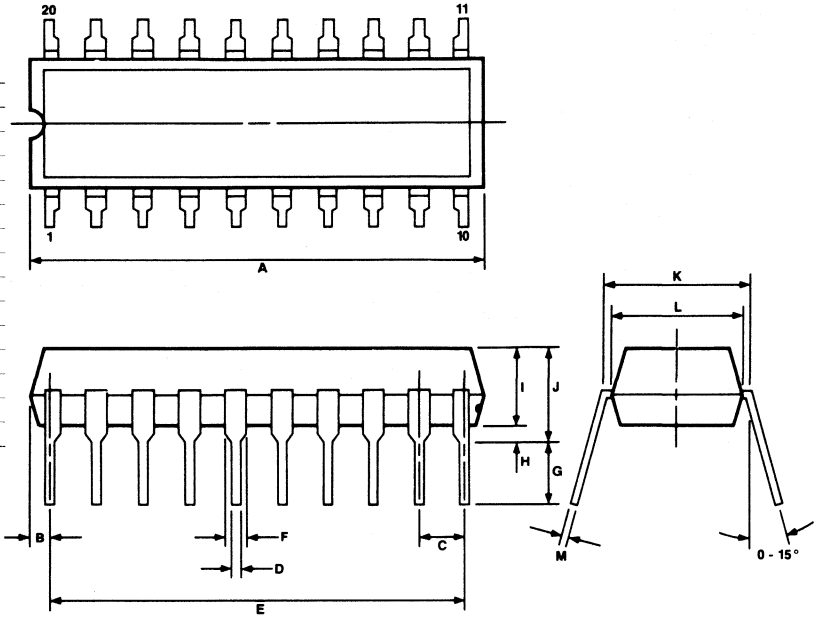


Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.25
M	$.25^{+.10}_{-.05}$

20 PIN Cerdip (300mil)

μPB421D
μPB424D

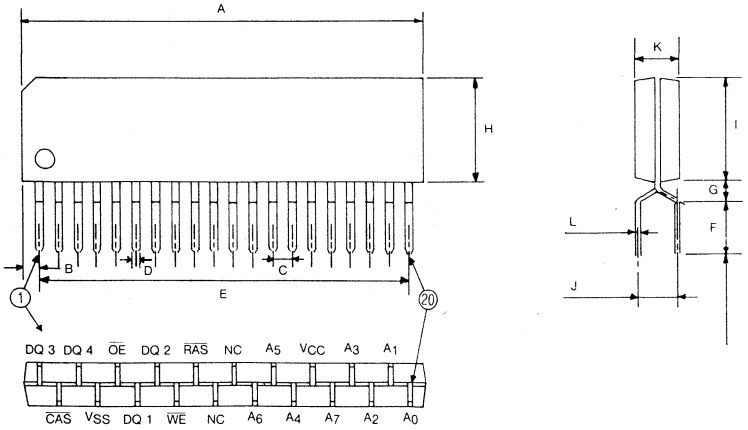
Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 (T.P.)
D	0.46 ± 0.05
F	1.42 min
G	3.5 ± 0.3
H	0.51 min
I	3.95
J	5.08 max
K	7.62 (T.P.)
L	7.32
M	0.25 ± 0.06
N	0.25
P	0.89 min



20-Pin ZIP

μPD41464V

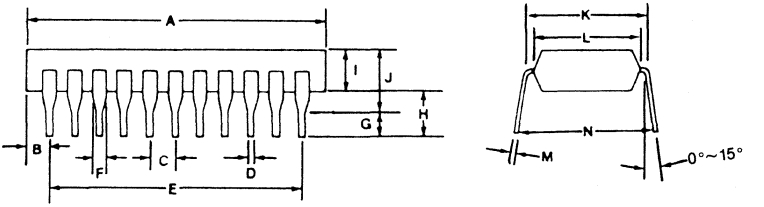
Item	Millimeters
A	26.67 max.
B	1.27 max.
C	1.27 (TP)
D	0.5±10
E	24,13
F	3.3±0,5
G	1.0 min.
H	7.0 max.
I	8.3 max.
J	2.54 (TP)
K	2.8±0,2)
L	$0.25^{+0.10}_{-0.05}$



22 PIN Plastic DIP

μPD4361C
μPD4362C

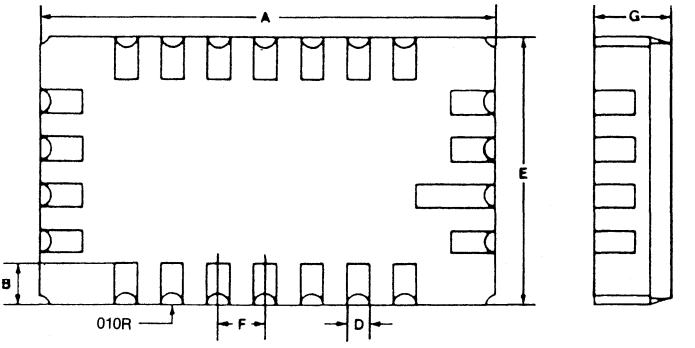
Item	Millimeters
A	27.5
B	0.8 max
C	2.54
D	0.5
E	25.4
F	1.2 min
G	3.2
H	3.8
I	4.31 min
J	5.08 max
K	7.62 typ
L	7.35
M	0.25
N	8.9



22 PIN Ceramic Leadless Chip Carrier

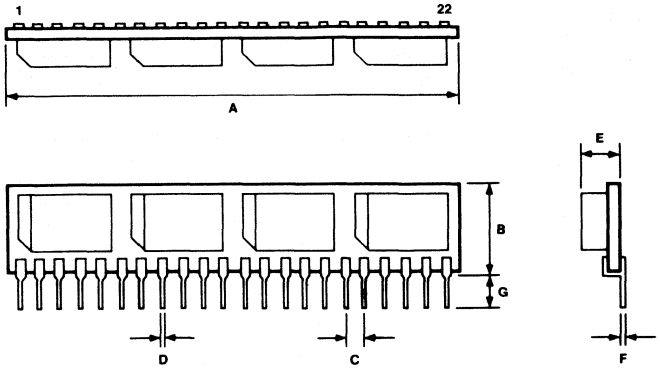
μPD4361K

Item	Millimeters
A	12.45
B	1.14
C	–
D	0.64
E	7.37
F	1.27
G	2.03



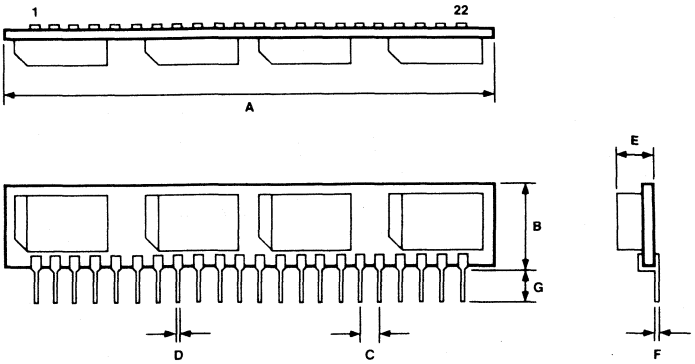
22 PIN SIMM, MC-41256A4A (Glass-epoxy Substrate)

Item	Millimeters
A	56.52
B	11.43 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



22 PIN SIMM, MC-411000A1A (Glass-epoxy Substrate)

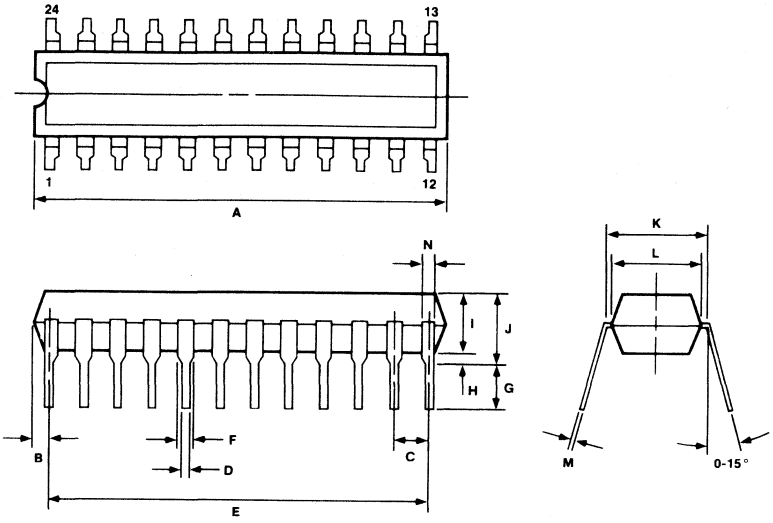
Item	Millimeters
A	61.0
B	10.92 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



24 PIN Plastic DIP (300 mil)

μPD41101C
μPD41102C
μPD42505C

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.50 ± 0.3
H	0.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min

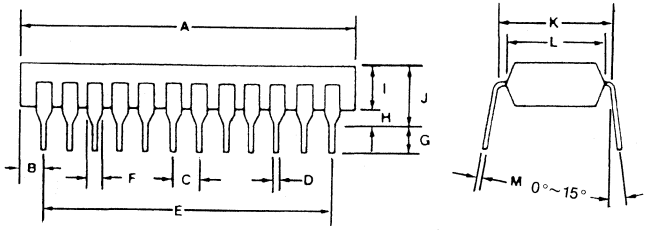


24 PIN Plastic Shrinkdip (300 mil)

μPD4016CX
μPD43251C*

*under development

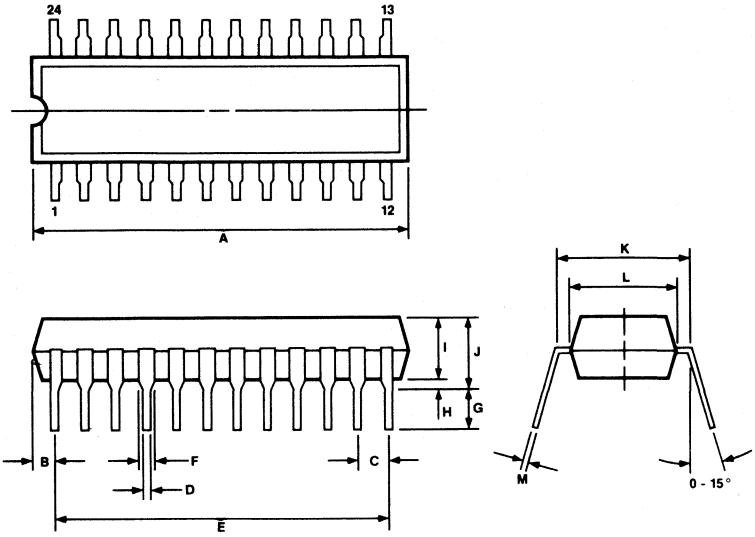
Item	Millimeters
A	33 max.
B	1.03
C	2.54
D	0.5±0.1
E	27.94 min
F	1.5
G	2.54 min.
H	0.5 min.
I	5.22 max.
J	5.72 max.
K	7.62
L	6.4
M	$0.25^{+0.01}_{-0.05}$



24 PIN Plastic DIP (400 mil)

μPD41264C

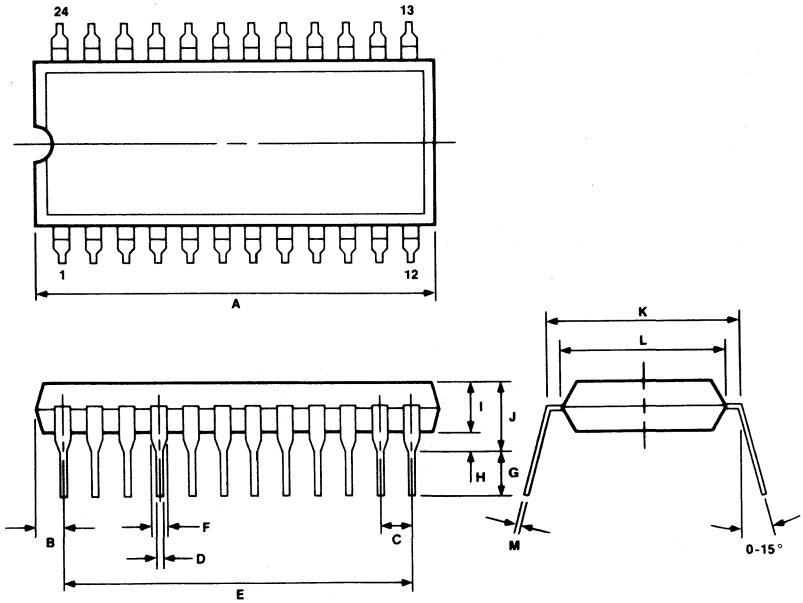
Item	Millimeters
A	30.48 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.2 ± 0.3
H	.51 min
I	4.31 max
J	5.08 max
K	10.16 [TP]
L	8.6
M	$.25^{+.10}_{-.05}$



24 PIN Plastic DIP (600 mil)

μPB405C
μPB408C
μPB409C
μPB417C
μPB419C
μPB425C
μPB428C
μPB429C
μPD4016C
μPD446C
μPD449C

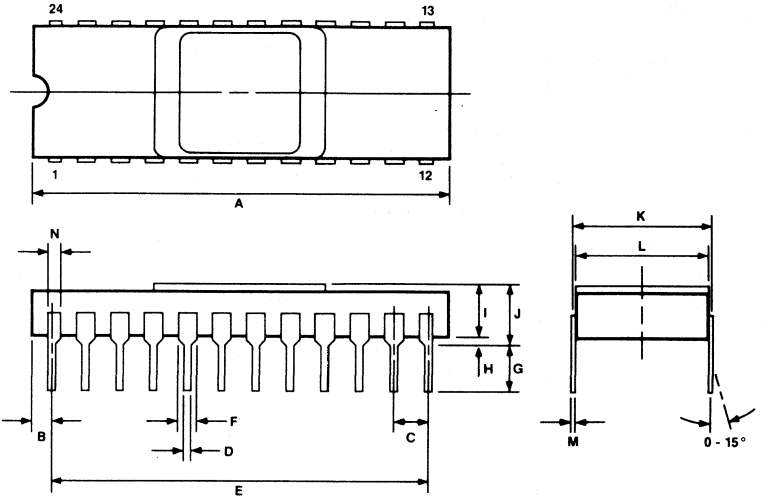
Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24 PIN Ceramic DIP (400 mil)

μPB10422D
μPB100422D
μPB10474D
μPB100474D

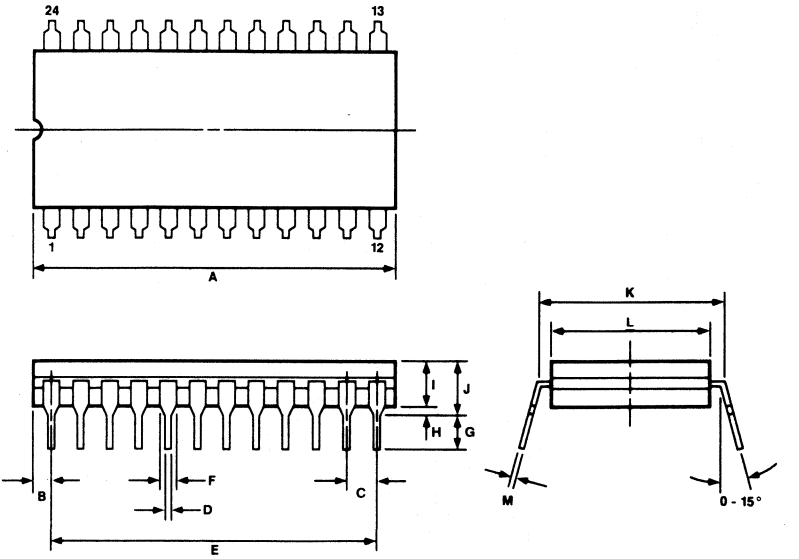
Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	27.94
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.74
J	4.57 max
K	10.16 [TP]
L	10.0
M	.25 ± .05
N	1.0 min



24 PIN Cerdip (600 mil)

μPB405D
μPB408D
μPB409D
μPB417D
μPB419D
μPB425D
μPB428D
μPB429D

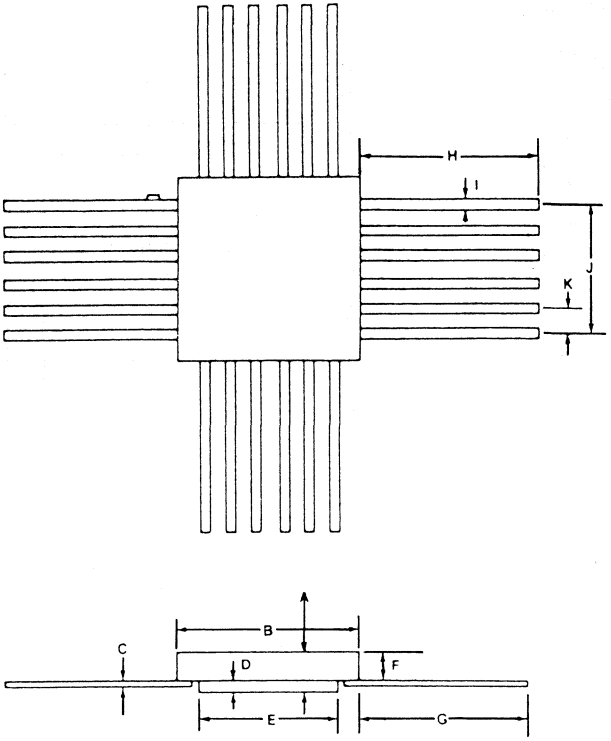
Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



24 PIN Flatpack

μPB100474B
μPB100422B

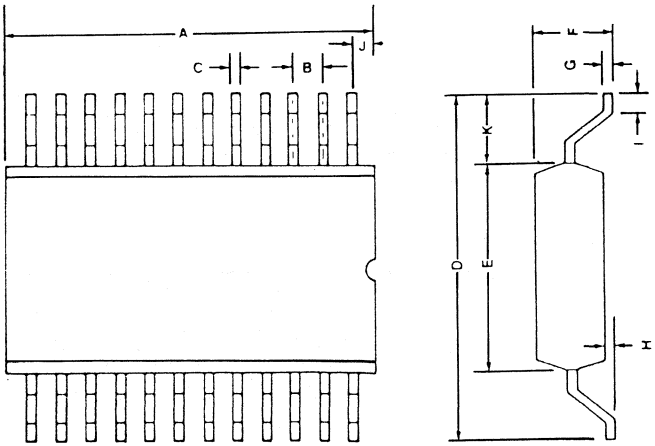
Item	Millimeters
A	2.5 (2.6 max)
B	9.5
C	0.13
D	0.5
E	6.9
F	2.0
G	8.9
H	8.9
I	0.43
J	6.35
K	1.27



24 PIN Miniflat

μPD449G

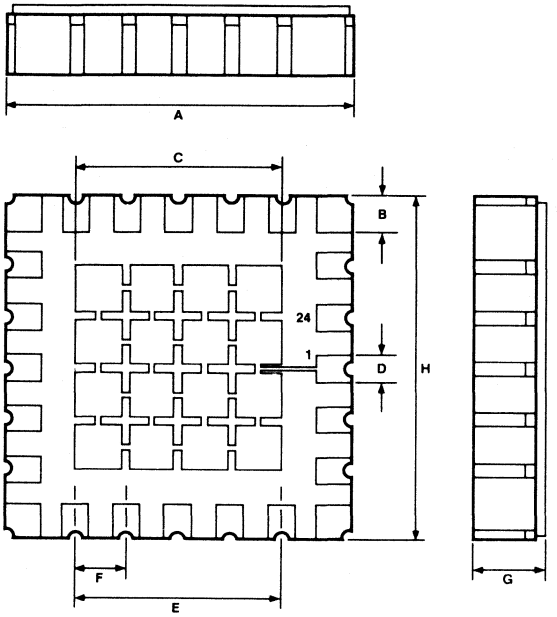
Item	Millimeters
A	15.8
B	1.27
C	0.4 ± 0.1
D	12.2
E	8.4
F	2.5 max
G	$0.15^{+0.10}_{-0.05}$
H	0.1 min
I	0.9
J	1.27 max
K	1.9 ± 0.2



24 PIN Ceramic LCC

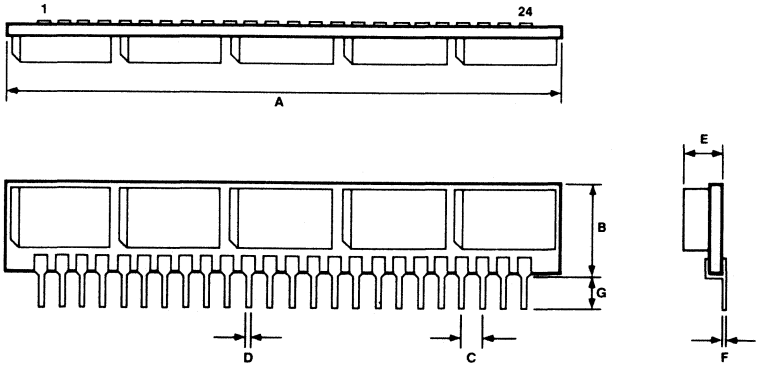
μPB100474K

Item	Millimeters
A	8.51
B	.89
C	5.14
D	.64
E	5.08
F	1.27
G	1.76
H	8.51



24 PIN SIMM, MC-41256A5A (Glass-epoxy Substrate)

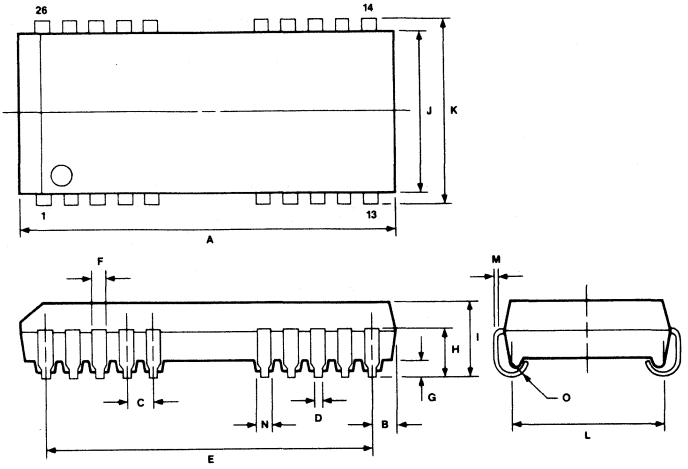
Item	Millimeters
A	68.60
B	11.40 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



26/20 PIN Plastic SOJ

μPD411000LA μPD421001LA
μPD411001LA μPD421002LA
μPD421000LA μPD424256LA
μPD424258LA

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad

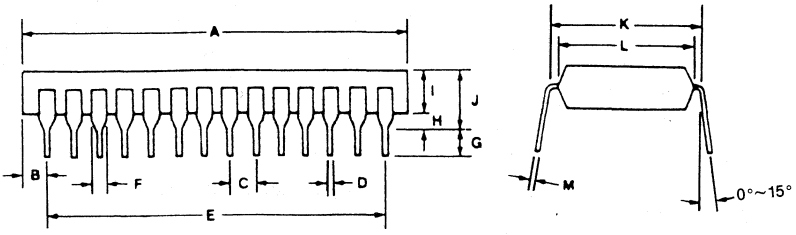


28 PIN Plastic DIP (600 mil)

μPD4168C μPD2364EC μPD2764C μPD27C256AC
μPD4364C-L μPD23128EC μPD23C128EC μPD27C512C*
μPD4464C-L μPD23C64EC μPD27256C μPD28C64C
μPD43256C μPD23C256C-1 μPD231000C μPD42832C
μPD43257C μPD23C256EAC μPD27C256C μPD23C1000C

*under development

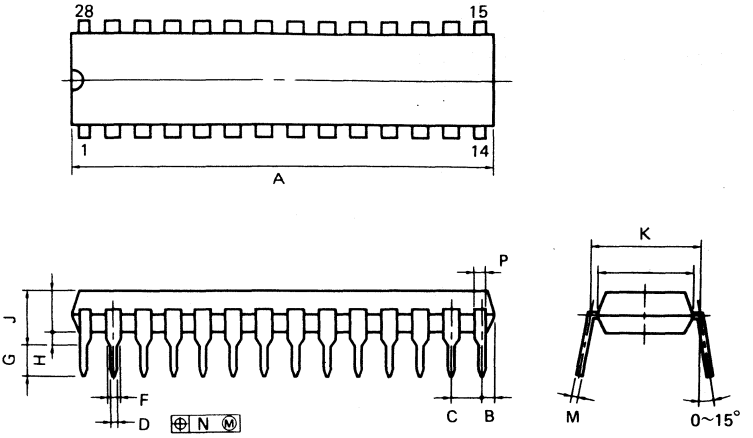
Item	Millimeters
A	38.0 max
B	2.49
C	2.54
D	0.5 ± 0.1
E	33.02
F	1.5
G	2.54 min
H	0.5 min
I	4.31 max
J	5.72 max
K	15.24
L	13.2
M	$0.25^{+0.01}_{-0.05}$



28 PIN Plastic DIP (300 mil)

μPD4364CX

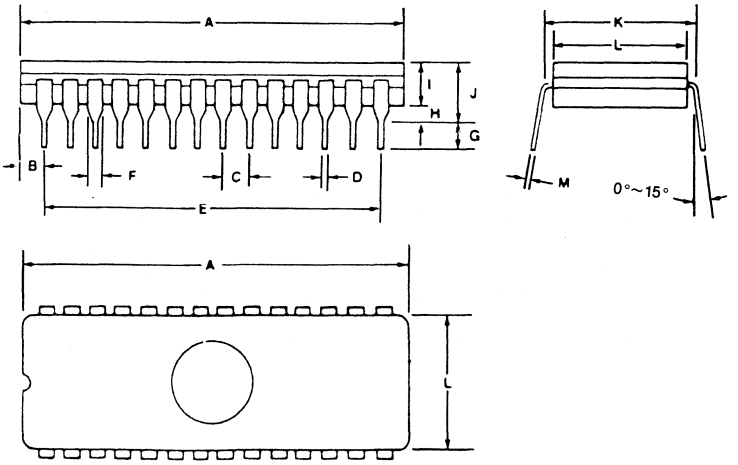
Item	Millimeters
A	35.56 max
B	1.27 max
C	2.54 (T.P.)
D	0.50 ± 0.10
F	1.2 min
G	3.2 ± 0.3
H	0.51 min
I	4.31 max
J	5.08 max
K	7.62 (T.P.)
L	6.7
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	1.0 min



28 PIN Cerdip (600 mil)

μPD27128D
μPD27256D
μPD27256AD
μPD27C256D
μPD27C256AD
μPD27C512D
μPD28C64D

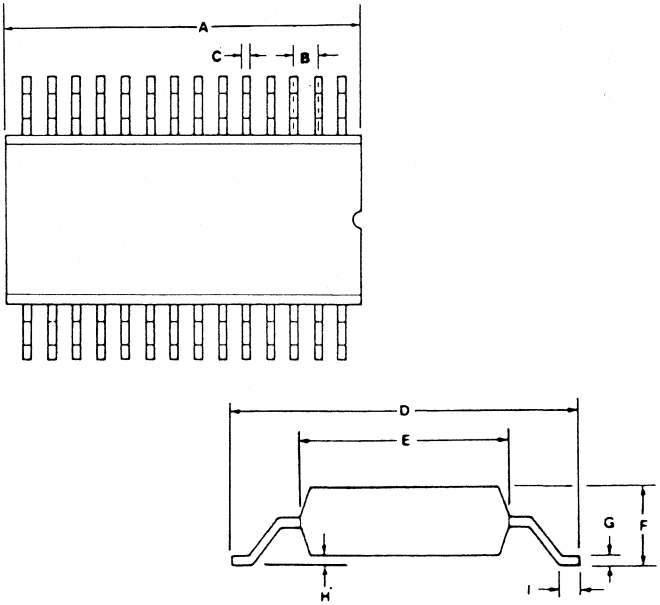
Item	Millimeters
A	38.10 max
B	2.78
C	2.54
D	0.5 ± 0.10
E	33.02
F	1.3
G	2.54 min
H	0.51 min
I	5.0 max
J	5.08 max
K	15.24
L	13.2
M	0.25 + 0.05



28PIN Miniflat

μPD4364G
μPD4463G
μPD23C256EG-1
μPD23C256EAG

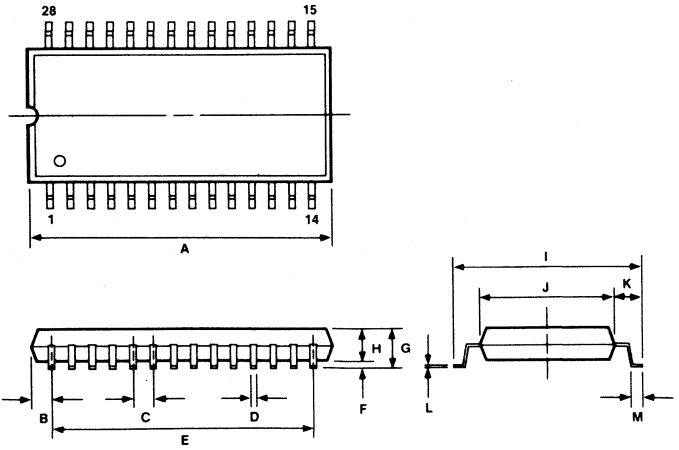
Item	Millimeters
A	18.0
B	1.27
C	0.4 ± 0.1
D	11.8
E	8.4
F	2.5
G	$0.15^{+0.10}_{-0.05}$
H	$0.1^{+0.2}_{-0.1}$
I	0.7



28 PIN Miniflat

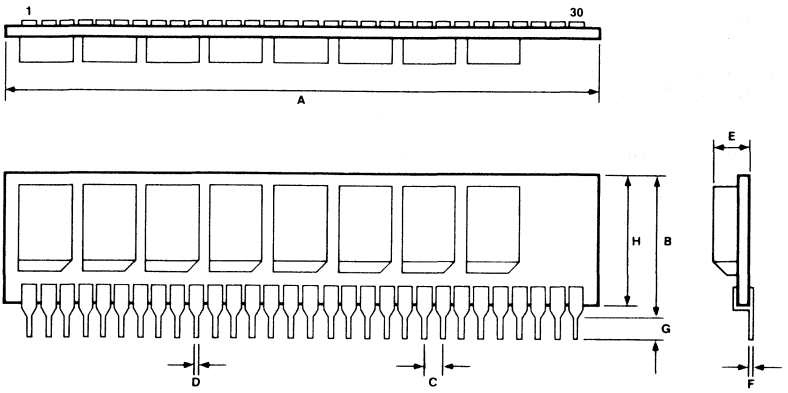
μPD43256GU
μPD42832G

Item	Millimeters
A	19.05 max
B	1.27 max
C	1.27 [TP]
D	.40 ± .10
E	16.51
F	$.1^{+.2}_{-.1}$
G	3.0 max
H	2.55
I	11.8 ± .3
J	8.4
K	1.7
L	$.15^{+.10}_{-.05}$
M	.7 ± .2



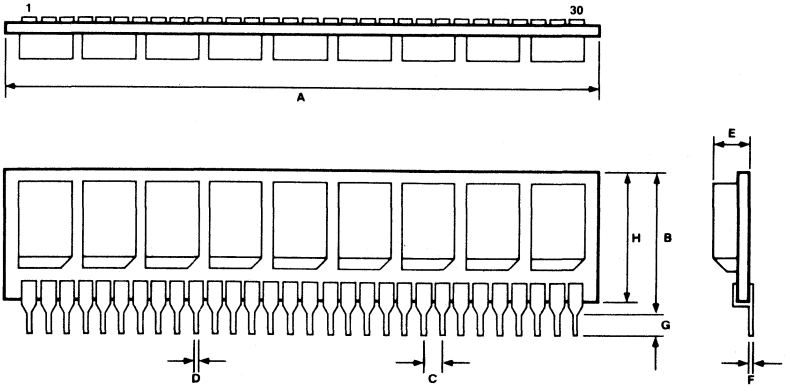
30 PIN SIMM, MC-41256A8A (Glass-epoxy Substrate)

Item	Millimeters
A	78.90
B	18.00 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00
H	16.76



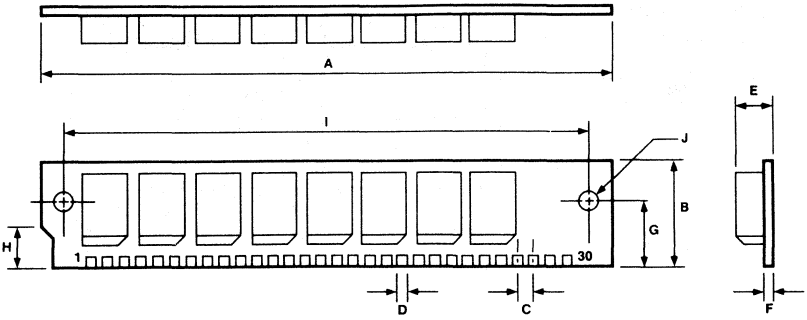
30 PIN SIMM, MC-41256A9A (Glass-epoxy Substrate)

Item	Millimeters
A	78.90
B	18.00 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00
H	16.76



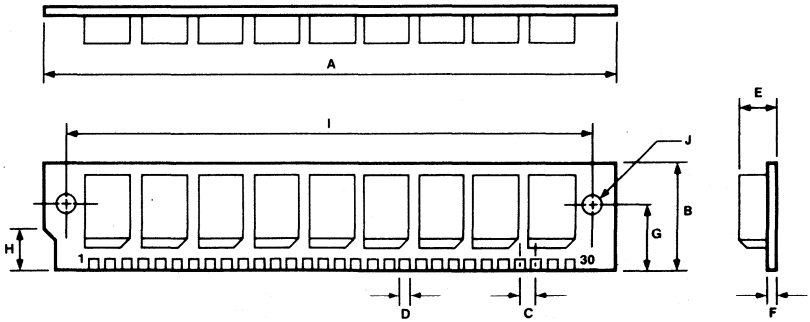
30 PIN SIMM, MC-41256A8B (Glass-epoxy Substrate)

Item	Millimeters
A	88.90
B	16.80 max
C	2.54
D	1.78
E	5.08 max
F	1.27 ± .08
G	10.16
H	6.35
I	82.10
J	3.175 dia



30 PIN SIMM, MC-41256A9B (Glass-epoxy Substrate)

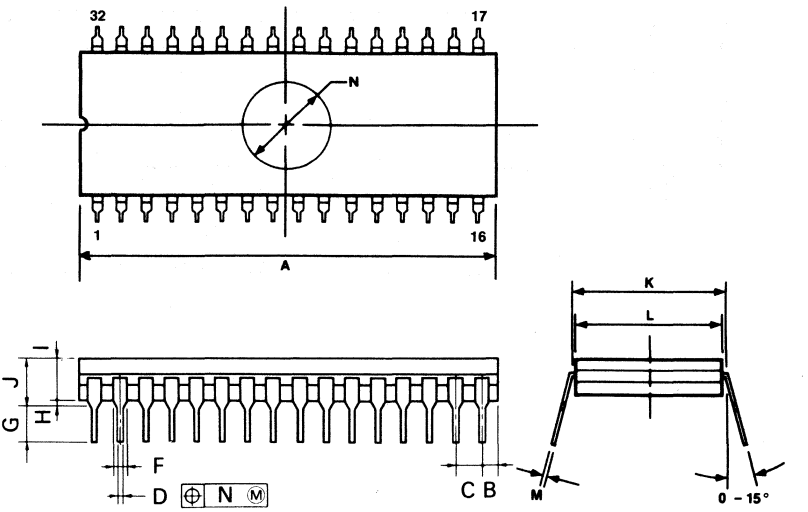
Item	Millimeters
A	88.90
B	16.80 max
C	2.54
D	1.78
E	5.08 max
F	1.27 ± .08
G	10.16
H	6.35
I	82.10
J	3.175 dia



32 PIN Ceramic DIP (600 mil)

μPD27C1000D
μPD27C1001D

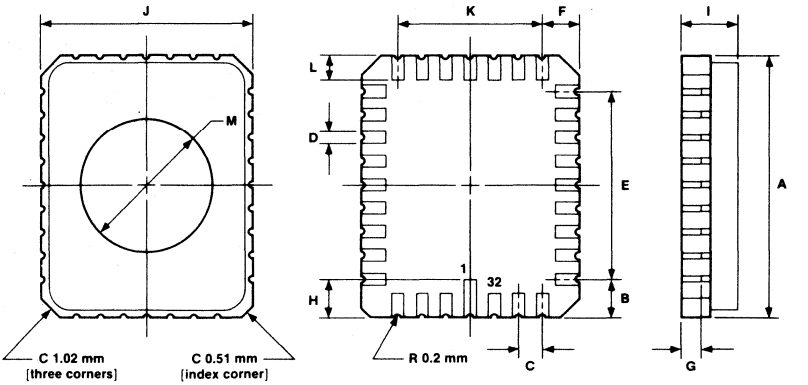
Item	Millimeters
A	43.18 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
F	1.2 min
G	3.5 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	14.66
M	.25 ± .05
N	8.89 dia



32 PIN Leadless Chip Carrier

μPD27C256AK

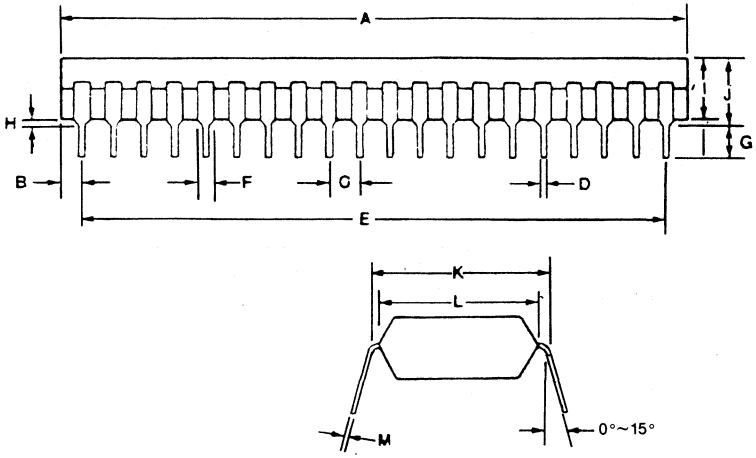
Item	Millimeters
A	13.97 ± 0.20
B	1.9
C	1.27
D	.64 ± .1
E	10.16
F	1.9
G	1.02
H	2.17
I	3.0 max
J	11.43 ± .15
K	7.62
L	1.27 ± .15
M	7.11 dia



40 PIN Plastic DIP (600 mil)

μPD23C2000C

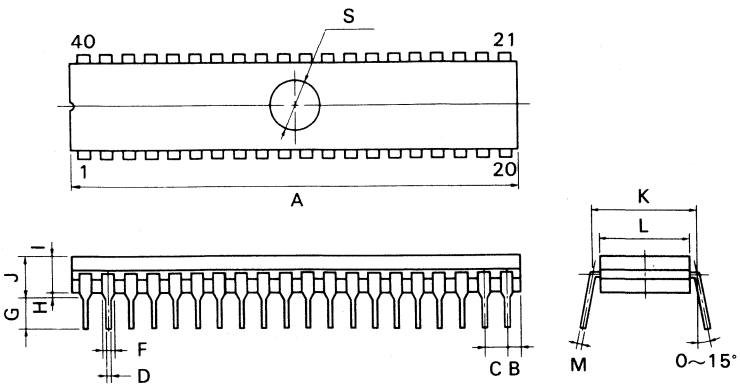
Item	Millimeters
A	53.34 max
B	2.54 max
C	2.54 ± 0.1
D	0.5 ± 0.1
E	48.26 ± 0.1
F	1.2 min
G	2.54 min
H	0.5 min
I	4.31 max
J	5.72 max
K	15.24 typ
L	13.2 typ
M	$0.25^{+0.1}_{-0.05}$



40 PIN Cerdip (600 mil)

μPD27C1024D

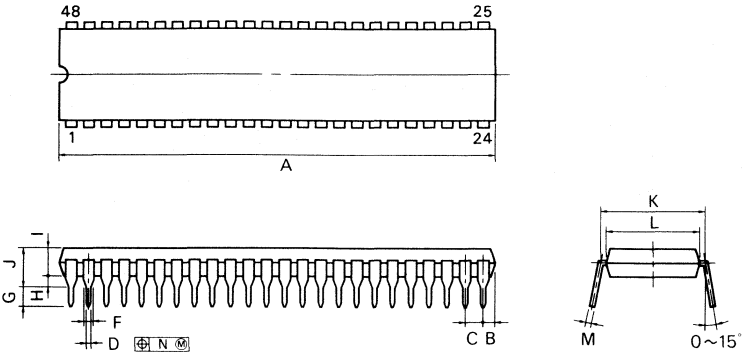
Item	Millimeters
A	53.34 max
B	2.54 max
C	2.54 (T.P.)
D	0.50 ± 0.10
F	1.2 min
G	3.5 ± 0.3
H	0.51 min
I	3.80
J	5.08 max
K	15.24 (T.P.)
L	14.66
M	0.25 ± 0.05
N	0.25
S	Ø 8.89



48 PIN Plastic DIP (600 mil)

μPB450BC

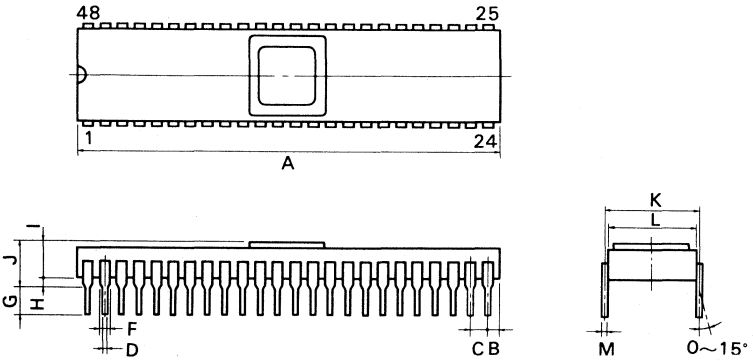
Item	Millimeters
A	63.50 max
B	2.54 max
C	2.54 (T.P.)
D	0.50±0.10
F	1.1 min
G	3.6±0.3
H	0.51 min
I	4.31 max
J	5.72 max
K	15.24 (T.P.)
L	13.8
M	$0.25^{+0.10}_{-0.05}$
N	0.25



48 PIN Ceramic DIP (600 mil)

μPB450BD

Item	Millimeters
A	63.50 max
B	2.54 max
C	2.54 (T.P.)
D	0.46±0.05
F	0.92 min
G	3.5±0.3
H	1.0 min
I	2.74
J	4.57 max
K	15.24 (T.P.)
L	14.93
M	0.25±0.05
N	0.25



CROSS REFERENCE CHARTS

CROSS REFERENCE

Dynamic RAMs

NEC	Organization	MODE	Process	Fujitsu	Hitachi	Mitsubishi	Toshiba	Ti
μPD4164	65,536 x 1	Page	NMOS	MB8264A	HM4864A	M5K4164AN	TMM4164A	TMS4164A
μPD41416	16,384 x 4	Page	NMOS	MB81416	HM48416A	M5M4416	–	TMS4416
μPD41256	262,144 x 1	Page	NMOS	MB81256	HM50256	M5M4256	TMM41256	TMS4256
μPD41257	262,144 x 1	Nibble	NMOS	MB81257	HM50257	M5M4257	TMM41257	TMS4257
μPD41464	65,536 x 4	Page	NMOS	MB81464	HM50464	M5M4464	TMM41464	TMS4464
μPD42832	32,768 x 8	–	CMOS	–	HM65256BP	–	TC51832	–
μPD411000	1,048,576 x 1	Page	NMOS	MB811000	–	–	–	–
μPD411001	1,048,576 x 1	Nibble	NMOS	MB811001	–	–	–	–
μPD421000	1,048,576 x 1	Fast Page	CMOS	MB81C1000	HM511000	M5M4C1000	TC511000	TMX4C1024
μPD421001	1,048,576 x 1	Nibble	CMOS	MB81C1001	HM511001	M5M4C1001	TC511001	TMX4C1025
μPD421002	1,048,576 x 1	Stat. Column	CMOS	MB81C1002	HM511002	M5M4C1002	TC511002	TMX4C1027
μPD424256	262,144 x 4	Fast Page	CMOS	MB81C4256	HM514256	M5M44C256	TC514256	TMX44C256
μPD424258	262,144 x 4	Stat. Column	CMOS	MB81C4258	HM514258	M5M44C258	TC514258	TMX44C257
μPD41264	65,536 x 4 256 x 4	Dual Port Video RAM	NMOS (NEC)	MB81461	HM53461	M5M4C264	–	TMX4461

CROSS REFERENCE

ECL RAMs

NEC	Organization	Fujitsu	Hitachi	Fairchild
μPB10422	256 x 4	MBM10422A	HM10422	F10422
μPB100422	256 x 4	MBM100422A	HM100422	F100422
μPB10470	4K x 1	MBM10470A	HM10470	F10470
μPB100470	4K x 1	MBM100470A	HM100470	F100470
μPB10474	1K x 4	MBM10474A	HM10474	F10474
μPB100474	1K x 4	MBM100474A	HM100474	F100474

CROSS REFERENCE

STATIC RAMS

NEC	Function	Package	Fujitsu	Hitachi	Matsushita	Mitsubishi	Oki	Sharp	Sony	Seiko	Toshiba
μPD4016	2048x8 SRAM	24 DIP 24 SKDIP	MB8128	HM 6116 HM6116SP	MN 4216		MSM 2128	LH 2128			TMM2016 TMM2015
μPD4311	16384x1 SRAM	20 DIP	MB81C67	HM 6267 HM 6167		M5M21C67					
μPD4314	4096x4 SRAM	20 DIP	MB81C68	HM 6168		M5M2168					TMM2068 TMM2069
μPD446/L	2048x8 SRAM	24 DIP	MB8416	HM 6116A	MN 4416	M5M5117	MSM 5128	LH 5128		SRM 2016	TC5517
μPD449/L	2048x8 SRAM	24 DIP 24 SOP	MB8418	HM6117		M5M5118				SRM 2019	TC5518
μPD4361C	65536x1 SRAM	22 DIP	MB81C71	HM 6287P							TC5561
μPD4361K	65536x1 SRAM	22 LCC Cerdip		HM6267CG							
μPD4362	16384x4 SRAM	22 DIP	MB81C74	HM 6288			MSM 5165				TC55416 TC55417
μPD4363	16348x4 SRAM	24 DIP									
μPD4364L μPD4364LL	8192x8 SRAM	28 DIP 28 SOP	MB8464	HM 6264		M5M5165	MSM 5105	LH5164	CXK 5864	SRM 2064	TC 5565
μPD4464L	8192x8 SRAM	28 DIP 28 SOP				M5M5164	MSM 5164				TC 5564
μPD4168	8192x8 P-SRAM	28 DIP									
μPD43256	32768x8 SRAM	28 DIP 28 SOP	MB84256	HM 62256		M5M5256			CXK 58256	SRM20256	TC55257
μPD43251*	256Kx1 SRAM	24 DIP 24 LCC	MBM 81C81								
μPD43254*	64Kx4 SRAM	24 DIP 24LCC	MBM 81C84 81C86								
μPD43257*	32Kx8 SRAM	28 DIP									
μPD4368*	8Kx8 SRAM	28 DIP	MBM 81C78A								
μPD4369*	8Kx9 SRAM	30 DIP	MBM 81C79								
μPD44256*	32Kx8 SRAM	28 DIP			MN 44256						

* under development

CROSS REFERENCE

STATIC RAMS

NEC	Function	Package	Intel	Motorola	National	AMD	Ti	Inmos	Matra Harris	RCA	Fairchild	IDT	Cypress
μPD4016	2048x8 SRAM	24 DIP 24 SKDIP	P/D 2128	MCM2016		AM 9128	TMS 4016				F 3528		
μPD4311	16384x1 SRAM	20 DIP	i51C67	MCM 2167H				IMS 1400	HM65261 HM65262			IDT6167A	CY7C167
μPD4314	4096x4 SRAM	20 DIP	i51C68/ 51C69	MCM 6168H		AM 2168		IMS 1421 IMS1420	HM65681			IDT6168A	CY7C168 CY7C169
μPD446/L	2048x8 SRAM	24 DIP								CMD 6116A			
μPD449/L	2048x8 SRAM	24 DIP 24 SOP		MCM 6116									
μPD4361C	65536x1 SRAM	22 DIP				AM99C641		IMS 1600			F 1600	IDT 7187S	CY7C187
μPD4361K	65536x1 SRAM	22 LCC Cerdip						IMS 1600					
μPD4362	16384x4 SRAM	22 DIP		MCM6187				IMS 1620				IDT 7188	
μPD4363	16384x4 SRAM	24 DIP											
μPD4364L μPD4364LL	8192x8 SRAM	28 DIP 28 SOP		MCM6164		AM99C88/L			HM 62642	CDM 6264			
μPD4464L	8192x8 SRAM	28 DIP 28 SOP	i51C86 i51C87		NMC6164								
μPD4168	8192x8 P-SRAM	28 DIP	i2186										
μPD43256	32768x8 SRAM	28 DIP											

CROSS REFERENCE

UVPROMS

NEC	Fujitsu	Hitachi	Mitsubishi	Oki	Toshiba
μPD2764	MBM 2764	HN 482764	M5L 2764	MSM 2764	
μPD27128	MBM 27128	HN4827128	M5L 27128	MSM 27128	
μPD27256					TMM 27256
μPD27256A	MBM 27256	HN 27256	M5L 27256	MSM 27256	TMM 27256AD
μPD27C64	MBM 27C64	HN 27C64			
μPD27C256	MBM 27C256				TC 57256
μPD27C256A	MBM27C256A	HN 27C256	M5L 27C256		
μPD27C512	MBM27C512				
μPD27C1000	MBM27C1000	HN 27C301			TC 571000
μPD27C1001	MBM27C1001	HN 27C101			TC 571001
μPD27C1024	MBM27C1024	HN27C1024			TC 571024

CROSS REFERENCE

UV PROMS

NEC	AMD	Intel	SEEQ	Texas Instruments	VLSI Technology	SGS	Thomson CSF
μPD2764	AM 2764	D 2764	DQ 2764	TMS 2764		M 2764	ET 2764
μPD27128	AM 27128	D 27128	DQ 27128	TMS 27128			ET 27128
μPD27256							
μPD27256A	AM 27256	D 27256		TMS 27256			
μPD27C64		D 27C64					
μPD27C256							
μPD27C256A		D 27C256	DQ 27C256A	TMS 27C256	VT 27C256		ET 27C256
μPD27C512		D 27C512					
μPD27C1000							
μPD27C1001		D 27010					
μPD27C1024	AM27C1024	D 27210					

DYNAMIC MOS RAM

65536 x 1-BIT DYNAMIC MOS RAM

DESCRIPTION

The NEC μPD4164 is a 65,536 words by 1 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative voltage substrate bias is internally generated – its operation is both automatic and transparent.

The μPD4164 utilizes a double poly N-channel silicon process which provides high storage cell density, high performance and high reliability.

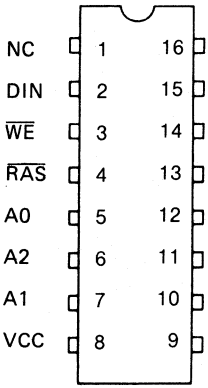
The μPD 4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

	Access Time	RW-Cycle	R/W-Cycle	Power (max.)
μPD4164 -12	120 NS	255 NS	230 NS	303 mW
μPD4164 -3	150 NS	280 NS	260 NS	275 mW
μPD4164 -2	200 NS	345 NS	330 NS	250 mW

FEATURES

- 65,536 x 1 bit Organization
- High Memory Density
- Multiplexed Address Inputs
- Single + 5V (± 10 %) Power Supply
- On Chip Substrate Bias Generator
- Low Power Dissipation: 28 mW (Standby)
- Non-latched Output is Three-State. TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, $\overline{RAS}$ Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Input Capacitance
- 128 Refresh Cycles (A_0 - A_6 Pins for Refresh Address)
- $\overline{CAS}$ controlled output allows Hidden Refresh
- Available in Plastic (4164C)
  16 Pin 300 Mil Dual in Line Package.

PIN CONFIGURATION



Pin Names

A0 - A7	—	Address Inputs
RAS	—	Row Address Strobe
CAS	—	Column Address Strobe
WE	—	Write Enable
DIN	—	Data Input
DOUT	—	Data Output
VCC	—	Power Supply (+5V)
VSS	—	Ground
NC	—	No Connection

ABSOLUTE MAX. RATINGS

Voltage on any pin relative to VSS	-1,0 to +7,0 V
Operating temperature, Ta (Ambient)	0 to +70°C
Storage temperature, Tstg (Ambient)	-55 to 125°C
Short circuit output current	50 mA
Power dissipation	1 W

Comment:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	VCC VSS	4.5 0	5.0 0	5.5 0	V V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.4		5.5	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0		0.8	V	1

DC Electrical Characteristics (Ta = 0 to +70°C)

(T_a = 0 to +70°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Supply Standby Current ($\overline{RAS}$ = VIH, DOUT = High Impedance)	ICC2			5.0	mA	
Input Leakage Current, any input (VIN = 0 to +5.5 V, all other pins not under test = 0 V)	II(L)	-10		10	μA	
Output Leakage Current (DOUT is Disabled, VOUT = 0 to +5.5 V)	IO(L)	-10		10	μA	
Output High (Logic 1) Voltage (I_{OUT} = -5 mA)	VOH	2.4		VCC	V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2 mA)	VOL	0		0.4	V	

Electrical Characteristics and recommended AC operating conditions (Notes 1, 2, 3, 4)
($0\,°C \leq T_a \leq 70\,°C$) $V_{CC} = 5.0\,V \pm 10\%$)

PARAMETER	Symbol	μPD 4164-12		μPD 4164-3		μPD 4164-2		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RCMIN}$)	I_{CC1}		55		50		45	mA	5
Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RCMIN}$)	I_{CC3}		45		40		35	mA	5
Average power supply current, page mode operation ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{RC} = t_{PCMIN}$)	I_{CC4}		45		40		35	mA	5
Random read or write cycle time	t_{RC}	230		260		330		ns	6
Read-write cycle time	t_{RWC}	255		280		345		ns	6
Page mode cycle time	t_{PC}	130		145		190		ns	6
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	7,8
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	7,9
Output buffer turn-off delay	t_{OFF}	0	35	0	40	0	50	ns	10
Transition time (rise and fall)	t_T	3	35	3	35	3	50	ns	4
$\overline{RAS}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	30	100	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	12
$\overline{CAS}$ precharge time, non-page cycles	t_{CPN}	25		25		30		ns	
$\overline{CAS}$ precharge time page cycle	t_{CP}	60		60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
ROW address set-up time	t_{ASR}	0		0		0		ns	
ROW address hold time	t_{RAH}	15		15		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		30		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		25		ns	13
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	13
Write command hold time	t_{WCH}	35		45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		155		ns	
Write command pulse width	t_{WP}	35		45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55			
Data-in set-up time	t_{DS}	0		0		0		ns	14
Data-in hold time	t_{DH}	35		45		55		ns	14
Data-in hold time referenced $\overline{RAS}$	t_{DHR}	95		120		155		ns	
Refresh period	t_{REF}		2		2		2	ms	
$\overline{WE}$ command set-up time	t_{WCS}	-10		-10		-10		ns	15
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		55		ns	15
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100		120		140		ns	15

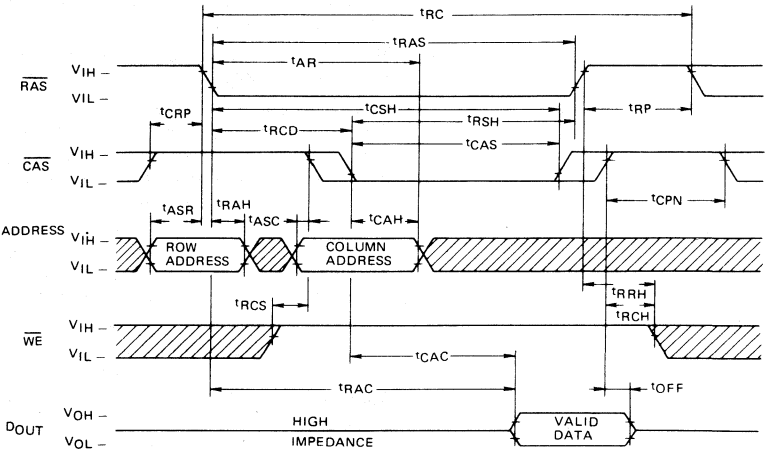
NOTES:

1. All voltages referenced to VSS.
2. An initial pause of 100 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
3. AC measurements assume $t_T = 5$ ns.
4. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. I_{CC1}, I_{CC3}, and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the output open.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (Ta = 0 to 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., $\overline{CAS}$ cycling during the $\overline{RAS}$ precharge time). If t_{CRP} period and in that case $\overline{CAS}$ precharge time should be t_{CP}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out at access time and until $\overline{CAS}$ goes back to V_{IH} is indeterminate.

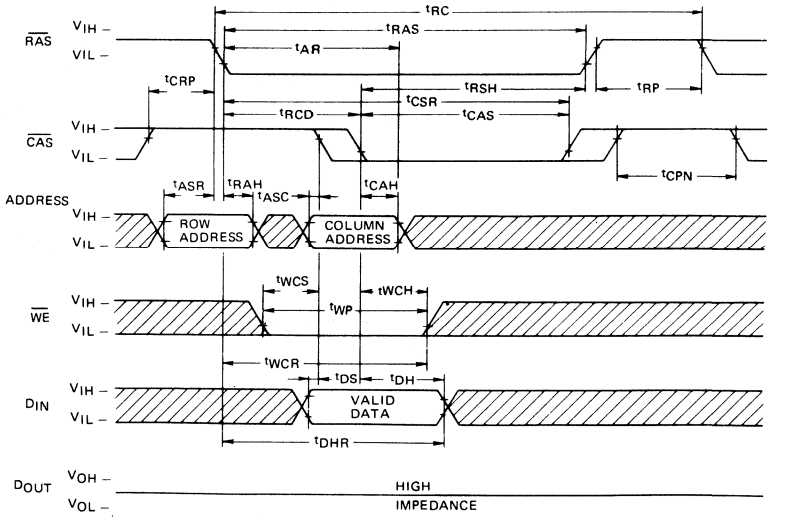
A.C. Electrical Characteristics ($0°C \leqq Ta \leqq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance ($A_0 \sim A_7$, D_{IN})	C_{I1}		5	pF	
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}		8	pF	
Output Capacitance (D_{OUT})	C_O		7	pF	

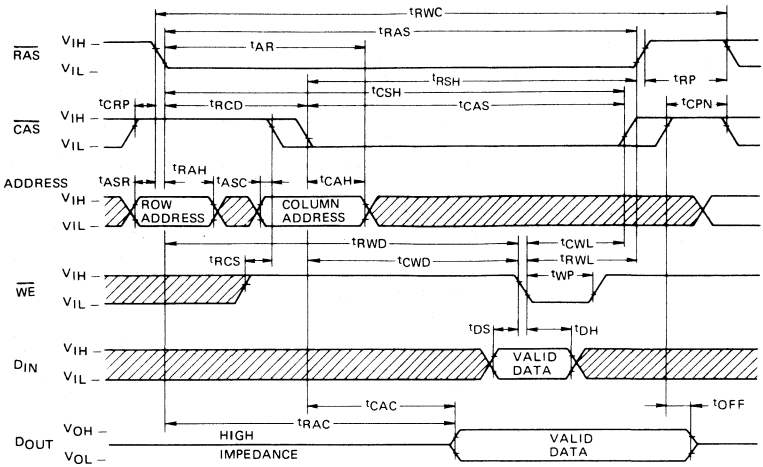
READ CYCLE



WRITE CYCLE
(EARLY WRITE)

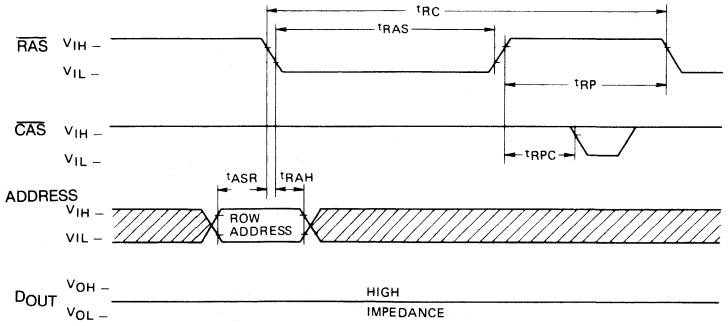


READ-WRITE / READ-MODIFY-WRITE CYCLE

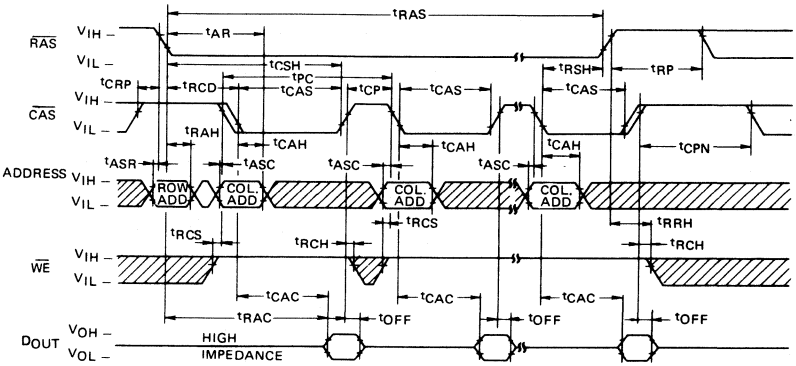


„RAS ONLY" REFRESH CYCLE

WRITE = Don't Care

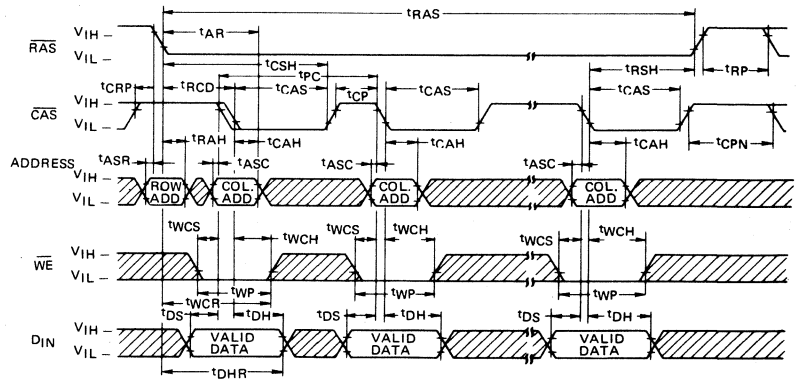


PAGE MODE READ CYCLE

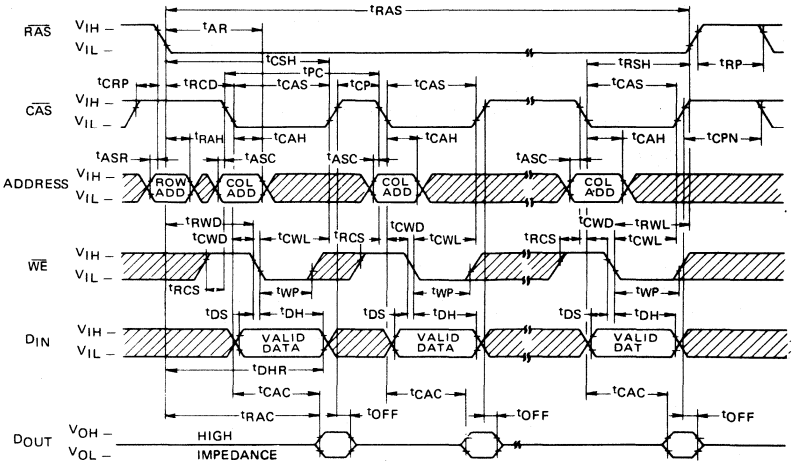


PAGE MODE WRITE CYCLE

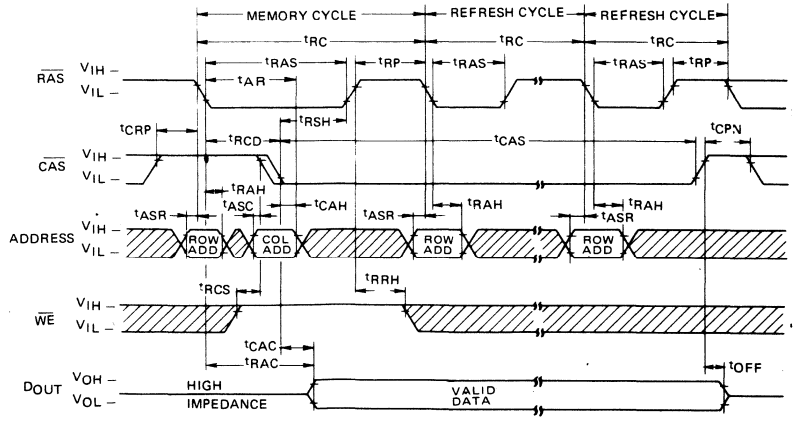
(EARLY WRITE)



PAGE MODE READ-WRITE / READ-MODIFY-WRITE CYCLE

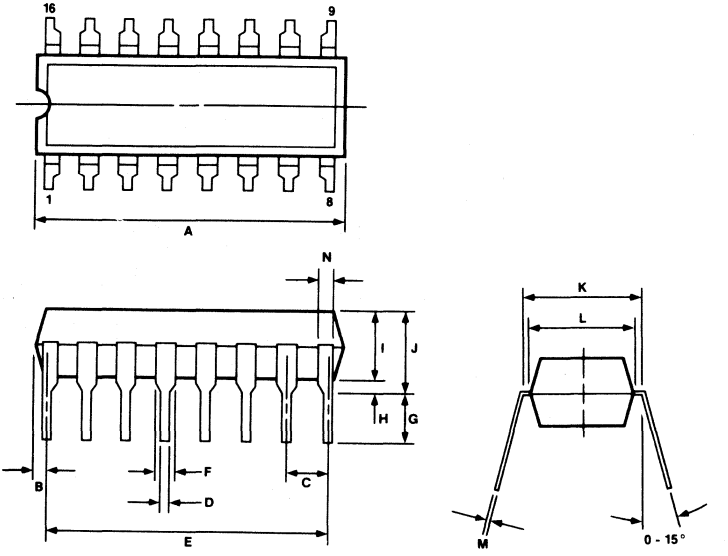


HIDDEN REFRESH CYCLE



Package Dimensions
16-PIN Plastic DIP

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.5 ± .03
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



16384 x 4-BIT DYNAMIC MOS RAM

DESCRIPTION

The NEC μPD41416 is a 16,384 words by 4 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative voltage substrate bias is internally generated – its operation is both automatic and transparent.

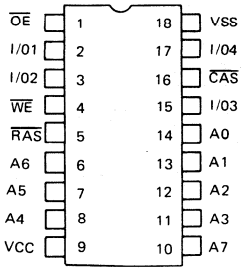
The μPD41416 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

	Access Time	RW-Cycle	R/W-Cycle	Power (max.)
μPD41416 -12	120 NS	300 NS	220 NS	303 mW
μPD41416 -15	150 NS	355 NS	260 NS	275 mW
μPD41416 -20	200 NS	445 NS	330 NS	250 mW

FEATURES

- 16,384 x 4 bits Organization
- High Memory Density
- Multiplexed Address Inputs
- Single + 5V (± 10 %) Power Supply
- On Chip Substrate Bias Generator
- Low Power Dissipation: 28 mW (Standby), 303 mW active (T_{RC} = 220 ns)
- Non-latched Output is Three-State. TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, $\overline{RAS}$ Only Refresh, and Page Mode Capability
- All Inputs TTL compatible, and Low Input Capacitance
- 128 Refresh Cycles (A_0 - A_6 Pins for Refresh Address) during 2 ms
- $\overline{CAS}$ controlled output allows Hidden Refresh
- Available in Plastic (41416C) 18 Pin Package

PIN CONFIGURATION



PIN NAMES

A0 - A7	:	ADDRESS INPUTS
$\overline{RAS}$	:	ROW ADDRESS STROBE
$\overline{CAS}$	:	COLUMN ADDRESS STROBE
$\overline{WE}$	:	WRITE ENABLE
IO 1-4	:	DATA IN / DATA OUT
$\overline{OE}$	:	OUTPUT ENABLE
VCC	:	POWER SUPPLY
VSS	:	GROUND

ABSOLUTE MAX. RATINGS

Voltage on any pin relative to V_{SS}	-1,0 to +7,0 V
Operating temperature, T_a (Ambient)	0 to +70°C
Storage temperature, T_{stg} (Ambient)	-55 to +125°C (Plastic)
Short circuit output current	50 mA
Power dissipation	1 W

Comment:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

(T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4		5.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0		0.8	V	1

DC Electrical Characteristics

(T_a = 0 to +70°C, V_{CC} = 5.0 V ± 10 %)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)	I_{CC2}			5.0	mA	
Input Leakage Current, any input (VIN = 0 to +5.5 V, all other pins not under test = 0 V)	$I_{I(L)}$	-10		10	μA	
Output Leakage Current (D_{OUT} is Disabled, V_{OUT} = 0 to +5.5 V)	$I_{O(L)}$	-10		10	μA	
Output High (Logic 1) Voltage (I_{OUT} = -2 mA)	V_{OH}	2.4		V_{CC}	V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2 mA)	V_{OL}	0		0.4	V	

Electrical Characteristics and recommended AC operating conditions (Notes 2, 3, 4)
(0 °C ≦ T_a ≦ 70 °C) (V_{CC} = 5.0 V ± 10 %)

PARAMETER	SYMBOL	μPD41416C-12		μPD41416C-15		μPD41416C-20		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RCMIN})	I_{CC1}		55		50		45	mA	5
Average power supply current, refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RCMIN})	I_{CC3}		45		40		35	mA	5
Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{RC} = t_{RCMIN})	I_{CC4}		45		40		35	mA	5
Random read or write cycle time	t_{RC}	220		260		330		ns	6
Read-write cycle time	t_{RWC}	300		355		445		ns	6
Page mode cycle time	t_{PC}	120		145		180		ns	6
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	7,8
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	7,9
Output buffer turn-off delay	t_{OFF}	0	30	0	40	0	50	ns	10
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	4
$\overline{RAS}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	30	100	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	12
$\overline{CAS}$ precharge time, non-page cycles	t_{CPN}	25		25		30		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	60		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
ROW address set-up time	t_{ASR}	0		0		0		ns	
ROW address hold time	t_{RAH}	15		15		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		30		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	13
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	13
Write command hold time	t_{WCH}	35		45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		155		ns	
Write command pulse width	t_{WP}	35		45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	14
Data-in hold time	t_{DH}	35		45		55		ns	14
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		155		ns	
Refresh period	t_{REF}		2		2		2	ms	
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	95		120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	155		195		255		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40		50	ns	
Data delay time	t_{OED}	30		40		50		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay to $\overline{OE}$	t_{OEZ}	0	30	0	40	0	50	ns	

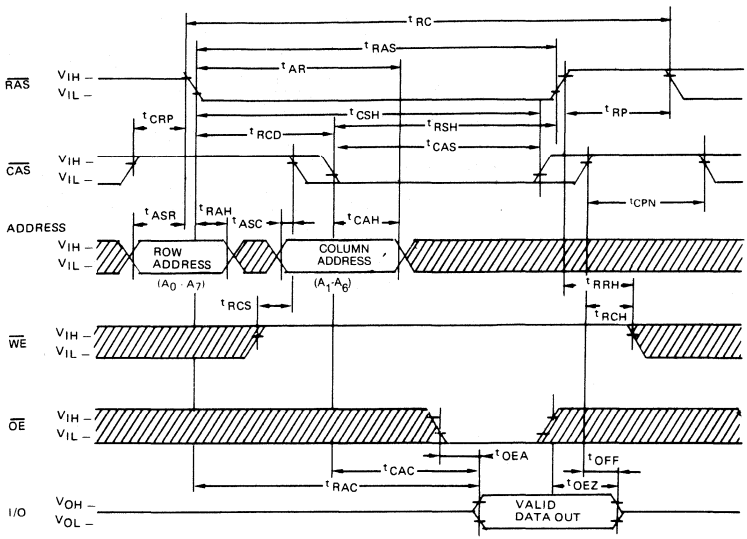
Notes:

1. All voltages referenced to GND.
2. An initial pause of 100 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
3. AC measurements assume $t_T = 5$ ns.
4. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. I_{CC1}, I_{CC3}, and I_{CC4}, depend on output loading and cycles rates. Specified values are obtained with the output open.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by any cycle.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

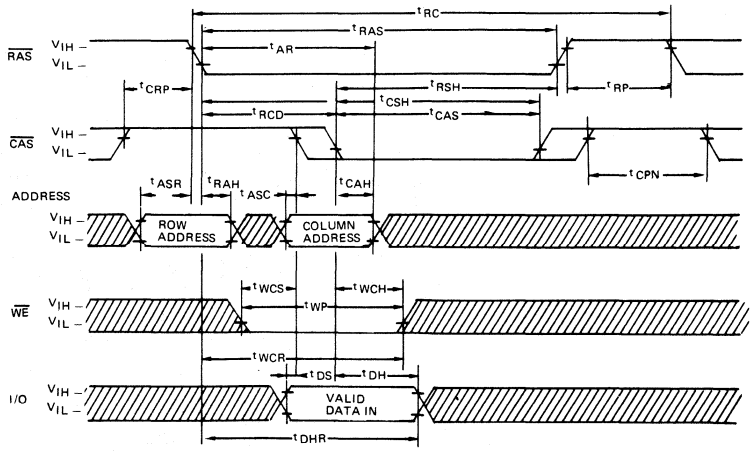
A.C. Electrical characteristics (0 °C ≦ Ta ≦70 °C) (V_{CC} = 5.0V ± 10%)

CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance (A_0-A_7)	C_{I1}		5	pF	
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}		8	pF	
Input/Output Capacitance, data ports	C_O		7	pF	

READ CYCLE

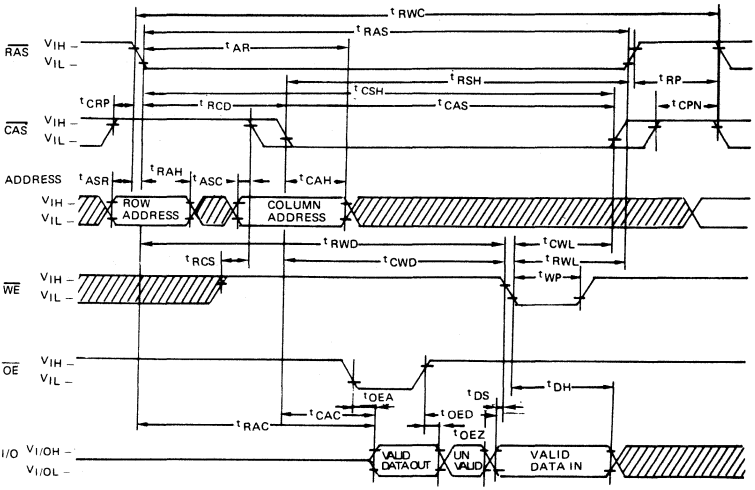


WRITE CYCLE (EARLY WRITE)

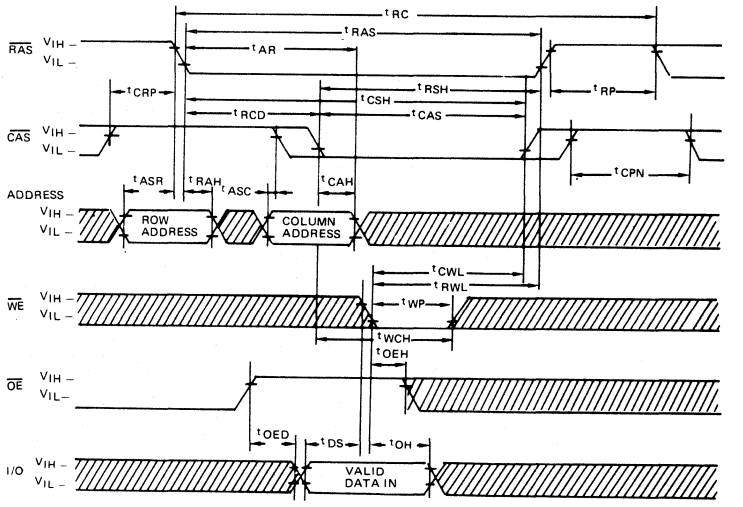


* $\overline{OE}$: Don't care

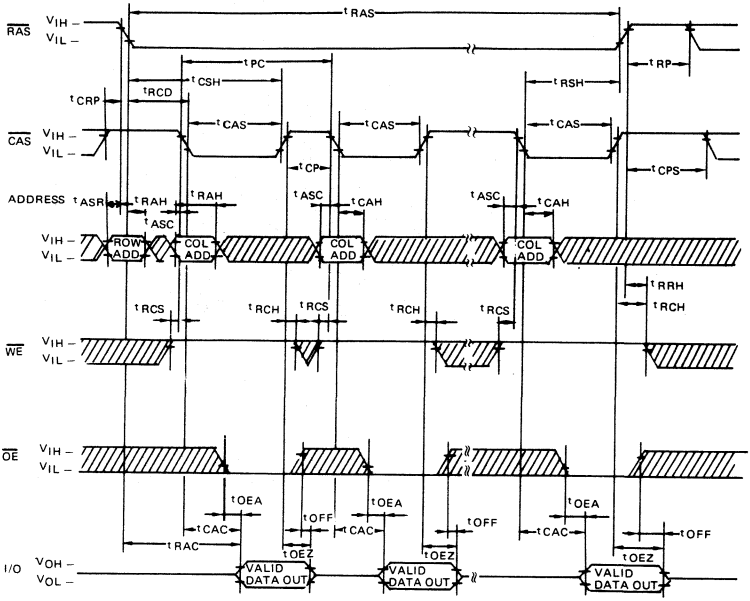
READ-WRITE/READ-MODIFY-WRITE CYCLE



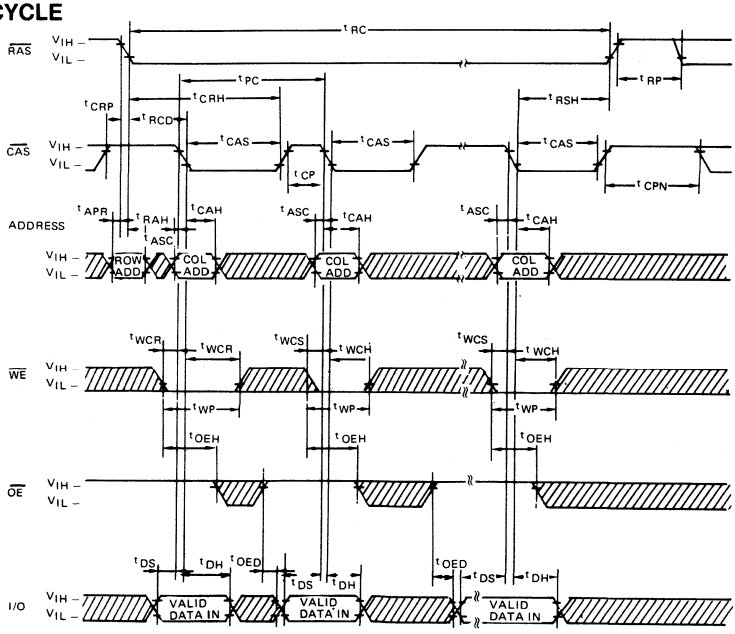
$\overline{OE}$ CONTROLLED WRITE CYCLE



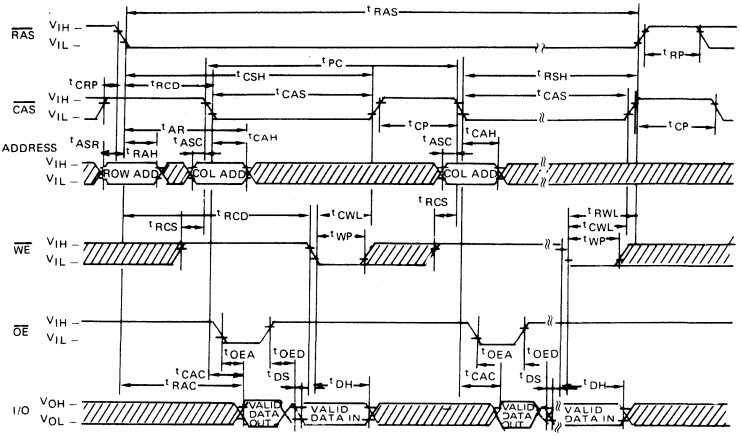
PAGE MODE READ CYCLE



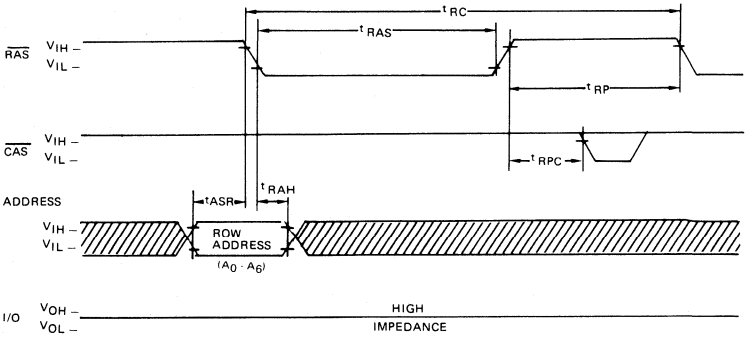
PAGE MODE WRITE CYCLE
(EARLY WRITE)



PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



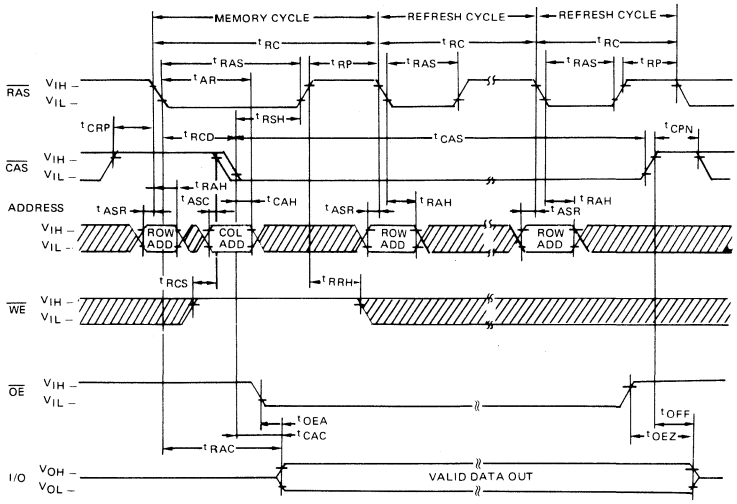
„RAS ONLY" REFRESH CYCLE



* $\overline{WE}$: Don't care

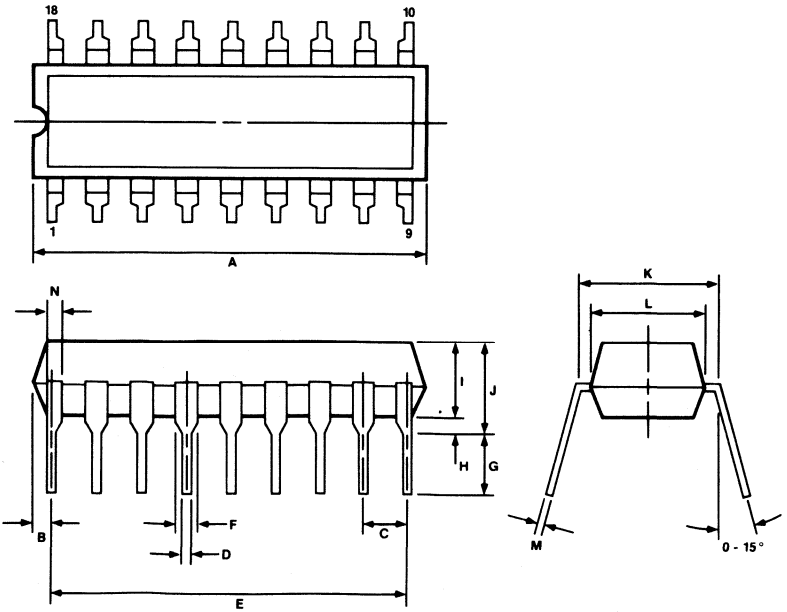
A_7 : V_{IH} or V_{IL}

HIDDEN REFRESH CYCLE



Package Dimensions
18 PIN Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.5 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	.25 $^{+.10}_{-.05}$
N	1.0 min



262.144 x 1-BIT DYNAMIC MOS RAM

DESCRIPTION

The NEC μPD 41256 is a 262.144-word by one-bit dynamic N-channel MOS RAM designed to operate from a single +5V power supply. The negative voltage substrate bias is generated internally providing automatic and transparent operation.

The μPD 41256 offers a direct upgrade from the 64K μPD 4164 achieveing a four-fold increase in bit density at the board level.

The μPD 41256 utilizes double poly layer N-channel silicon gate processing which provides for high storage cell density, high performance, and high reliability.

The μPD 41256 utilizes a single transistor dynamic storage cell and advanced dynamic circuitry throughout including the 1024 sense amplifiers, which ensures that power dissipation is minimized.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to the high impedance state by returning the $\overline{CAS}$ to the high state. Refresh is acccomplished on the 256 address combinations of A0-A7, during a 4-millisecond period.

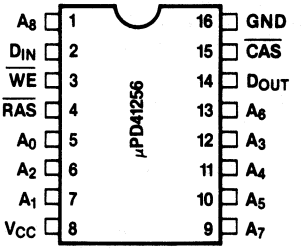
FEATURES

- ☐ 262,144 X 1-bit organization
- ☐ Multiplexed address inputs
- ☐ Non-Latched output is three-state, TTL-compatible
- ☐ On-chip substrate bias generator
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 256 refresh cycles (A0-A7 pins for refresh address)/4ms
- ☐ Read, write, read-write, read-modify-write, $\overline{RAS}$-only-refresh, and page mode capability
- ☐ Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode (Note 16)
- ☐ 3 performance ranges:
- ☐ Single +5V, ±10% power supply
- ☐ Low power dissipation; 28mW standby (max.)
- ☐ 16 Pin plastic (41256C) and hermetic (41256D) DIP Packages
- ☐ 18 Pin PLCC (41256L)
- ☐ 16 Pin ZIP (41256V)

Device	Access Time	R/W Cycle	RW Cycle	Power dissipation (max.)
μPD 41256-10	100 ns	200 ns	240 ns	457 mW
μPD 41256-12	120 ns	220 ns	265 ns	457 mW
μPD 41256-15	150ns	260 ns	310 ns	385 mW

PIN Configuration DIP (Dual-in-line Package)

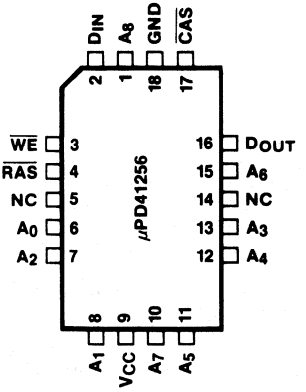
μPD41256C/D



A_0~A_8	:	ADDRESS INPUTS
$\overline{RAS}$	:	ROW ADDRESS STROBE
$\overline{CAS}$	:	COLUMN ADDRESS STROBE
$\overline{WE}$	:	WRITE ENABLE
D_{IN}	:	DATA INPUT
D_{OUT}	:	DATA OUTPUT
V_{CC}	:	POWER SUPPLY (+5.0 V)
GND	:	GROUND
NC	:	NO CONNECTION

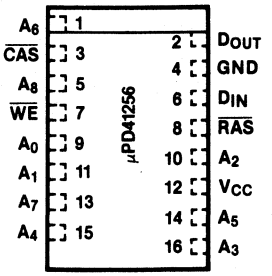
PIN Configuration PLCC (Plastic Leaded Chip Carrier)

μPD41256L



PIN Configuration ZIP (Zig-Zag-in-line Package)

μPD41256V



PIN IDENTIFICATION

Plastic/Hermetic DIP

No.	Symbol	Function
1, 5-7, 9-13	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable input
4	$\overline{RAS}$	Row address strobe
8	V_{CC}	+5 V power supply input
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe input
16	GND	Ground

Plastic PLCC

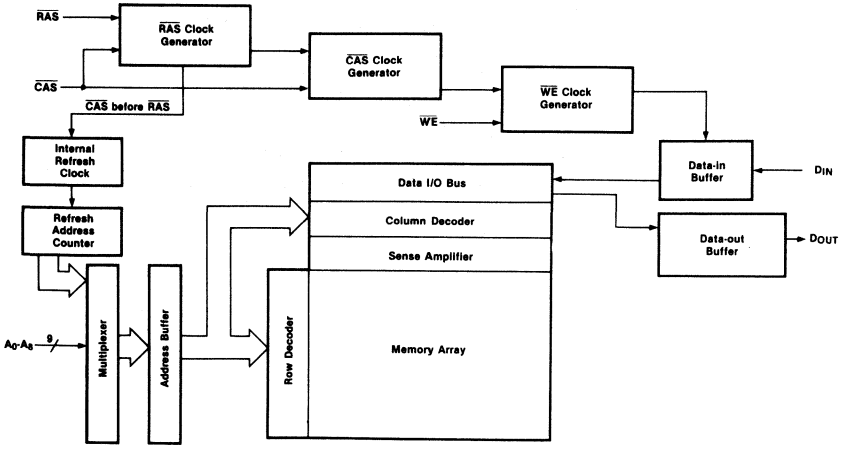
No.	Symbol	Function
1, 6-8 10-13, 15	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable input
4	$\overline{RAS}$	Row address strobe
5, 14	NC	No connection
9	V_{CC}	+5 V power supply input
16	D_{OUT}	Data output
17	$\overline{CAS}$	Column address strobe input
18	GND	Ground

PIN IDENTIFICATION

Plastic ZIP

No.	Symbol	Function
1, 5, 9-11 13-16	A_0-A_8	Address inputs
2	D_{OUT}	Data output
3	$\overline{CAS}$	Column address strobe input
4	GND	Ground
6	D_{IN}	Data input
7	$\overline{WE}$	Write enable input
8	$\overline{RAS}$	Row address strobe
12	V_{CC}	+5 V power supply input

Block Diagram



ABSOLUTE MAX. RATINGS*

Voltage on any pin relative to GND	-1.0 to + 7.0 V
Operating temperature, Ta (Ambient)	0 to + 70° C
Storage temperature, Tstg (Ambient)	-55 to + 150° C (ceramic) -55 to + 125° C (plastic)
Short circuit output current	50 mA
Power dissipation	1 W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≦ Ta ≦ 70°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{CC} GND	4.5 0	5.0 0	5.5 0	V V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4		5.5	V	
Input Low (Logic o) Voltage, all inputs	V_{IL}	-1.0		0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C ≦ Ta ≦ 70°C) (V_{CC} = 5.0 V ± 10 %)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNITS	NOTES
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)	I_{CC2}		5	mA	
INPUT LEAKAGE Input leakage current, any input (0V ≦ V_{IN} ≦ V_{CC} all other pins not under test = 0 volts)	$I_{I(L)}$	-10	10	μA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≦ V_{OUT} ≦ ± 5.5 V)	$I_{O(L)}$	-10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5 mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

PARAMETER	Symbol	μPD41256-10		μPD41256-12		μPD4125-15		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RCMIN})	I_{CC1}		83		83		70	mA	5
Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RCMIN})	I_{CC3}		65		65		55	mA	5
Average power supply current page mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{RC} = t_{PCMIN})	I_{CC4}		60		60		55	mA	5
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RCMIN})	I_{CC5}		65		65		60	mA	5
Random read or write cycle time	t_{RC}	200		220		260		ns	6
Read-write cycle time	t_{RWC}	240		265		310		ns	6
Page mode cycle time	t_{PC}	100		120		145		ns	6
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	7,8
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	7,9
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	35	ns	10
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	4
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	1000	120	1000	150	1000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	1000	60	1000	75	1000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	12
$\overline{CAS}$ precharge time, non-page cycles	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time page cycle	t_{CP}	40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
ROW address set-up time	t_{ASR}	0		0		0		ns	
ROW address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		20		20		ns	13
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	13
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	14
Data-in hold time	t_{DH}	25		30		40		ns	14
Data-in hold time referenced $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Refresh period	t_{REF}		4		4		4	ms	
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50		60		75		ns	15
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100		120		150		ns	15
$\overline{CAS}$ set-up time for CBR refresh	t_{CSR}	10		10		10		ns	16
$\overline{CAS}$ hold time for CBR refresh	t_{CHR}	20		30		30		ns	16

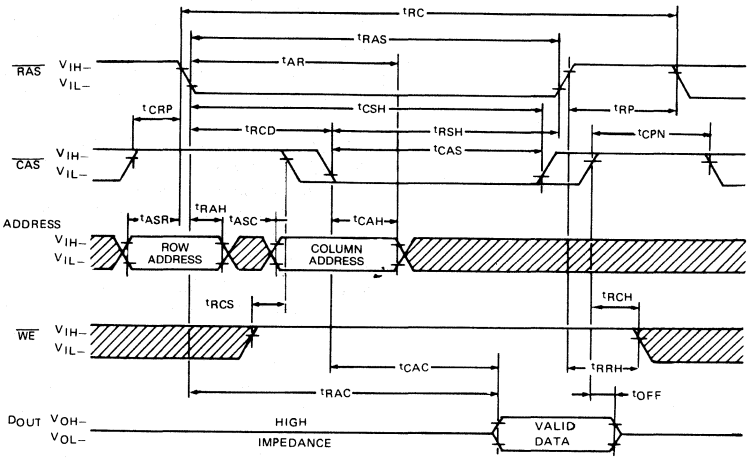
NOTES:

1. All voltages referenced to GND.
2. An initial pause of 100 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
3. AC measurements assume $t_T = 5$ ns.
4. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with output open.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (Ta = 0 to 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by any cycle.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. K, E, P process code products have no $\overline{CAS}$-Before-$\overline{RAS}$ Refresh function. On K, E, P process code products, the external address is required in Hidden Refresh cycle and the address signal must be met t_{ASR}, t_{RAH} which are specified from $\overline{RAS}$ falling edge.
17. Applies for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

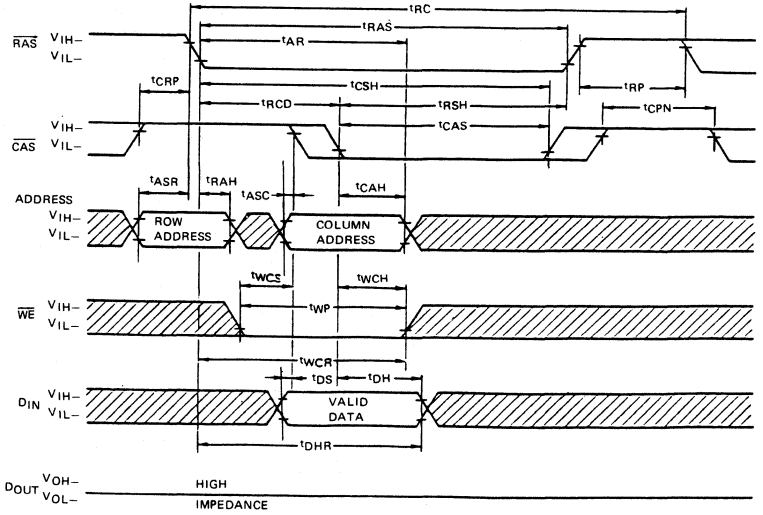
A.C. Electrical characteristics (0°C ≦ Ta ≦70°C) (V_{CC} = 5.0V ± 10%)

CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance ($A_0 \sim A_8$, D_{IN})	C_{I1}		5	pF	
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}		8	pF	
Output Capacitance (D_{OUT})	C_O		7	pF	

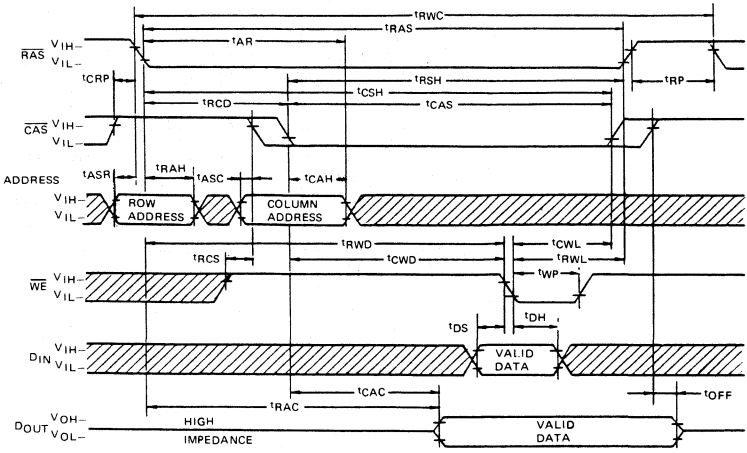
READ CYCLE



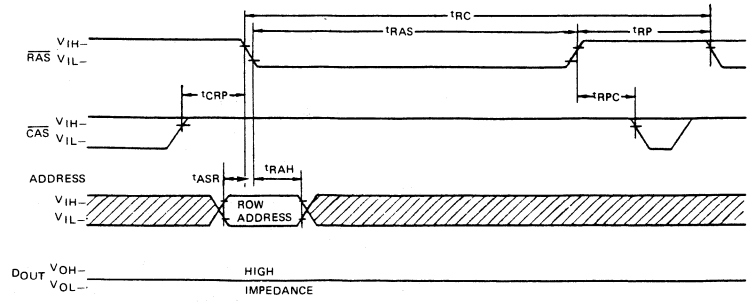
WRITE-CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

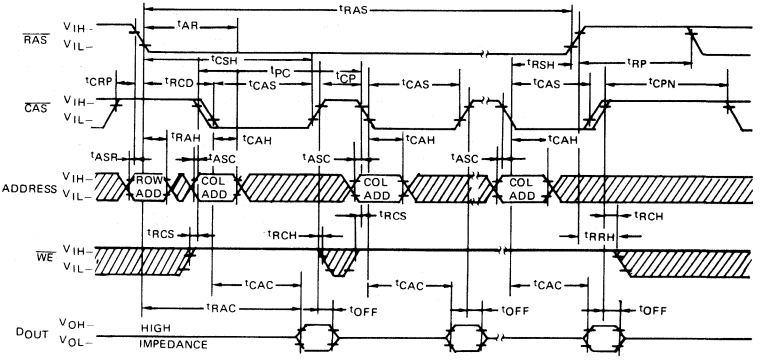


„RAS-ONLY" REFRESH CYCLE

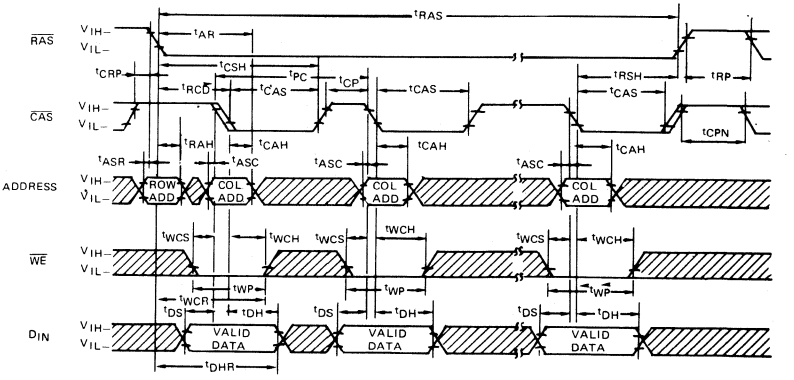


$\overline{WE}$ = DON'T CARE

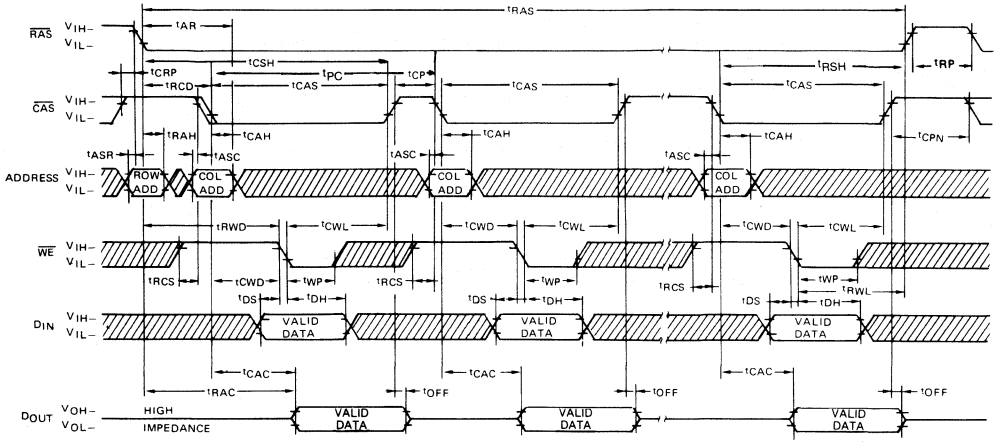
PAGE MODE READ CYCLE



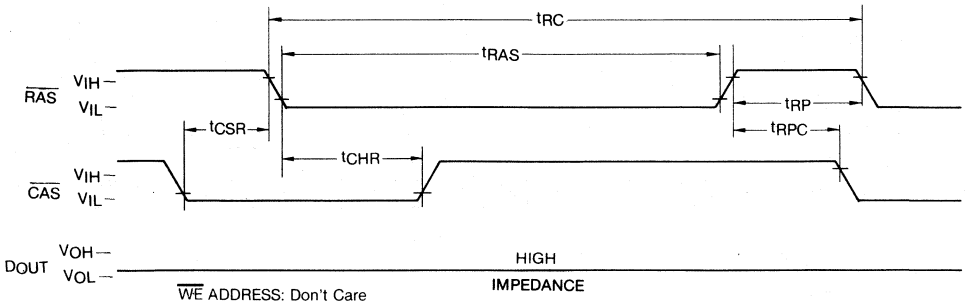
PAGE MODE WRITE CYCLE
(EARLY WRITE)



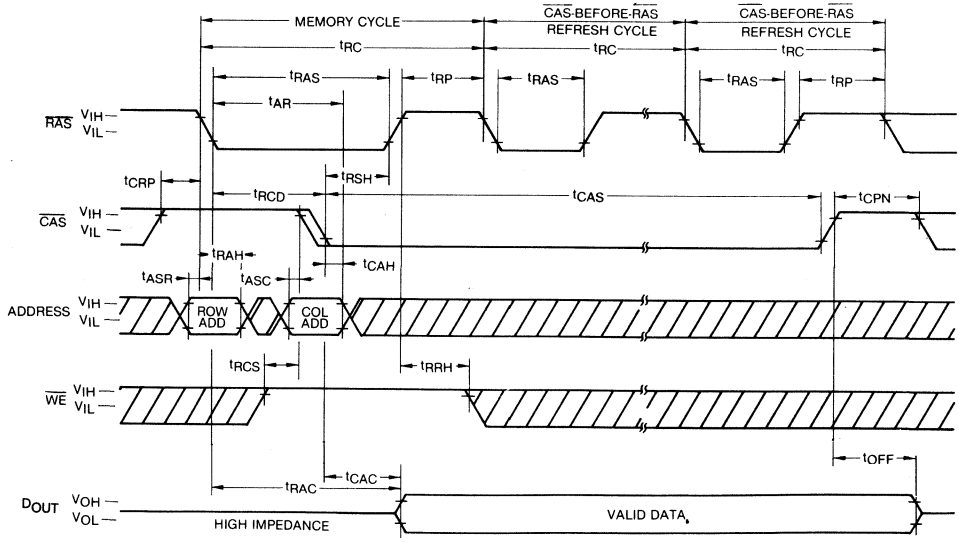
PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



$\overline{CAS}$ Before $\overline{RAS}$ REFRESH Cycle

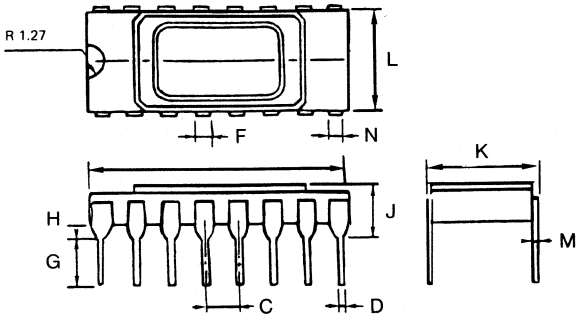


HIDDEN REFRESH CYCLE



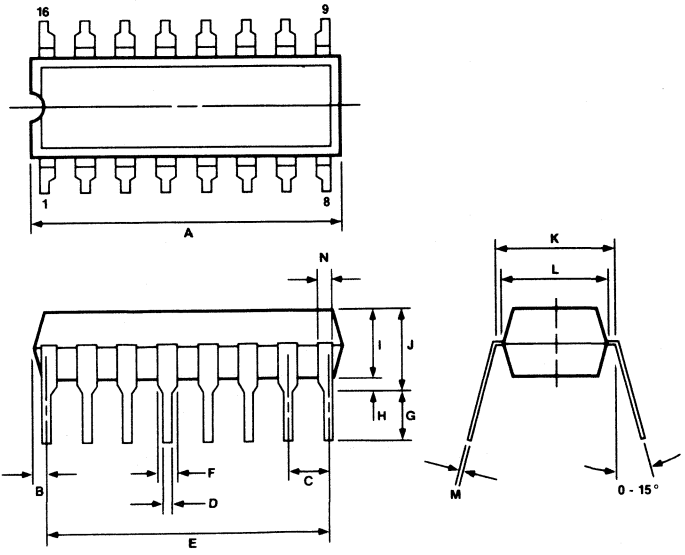
Package Dimensions
Ceramic DIP

Item	Millimeters
A	20.5 max.
B	–
C	2.54(TP)
D	.05±.10
E	–
F	1.35
G	2.54 min.
H	0.5 min.
I	–
J	5.08 max
K	7.62(TP)
L	7.3
M	$0.25^{+0.10}_{-0.05}$
N	1.1



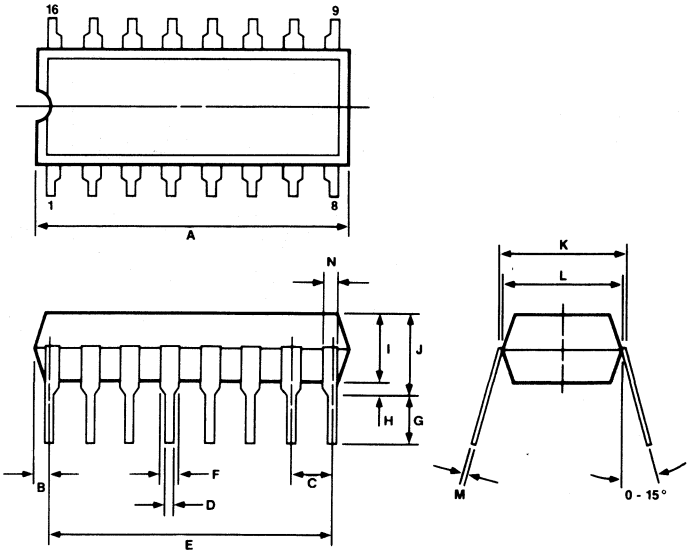
Plastic DIP (Semiwide Body)

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.7
M	$.25^{+.10}_{-.05}$
N	1.0 min



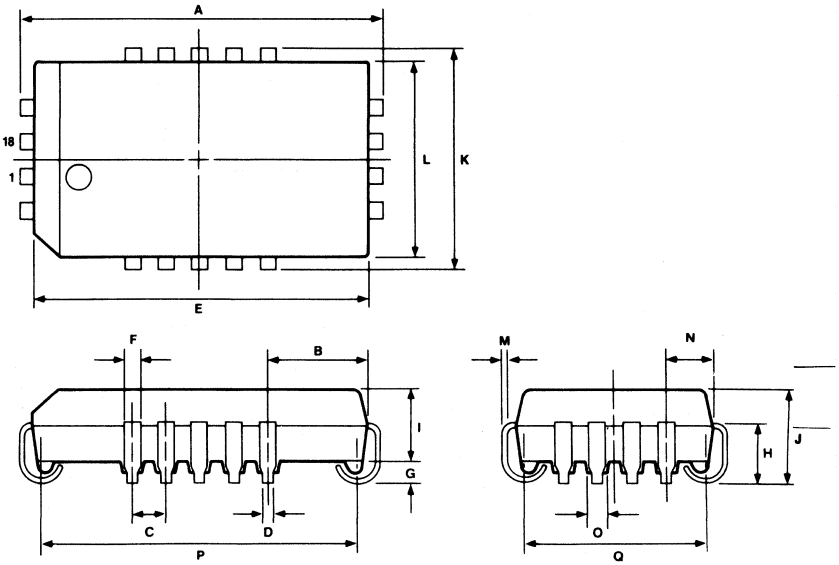
Plastic DIP (Wide Body)

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



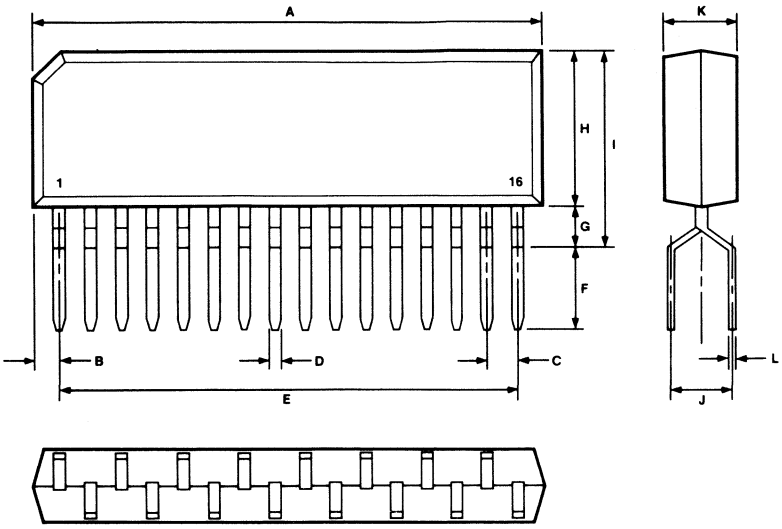
PLCC

Item	Millimeters
A	13.4 ± .20
B	3.71 ± .15
C	1.27
D	.40 ± .10
E	12.5
F	.60
G	.8 min
H	2.40 ± .20
I	2.6
J	3.50 ± .20
K	8.30 ± .20
L	7.40
M	$.20^{+.10}_{-.05}$
N	1.80 ± .20
O	.70
P	11.68 ± .20
Q	6.6 ± .20



ZIP

Item	Millimeters
A	21.59 max
B	1.27 max
C	1.27 [TP]
D	.50 ± .10
E	19.05
F	3.5 ± .3
G	.9 min
H	6.6
I	8.3 max
J	2.54 [TP]
K	2.8 ± .2
L	$.25^{+.10}_{-.05}$



Introduction

In parallel with the increased integration of ICs and LSIs, including memory LSIs, the continuing trends towards smaller, more compact electronic device geometry are rapid and extensive. In recent years, smaller package geometry has made possible electronic devices that are more intelligent and more compact. The development of smaller packages for dynamic RAMs is now seen as essential to making available more intelligent, more compact electronic devices using these RAMs.
NEC has developed a 256K bit dynamic RAM using an 18-pin plastic leaded chip carrier (PLCC) to address this need.
This paper provides introductory information on this new product, including its features and mounting methods.

1. Description
2. Features
3. Mounting Methods
4. Packing Specifications
5. Reliability Test Data

1. Description

The μPD41256L is a dynamic RAM organized as 256K-word by 1-bit, and has the same electrical characteristics as the previously available plastic DIP μPD41256C. Table 1 summarizes principal characteristics of the μPD41256L family.

Table 1 Principal Characteristics

Device Name	Access Time (Max.)	R/W Cycle Time (Min.)	RW Cycle Time (Min.)	Power Dissipation (Max.)
μPD41256L-10	100 ns	200 ns	240 ns	457 mW
μPD41256L-12	120 ns	220 ns	265 ns	457 mW
μPD41256L-15	150 ns	260 ns	310 ns	385 mW

The leads are arranged in four directions at 50 mil (1.27 mm) pitches. All are bent in a J-shape on the bottom of the package.
Fig. 1 is the pin configuration of μPD41256L; Fig. 2 is the package dimension of the 18-pin PLCC; and Fig. 3 gives the recommended mount pad dimension.

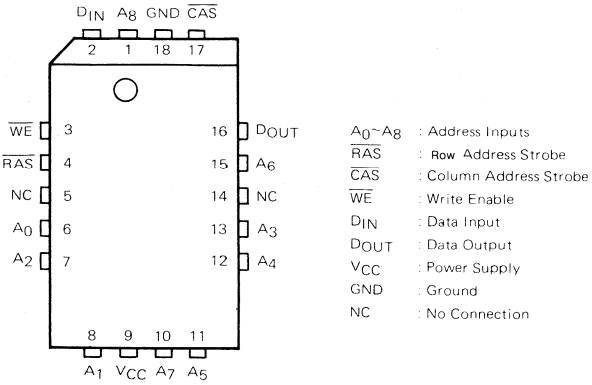


Fig. 1 Pin Configuration

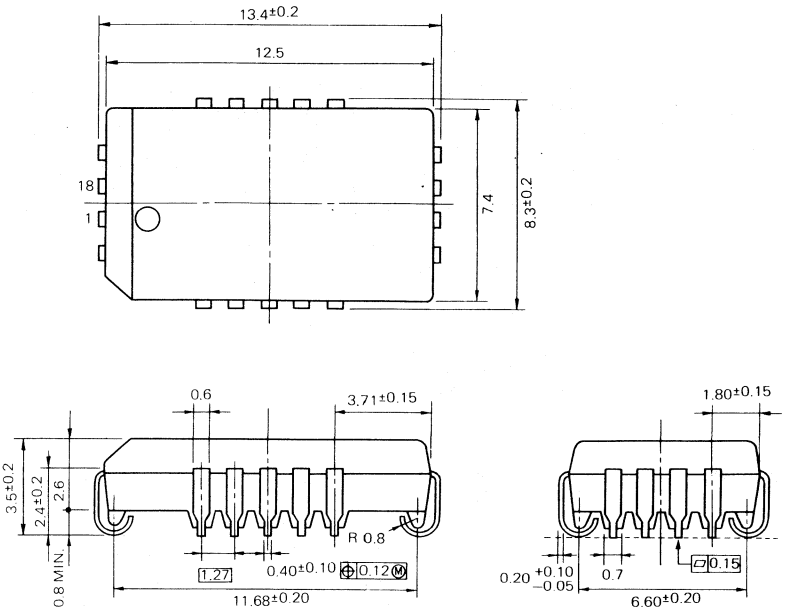


Fig. 2 Package Dimension (Unit: mm)

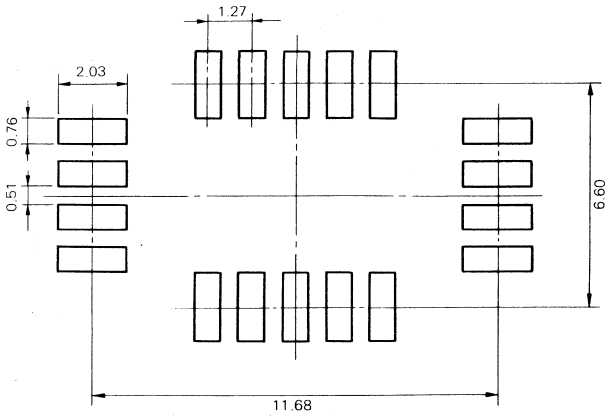


Fig. 3 Recommended Mount Pad Dimension (Unit: mm)

2. Features

The most outstanding feature of the PLCC is its suitability for high-density integration. Fig. 4 shows a DIP and PLCC area comparison.

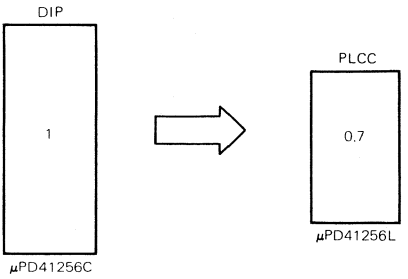


Fig. 4 DIP and PLCC Area Comparison

The area ration of DIP/PLCC is 1/0.7. PLCC mounting thus increases packing density by about 30%. A further increase in packing density is expected with double-sided mounting.
In addition, the PLCC offers the following features:

(1) The leads, bent in a J-shape on the package plastic side, are hard to deform and easy to handle when compared with the DIP and mini-flat package.
(2) Surface mounting eliminates the need for packing through-holes, with resultant cuts in board costs.
(3) The copper lead frame provides an equivalent thermal resistance of the μPD41256C 16-pin plastic DIP as shown in Fig. 5.
(4) A broad range of printed wiring materials can be selected in the copper lead frame since it can accommodate thermal stress during soldering.

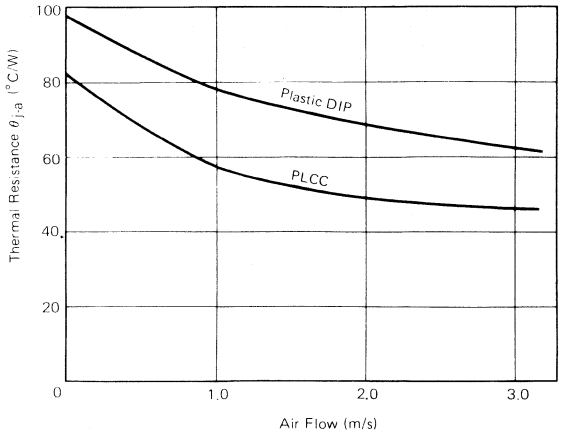


Fig. 5 Thermal Resistance

3. Mounting Methods

The surface mounting installation of the PLCC calls for a special notice on the mounting methods. Fig. 6 shows the standard flow of PLCC mounting.

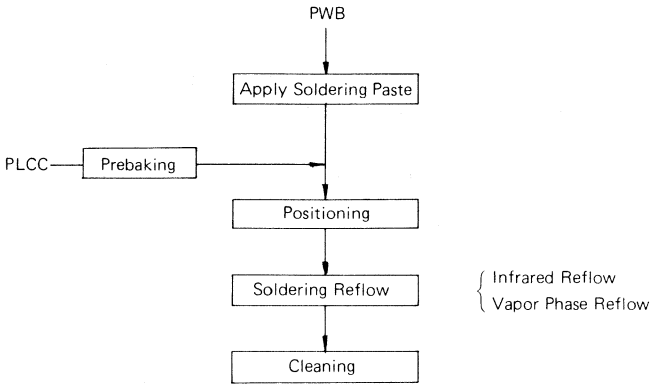


Fig. 6 Mounting Flowchart

Glass epoxy is typically used as the PLCC wiring board. A Sn-Pb alloy soldering paste (Sn – 63%, Pb – 37%) is commonly used with a resin flux. Use of soldering pastes having high melting points and flux with a lot of chlorine should be avoided because they could have an adverse effect on mounting performance.

Soldering is done in a reflow atmosphere. During reflow, the IC should be protected against unnecessary thermal stress, because excessive thermal stress could cause cracks in the package.
Two methods of soldering reflow are currently in widespread use: infrared reflow and vapor phase reflow. Fig. 7 shows the temperature profile of a typical infrared reflow. Fig. 8 shows the temperature profile of a vapor phase reflow.

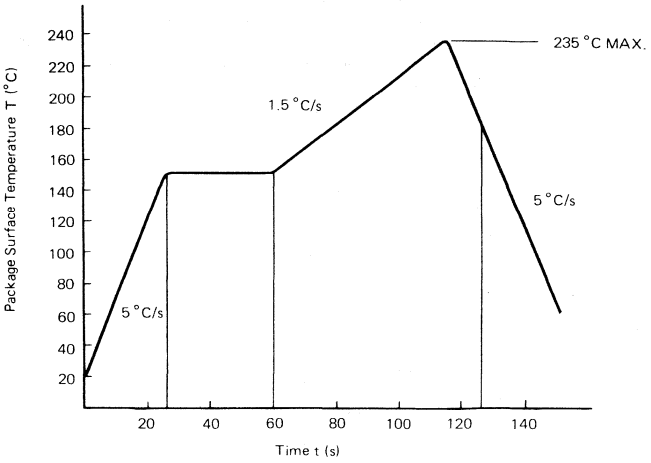


Fig. 7 Infrared Reflow Temperature Profile

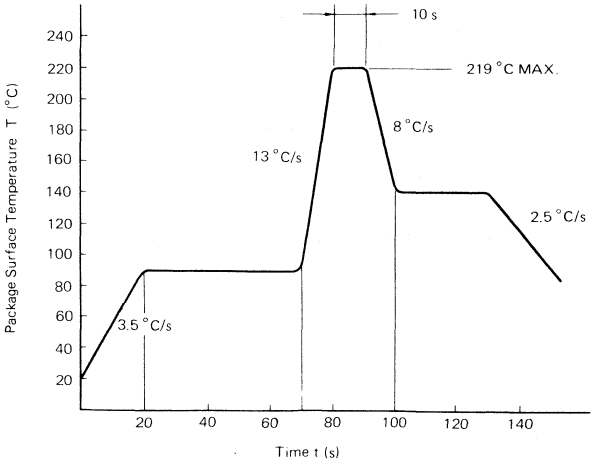
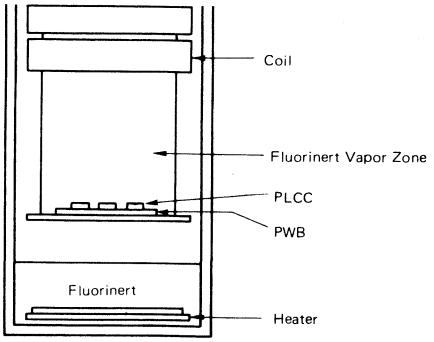
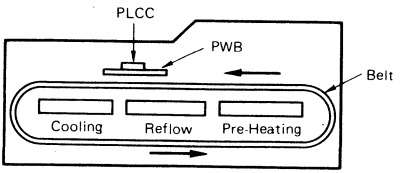


Fig. 8 Vapor Phase Reflow Temperature Profile

Vapor phase reflow is a technique of soldering reflow utilizing the vaporization latent heat of a special organic solvent. In operation, a saturated vapor layer is formed using a fluorine solvent, and a print wiring board (PWB) is inserted in this vapor layer to perform soldering reflow with evaporation latent heat. (Fluorinert (boiling point 215°C, 3M product) is commonly used as a fluorine solvent.) Fig. 9 is a schematic of the vapor phase reflow device.



(a) Batch Type



(b) Belt Type

Fig. 9 Vapor Phase Reflow Device Schematic

Table 2 compares the infrared reflow and vapor phase reflow operations.

Table 2 Infrared Reflow and Vapor Phase Reflow Comparisons

	Infrared Reflow	Vapor Phase Reflow
Advantages	● Wide temperature setting range ● Low running cost	● Precise temperature control ● Freedom from site-dependent temperature variations ● Soldering in an inactive atmosphere prevents oxidation of lead electrodes
Disadvantages	● Infrared absorption efficiency varies from site to site on the board, causing local temperature differences. ● Lead electrodes are oxidized	● Device expense ● High running cost (costly organic solvents) ● Ventilation

In cleaning, flux residues, fused soldering balls, etc. must be completely removed. Use of freon, diphron, or isopropyl alcohol is recommended as a resin flux cleaning solution.
The PLCC, which is smaller in geometry than DIP and which uses plastic sealing materials, requires special protection against moisture. After cleaning, allow the PLCC to dry fully. Store it with care to assure minimum moisture absorption.
NEC recommends prebaking the PLCC before mounting it on a PWB. Prebaking means to allow the PLCC to stand for 4–16 hours at a temperature of 125°C.

4. Packing Specifications

The μPD41256L is shipped in a 35-piece magazine case. Fig. 10 shows the case dimensions.
(1) Material
Polyvinyl chloride (PVC), anti-static
(2) Marking
'CAUTION-ELECTROSTATIC SENSITIVE DEVICES'
(3) 35 pieces/case

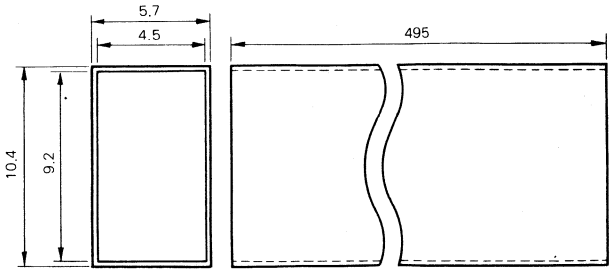


Fig. 10 18-pin PLCC Magazine Case (Unit: mm)

5. PLCC μPD41256L Reliability Test Data

Table 3,4 summarize the reliability data on the PLCC μPD41256L. Fig. 11, 12 show the circuit used to test it.
The results of testing were all found satisfactory, ensuring the equivalent reliability of the plastic DIPs.
Because the PLCC is a double-sided mounting package, it was subjected to thermal stress by at least two cycles of soldering reflow before HHBT. The results were found satisfactory as summarized in Table 4.

Table 3 μPD41256L Reliability Test Results (1)

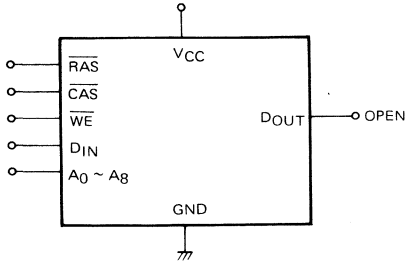
Test Item	Symbol	MIL-STD 883B	Test Condition	Sample Size	Test Results (No. of Failures)
High Temp. Dynamic Test	HTOL	1005 2	T_a = 125°C, V_{CC} = 5,5 V T_{cyc} = 2.6 μs Address Scan 0.1 Write (Fig. 11)	65	1000 h 0
High Temp. Storage Test	HTS	1008 1	T_a = 150°C	65	1000 h 0
Temp. Cycling	T/C	1010 C	− 65°C to + 150°C (30 min.) (30 min.)	40 24*	100CY 200CY 300CY 400CY 0 0 0 0 0 0 0 0

*These samples are mounted on PWB using infrared reflow at peak temperature 235°C before testing.

Table 4 μPD41256L Reliability Test Results (2)

Test Item	High Humidity Bias Test		Pressure Cooker Test	
Symbol	T/H		PCT	
Test Conditions	T_a = 85°C, RH = 85%, V_{CC} = 5.5 V (Fig. 12)		T_a = 125°C, RH = 100%	
Stress before Testing	Sample Size	Test Results (No. of Failures)	Sample Size	Test Results (No. of Failures)
−	−	−	70	96 h 192 h 0 0
V.P.S. 1 Time	25	1 000 h 0	25	360 h 0
V.P.S. 2 Times	50	1 000 h 0	50 70	96 h 192 h 360 h 0 0 0 0 0
V.P.S. 3 Times	25	1 000 h 0	25	360 h 0
After T/C 20 CY V.P.S. 2 Times	−	−	15	360 h 0
After H/H 72h V.P.S. 2 Times	25	1 000 h 0	−	−
After H/H 72h I.R.	39	1 000 h 0	36	360 h 0

Notes: V. P. S. . . . . Thermal stress by vapor phase reflow (Peak temperature 219° C).
I.R. . . . . Thermal stress by infrared reflow (Peak temperature 235° C).
T/C . . . . . Thermal stress by temperature cycling. (−65°C ~ +150° C).
H/H . . . . . Stress by high humidity storage (T_a= 85°C, RH = 85%).



Pin Names	V_{IH}	V_{IL}
$\overline{RAS}$	5.0 V	0.0 V
$\overline{CAS}$	5.0 V	0.0 V
$\overline{WE}$	–	0.0 V
D_{IN}	5.0 V	0.0 V
$A_0 \sim A_8$	5.0 V	0.0 V

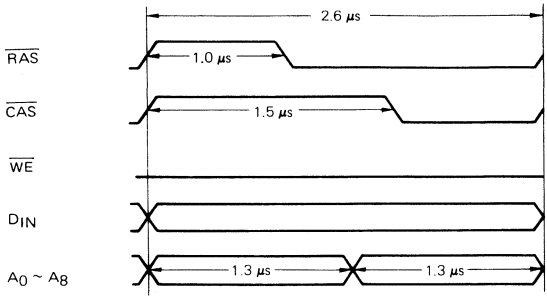


Fig. 11 HTOL Test Condition

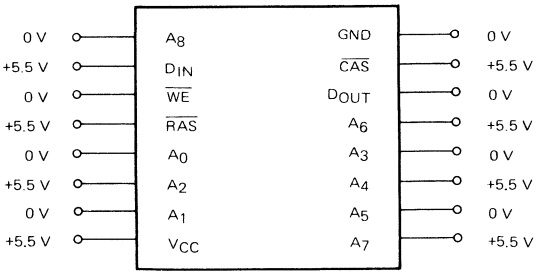


Fig. 12 T/H Test Condition

The preceding descriptions presented introductory information on the PLCC μPD41256L, including its features and mounting method. Though the PLCC requires certain care in mounting and storage, it is ideally suited for minituarizing electronic devices, and thus is expected to offer a growing range of applications.

262144 x 1-BIT DYNAMIC MOS RAM

DESCRIPTION

The NEC μPD41257 is a 262, 144-word by 1-bit dynamic N-channel MOS random-access memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally.
The μPD41257 utilizes double polylayer N-channel silicon gate processing which provides for high storage cell density, high performance, and high reliability.
The device also utilizes a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 1024 sense amplifiers, which ensures that power dissipation is minimized.
The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. The device is capable of nibble mode operation on either read or write cycles by cycling $\overline{CAS}$.
Refresh is accomplished by utilizing a $\overline{CAS}$ before $\overline{RAS}$ cycle that will enable the internal generation of the refresh address. Refresh can also be accomplished using $\overline{RAS}$-only refresh, hidden refresh, or normal read or write cycles on the 256 address combinations of A_0-A_7, during a 4 ms period.

FEATURES

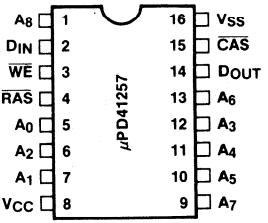
- ☐ 262, 144-word x 1 bit organization
- ☐ High density plastic DIP and PLCC packaging
- ☐ Multiplexed address inputs
- ☐ Single +5V ± 10% power supply
- ☐ Nibble mode on read or write or read-modify-write cycles
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Low power dissipation:
  - 28 mW max (standby)
  - 440 mW max (active, t_{RC} = 200 ns)
- ☐ Non-latched output, three-state, TTL-compatible
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 256-cycle, 4 ms refresh (A_0-A_7 pins for refresh address)

PERFORMANCE RANGES

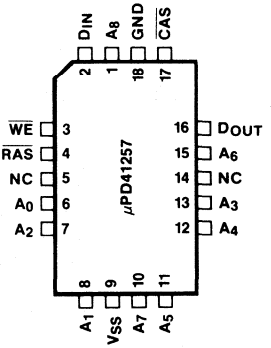
Device	Access Time	R/W Cycle	RMW Cycle
μPD41257-10	100 ns	200 ns	230 ns
μPD41257-12	120 ns	220 ns	265 ns
μPD41257-15	150 ns	260 ns	310 ns

PIN CONFIGURATIONS

Plastic DIP (μPD41257C)



Plastic Leaded Chip Carrier (PLCC) (μPD41257L)



PIN IDENTIFICATION

For DIP

No.	Symbol	Function
1, 5-7, 9-13	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
8	V_{CC}	Power supply (+5.0V)
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe
16	GND	Ground

For PLCC

No.	Symbol	Function
1, 6-8, 10-13, 15	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5, 14	NC	No connection
9	V_{CC}	Power supply (+5.0V)
16	D_{OUT}	Data output
17	$\overline{CAS}$	Column address strobe
18	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND	−1.0 to + 7.0 V
Operating temperature, T_A	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current	50 mA
Power Dissipation, P_D	1W

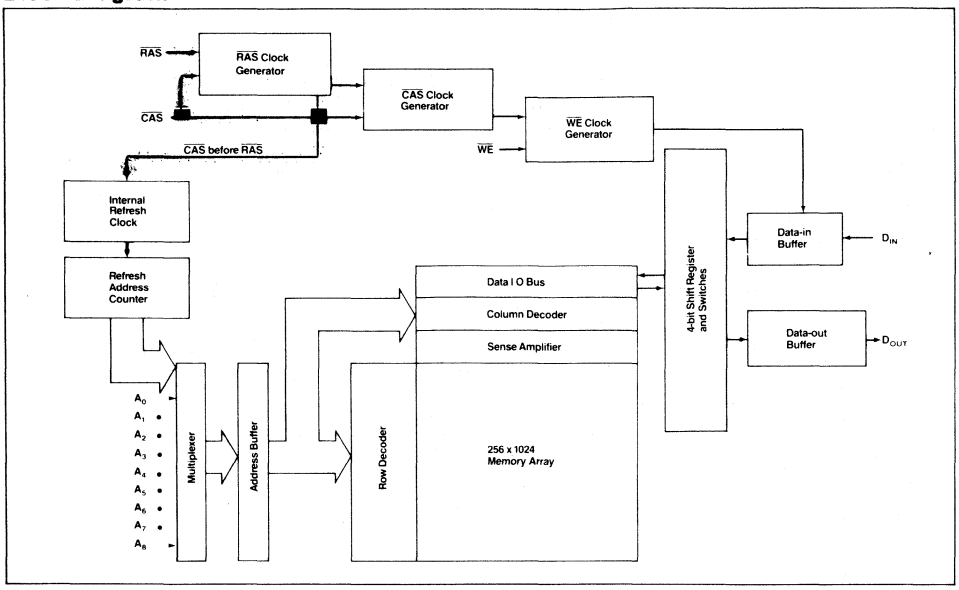
Comment: Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

$T_A = 0$ to + 70°C; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{I1}			5	pF	A_0-A_8, D_{IN}
Input capacitance	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O			7	pF	D_{OUT}

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%; GND = 0 V (Note 1,2)

Parameter	Symbol	Limits Min	Typ	Max	Test Unit	Conditions
Power supply standby current	I_{CC2}			5	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	Any input V_{IN} = 0 V to V_{CC}, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, V_{OUT} = 0 to 5.5 V
Output high (logic 1) voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA
Output low (logic 0) voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input high (logic 1) voltage, all inputs	V_{IH}	2.4		5.5	V	
Input low (logic 0) voltage, all inputs	V_{IL}	−1.0		0.8	V	

AC Characteristics

T_A = 0 to + 70°C; V_{CC} = 5.0 V ± 10% (Note 2, 3, 4)

Parameter	Symbol	Limits						Unit	Note
		μPD41257 -10		μPD41257 -12		μPD41257 -15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{RCMIN})	I_{CC1}		80		75		70	mA	5
Average power supply current, refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RCMIN})	I_{CC3}		65		60		55	mA	5
Random read or write cycle time	t_{RC}	200		220		260		ns	6
Read-write cycle time	t_{RWC}	230		265		310		ns	6
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	7.8
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	7.9
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	10
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{Ras}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	12
$\overline{CAS}$ precharge time	t_{CPN}	30		30		30		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
ROW address set-up time	t_{ASR}	0		0		0		ns	
ROW address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASH}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	13
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	13
Write command hold time	t_{WCH}	25		30		40		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits						Unit	Note
		μPD41257 -10		μPD41257 -12		μPD41257 -15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write command hold time referenced to $\overline{RAS}$	tWCR	75		90		115		ns	
Write command pulse width	tWP	15		20		25		ns	16
Write command to $\overline{RAS}$ lead time	tRWL	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	tCWL	35		40		45		ns	
Data-in set-up time	tDS	0		0		0		ns	14
Data-in hold time	tDH	25		30		40		ns	14
Data-in hold time referenced to $\overline{RAS}$	tDHR	75		90		115		ns	
Refresh period	tREF		4		4		4	ms	
$\overline{WE}$ command set-up time	tWCS	0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	50		60		75		ns	15
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	100		120		150		ns	15

Nibble Mode Operation

Parameter	Symbol	Limits						Unit	Note
		μPD41257 -10		μPD41257 -12		μPD41257 -15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Average power supply current, nibble mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, tNC = tNCmin)	ICC4		40		35		27	mA	5
Nibble mode cycle time	tNC	55		60		70		ns	
Nibble mode access time	tNAC		25		30		35	ns	7
Nibble mode precharge time	tNP	20		20		25		ns	
Nibble mode $\overline{CAS}$ Pulse width	tNAS	25		30		35		ns	
Nibble mode $\overline{RAS}$ hold time (Read)	tNRRSH	25		30		35		ns	
Nibble mode $\overline{RAS}$ hold time (Write)	tNWRSH	35		35		35		ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay	tNCWD	25		30		35		ns	
Nibble mode $\overline{WE}$ to $\overline{CAS}$ lead time	tNCWL	25		30		35		ns	
Nibble mode write command pulse width	tNWP	15		20		25		ns	
Random read or write cycle time (refresh counter test cycle)	tTRC	220		245		285		ns	17
Read-write cycle time (refresh counter test cycle)	tTRWC	260		290		335		ns	17
$\overline{CAS}$ precharge time (refresh counter test cycle)	tTCP	40		50		60		ns	17

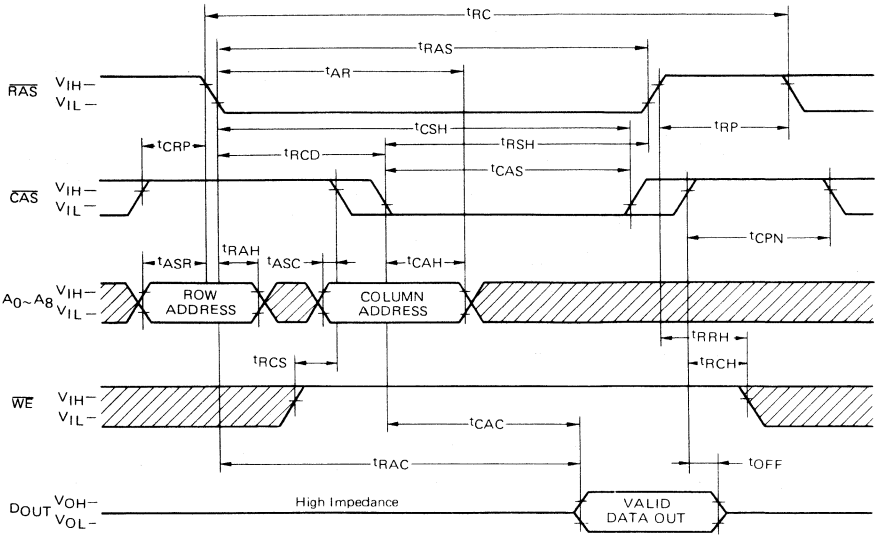
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Operation

Parameter	Symbol	Limits						Unit	Note
		μPD41257 -10		μPD41257 -12		μPD41257 -15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode ($\overline{RAS}$ cycling $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC}min)	I_{CC5}		70		65		60	mA	5
$\overline{CAS}$ set-up time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	

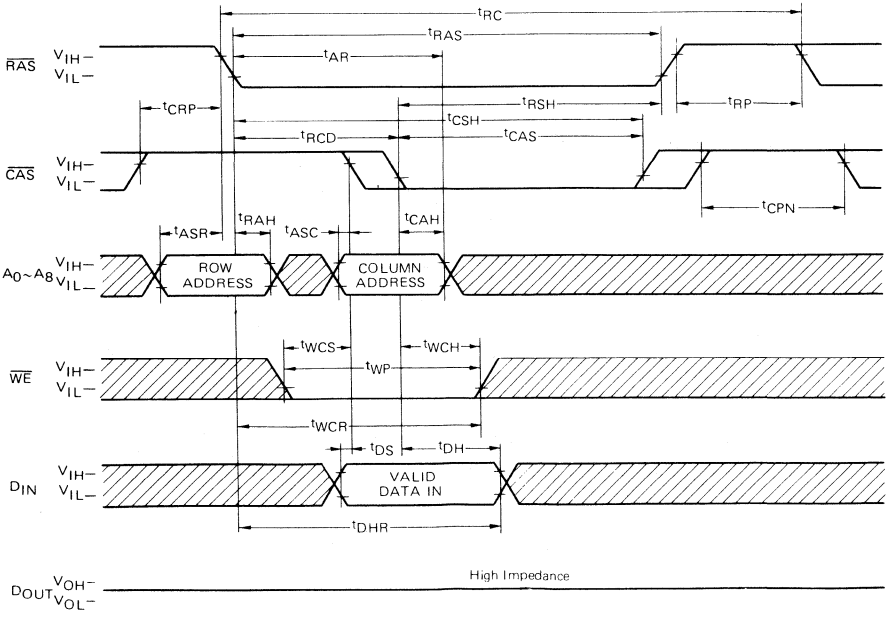
Notes:

1. All voltages referenced to GND.
2. An initial pause of 100 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
3. AC measurements assume t_T = 5 ns.
4. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. I_{CC1}, I_{CC3}, I_{CC5} and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (Ta = 0 to 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $r_{RCD} \leqq t_{RCD}$ (max.).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by any cycle.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. t_{WP} is applicable for delayed write cycle. If the cycle is early write, it should be satisfied value of t_{WCH}.
17. Applies for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

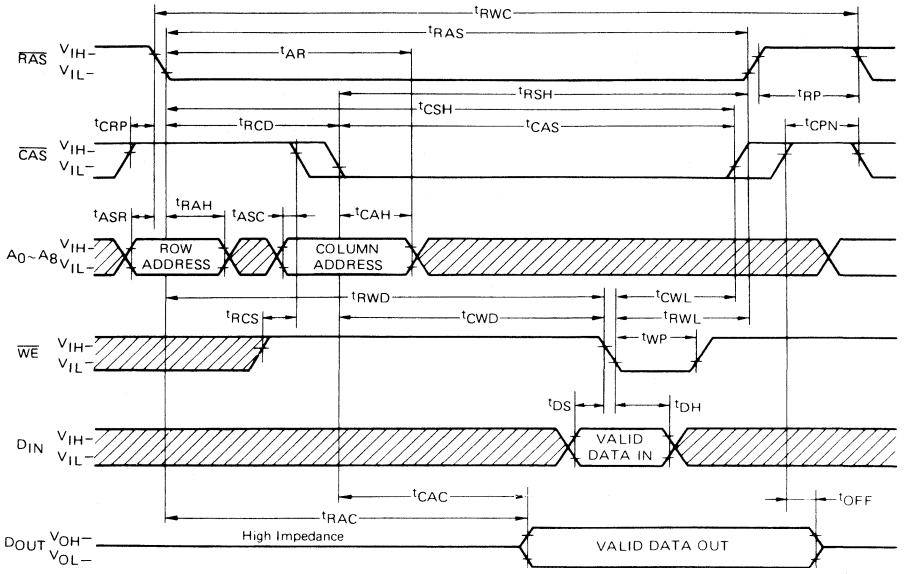
READ CYCLE



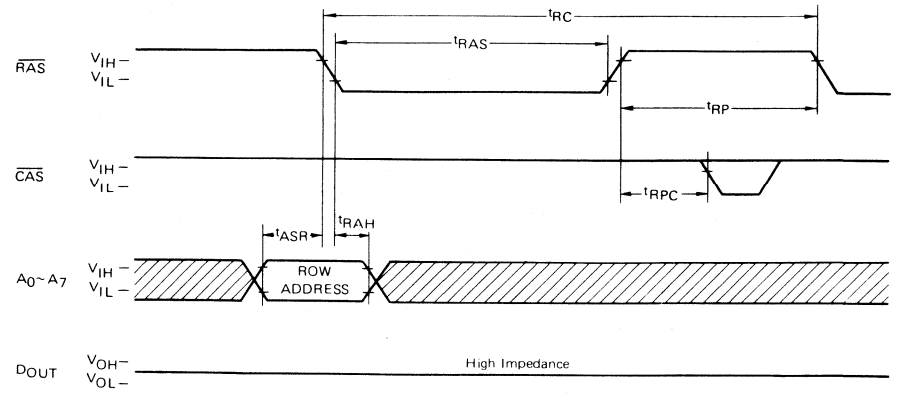
WRITE CYCLE (EARLY WRITE)



READ-WRITE / READ-MODIFY-WRITE CYCLE

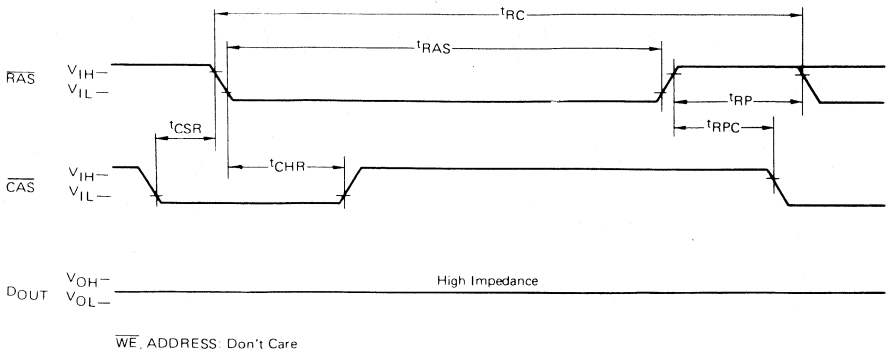


RAS ONLY" REFRESH CYCLE

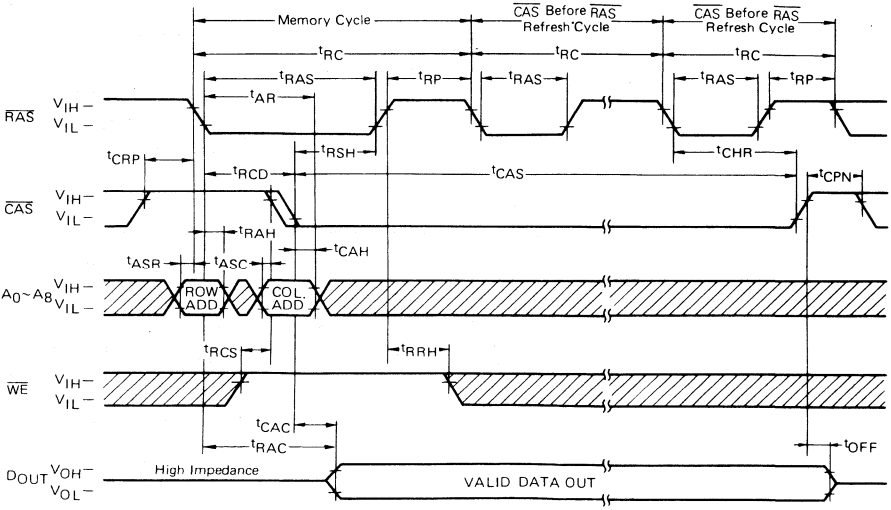


WE: Don't Care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE (CBR Cycle)



HIDDEN REFRESH CYCLE



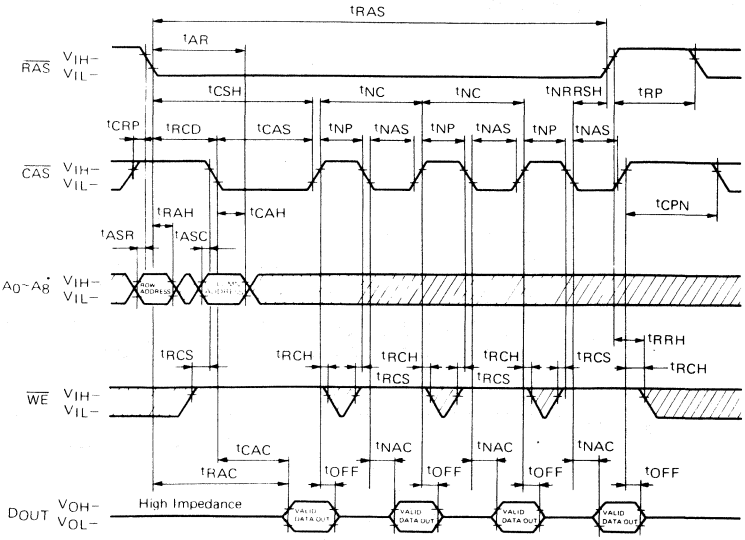
NIBBLE MODE OPERATION

μPD41257 is capable of performing a Nibble-mode operation on read, write or read-modify-write cycles. Nibble-mode operation allows high speed serial access of maximum 4 bits of data. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A8 and column address A8 in the following sequence.

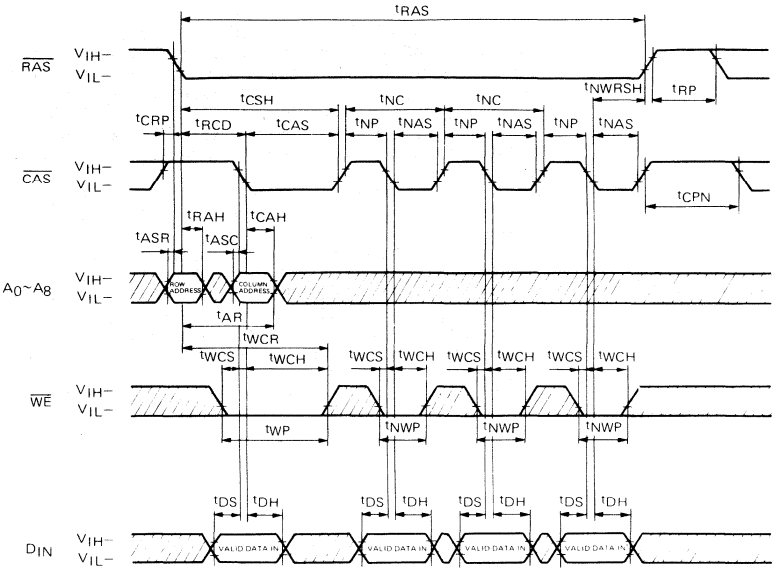
Sequence	Nibble Bit	Row Address								Column Address								Comment
		A8	A7	A6	A5	A4	A3	A2	A1	A0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
$\overline{RAS}/\overline{CAS}$	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	External address input
$\overline{CAS}$ cycling	2	1	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Repeated sequence

Fig. 1 Nibble Mode Address Sequence (Example)

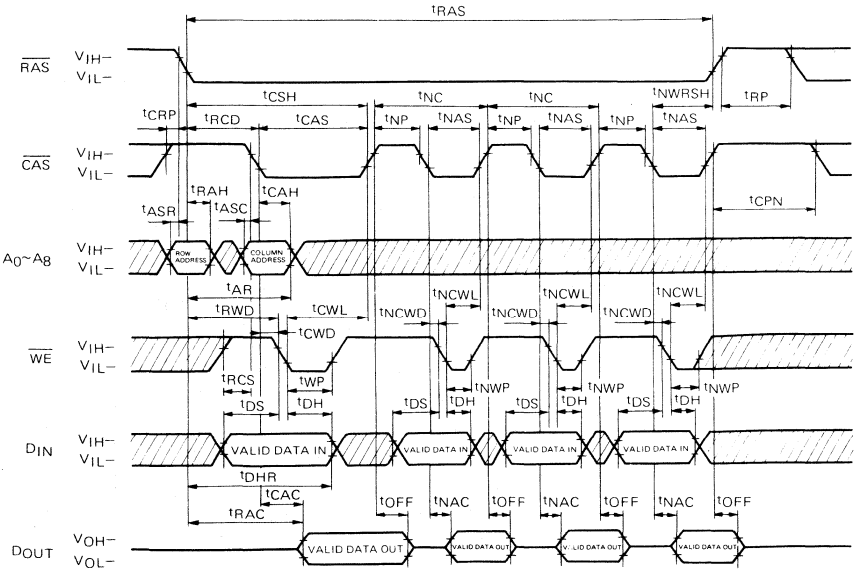
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-WRITE / READ-MODIFY-WRITE CYCLE



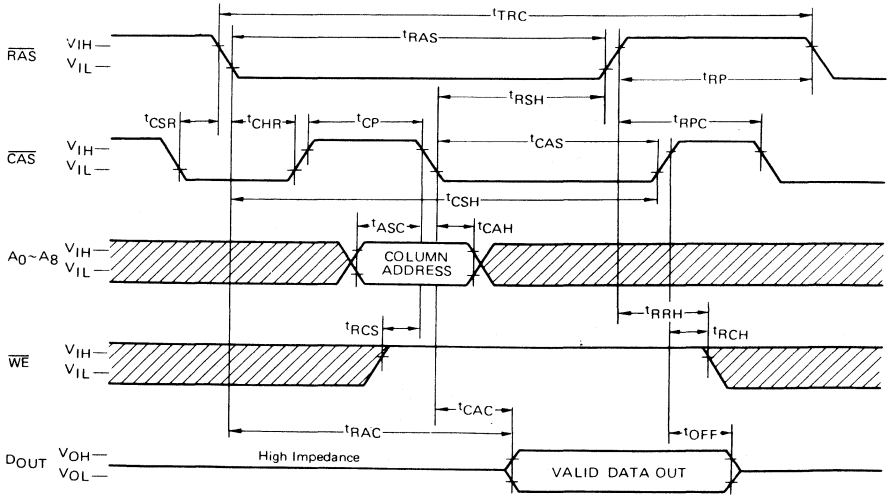
CAS BEFORE RAS REFRESH COUNTER TEST

Using CAS before RAS refresh counter test cycle, it provides a method of verifying the CAS before RAS refresh activated functionality. After CAS before RAS refresh operation, CAS goes to high level (with prescribed time: tCHR) and goes to low level (with prescribed time: tCP) while RAS is held low level, the read, write and read-modify-write operations are enabled. It's shown in CAS before RAS refresh counter test timing diagrams. A row address is defined by CAS before RAS refresh internal address counter, and a column address is defined by latching external address at the second falling edge of CAS.

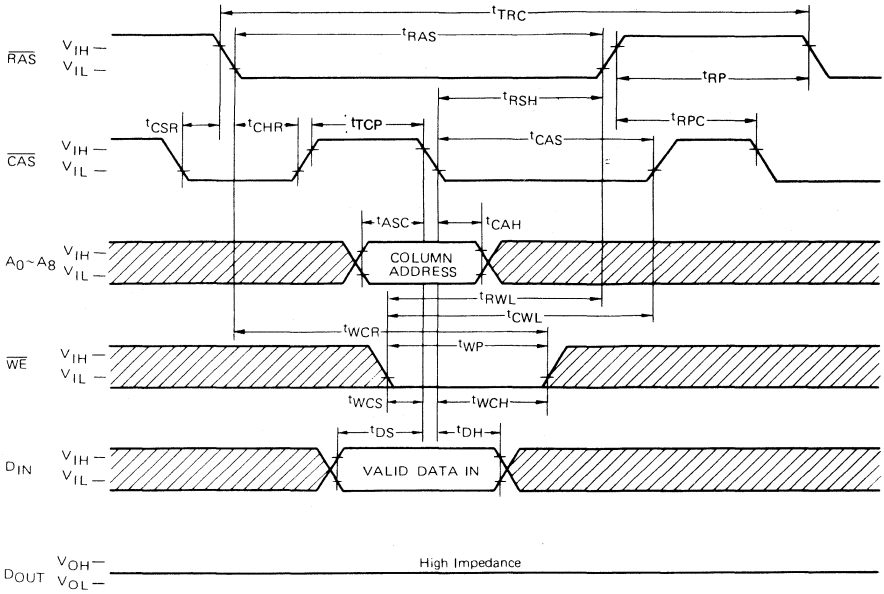
Suggested CAS before RAS refresh counter test pattern:

(1) Initialize the internal refresh counter. It's required 8 RAS only refresh cycles after power on for this operation.
(2) Write a test pattern of '0's into 256-memory cells at a fixed single column address using 256 times CAS before RAS refresh counter test write cycles.
(3) Using CAS before RAS refresh counter test read modify write cycle, read the '0' written at the last cycles (operation (2)), and write a new '1' in the same cycle. This is repeated 256 times and pattern '1's are written into the 256 memory cells.
(4) Read the '1' written in the last cycles (operation (3)), using CAS before RAS refresh counter test read cycle.
(5) Complement the test pattern and repeat the operation (2), (3), (4).

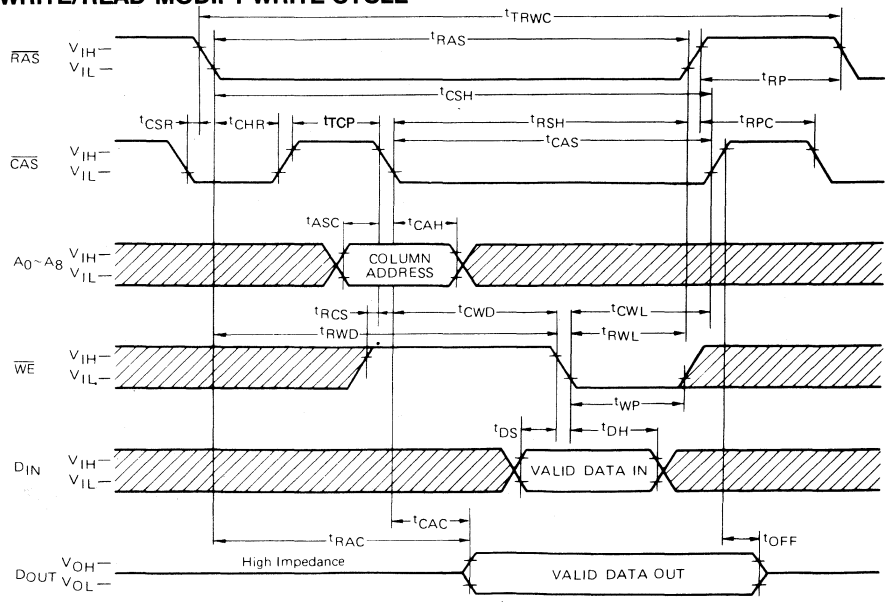
CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



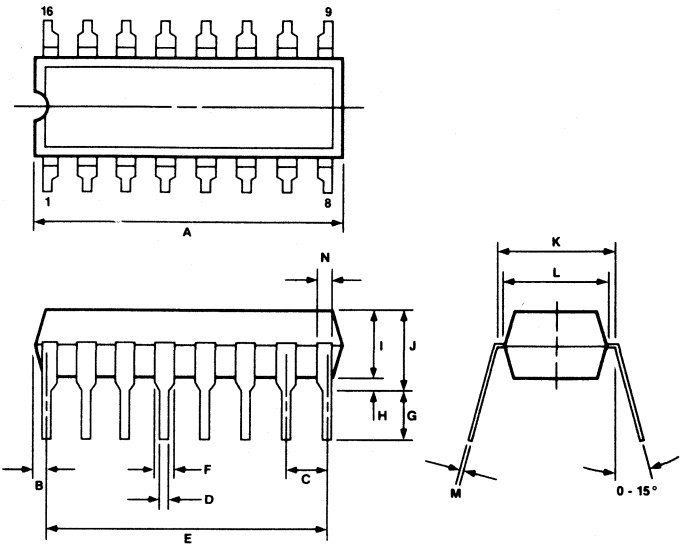
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-WRITE/READ-MODIFY-WRITE CYCLE



PACKAGE DIMENSIONS

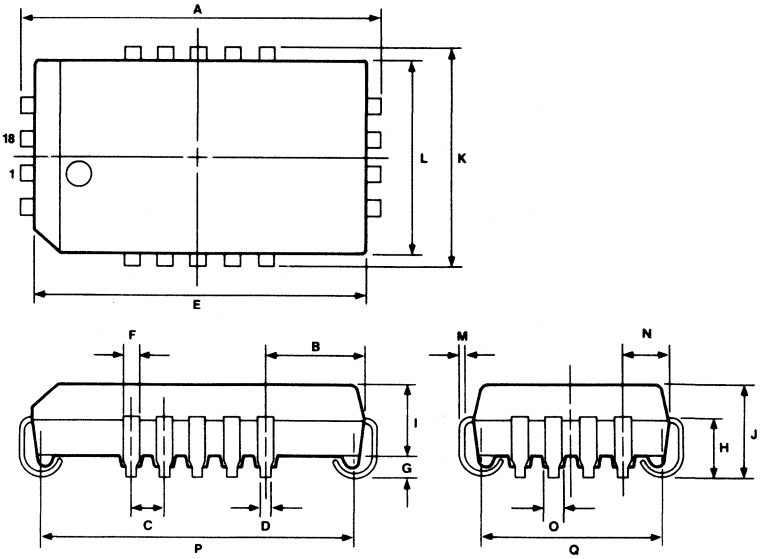
Plastic DIP

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.2 ± .03
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



PLCC

Item	Millimeters
A	13.4 ± .20
B	3.71 ± .15
C	1.27
D	.40 ± .10
E	12.5
F	.60
G	.8 min
H	2.40 ± .20
I	2.6
J	3.50 ± .20
K	8.30 ± .20
L	7.40
M	$.20^{+.10}_{-.05}$
N	1.80 ± .20
O	.70
P	11.68 ± .20
Q	6.6 ± .20



65536 x 4-BIT DYNAMIC MOS RAM

DESCRIPTION

The μPD41464 is a 65,536-word by 4-bit dynamic N-channel MOS random access memory (RAM) designed to operate from a single +5V power supply. The negative voltage substrate bias is generated internally; its operation is automatic and transparent. The μPD41464 utilizes double polylayer N-channel silicon gate processing which provides high storage cell density, high performance, and high reliabilty. The device also uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state I/O is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held on the I/O holding $\overline{CAS}$ low. The data I/O is returned to the high-impedance state by returning $\overline{CAS}$ high. The μPD41464 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by using $\overline{CAS}$ before $\overline{RAS}$ cycles, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or normal read or write cycles on the 256 address combinations of A_0-A_7 during the 4 ms refresh period.

FEATURES

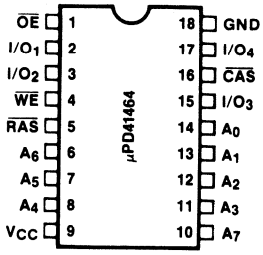
- ☐ 65,536-word by 4-bit organization
- ☐ Single +5 V± 10% power supply
- ☐ Standard 18-pin DIP and PLCC and 20-pin ZIP packages
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation:
  - 28 mW (standby)
  - 440 mW (active, $t_{RC} = t_{RC}$ min)
- ☐ Non-latched TTL-compatible I/O
- ☐ Low input capacitance
- ☐ 256 refresh cycles during 4 ms period

PERFORMANCE RANGES

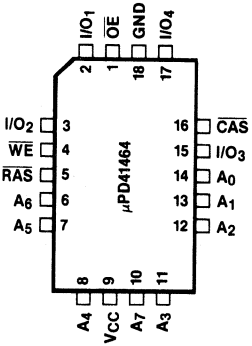
Device	t_{RAC}	t_{CAC}	t_{OEA}	I_{CC1}
μPD41464-10	100 ns	50 ns	25 ns	80 mA
μPD41464-12	120 ns	60 ns	30 ns	75 mA
μPD41464-15	150 ns	75 ns	40 ns	70 mA

PIN CONFIGURATIONS

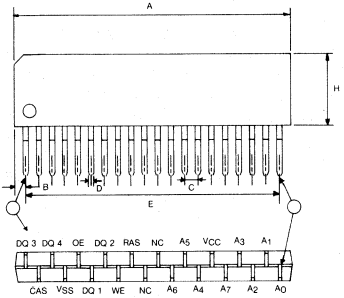
18-Pin DIP (μPD41464C)



18-Pin PLCC (μPD41464L)



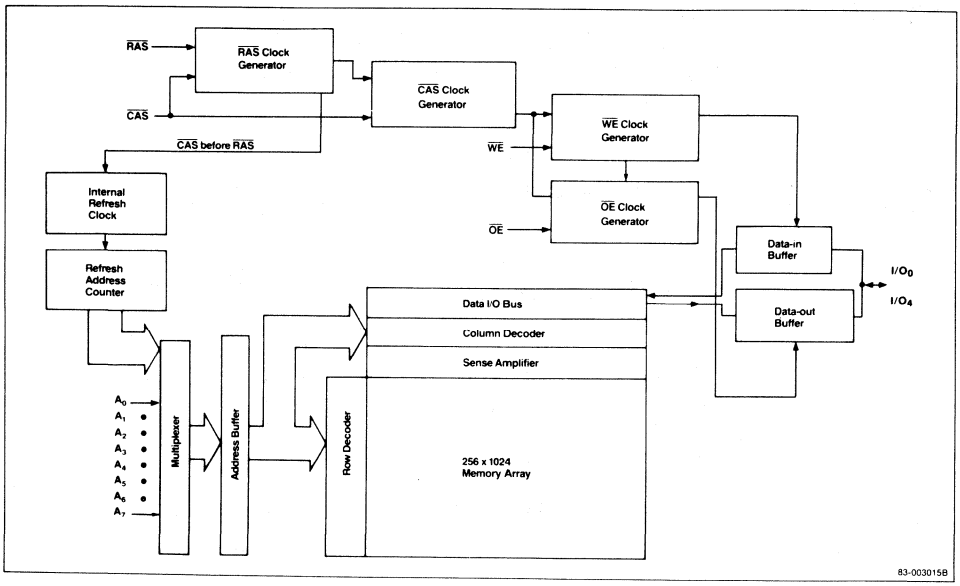
20-Pin ZIP (μPD41464V)



PIN IDENTIFICATION

Symbol	Function
$\overline{OE}$	Output enable
I/O1-I/O4	Data I/O
$\overline{WE}$	Write enable
$\overline{RAS}$	Row address strobe
A0-A7	Address inputs
VCC	Power supply
$\overline{CAS}$	Column address strobe
GND	Ground
NC	No connection

BLOCK DIAGRAM



ABSOLUTE MAX. RATINGS

Voltage on any pin relative to GND	-1,0 to + 7.0 V
Operating temperature, Ta (Ambient)	0 to + 70 ° C
Storage temperature, Tstg (Ambient)	-55 to + 125 ° C (plastic)
Short circuit output current	50 mA
Power dissipation	1 W

Comment:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

($0\,°C \leqq T_a \leqq 70\,°C$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC} G_{ND}	4.5 0	5.0 0	5.5 0	V V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4		5.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0		0.8	V	

DC Electrical Characteristics

($T_a = 0$ to $+70\,°C$, $V_{CC} = 5.0\,V \pm 10\,\%$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Supply Standby Current ($\overline{RAS} = V_{IH}$, D_{OUT} = High Impedance)	I_{CC2}			5.0	mA	
Input Leakage Current, any input (VIN = 0 to +5.5 V, all other pins not under test = 0 V)	$I_{I(L)}$	-10		10	μA	
Output Leakage Current (D_{OUT} is Disabled, V_{OUT} = 0 to +5.5 V)	$I_{O(L)}$	-10		10	μA	
Output High (Logic 1) Voltage (I_{OUT} = -2 mA)	V_{OH}	2.4		V_{CC}	V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2 mA)	V_{OL}	0		0.4	V	

AC CHARACTERISTICS (1) (2)

(T_A = 0°C ~ 70°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	D41464 -10		D41464 -12		D41464 -15		Unit	Notes
		MIN	MAX.	MIN.	MAX.	MIN	MAX.		
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC}min)	ICC1		80		75		70	mA	(5)
Average power supply current, refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC}min)	ICC3		65		60		55	mA	(5)
Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{RC} = t_{RC}min)	ICC4		55		50		45	mA	(5)
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC}min)	ICC5		70		65		60	mA	(5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(6)
Read write cycle time	t_{RWC}	270		300		355		ns	(6)
Page mode cycle time	t_{PC}	100		120		145		ns	(6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(7) (8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(7) (9)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(3)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(12)
$\overline{CAS}$ precharge time	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	

AC CHARACTERISTICS (Cont.)

$T_A = 0°C \sim 70°C$, $V_{CC} = 5V \pm 10\%$

Parameter	Symbol	D41464-10		D41464-12		D41464-15		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		20		25		ns	
Column address hold time referenced $\overline{RAS}$	tAR	65		80		100		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	tRRH	10		10		10		ns	(13)
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	(13)
Write command hold time	tWCH	25		30		40		ns	
Write command hold time referenced $\overline{RAS}$	tWCR	75		90		115		ns	
Write command pulse width	tWP	25		30		40		ns	
Write command to $\overline{RAS}$ lead time	tRWL	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	tCWL	35		40		45		ns	
Data-in set-up time	tDS	0		0		0		ns	(14)
Data-in Hold time	tDH	25		30		40		ns	(14)
Data-in hold time referenced $\overline{RAS}$	tDHR	75		90		115		ns	
Write command set-up time	tWCS	0		0		0		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	130		155		195		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	90		95		120		ns	
Access time from $\overline{OE}$	tOEA		25		30		40	ns	
Data delay time	tOED	25		30		40		ns	
$\overline{OE}$ command hold time	tOEH	0		0		0		ns	
Output turn-off delay to $\overline{OE}$	tOEZ	0	25	0	30	0	40	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive set-up time	tOES	10		10		10		ns	
$\overline{CAS}$ set-up time for $\overline{CAS}$ before $\overline{RAS}$ refresh	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	tCHR	20		25		30		ns	
Random read or write cycle time (refresh counter test cycle)	tTRC	220		245		285		ns	(15)
Read-write cycle time (refresh counter test cycle)	tTRWC	260		290		335		ns	(15)
$\overline{CAS}$ precharge time (refresh counter test cycle)	tTCP	40		50		60		ns	(15)

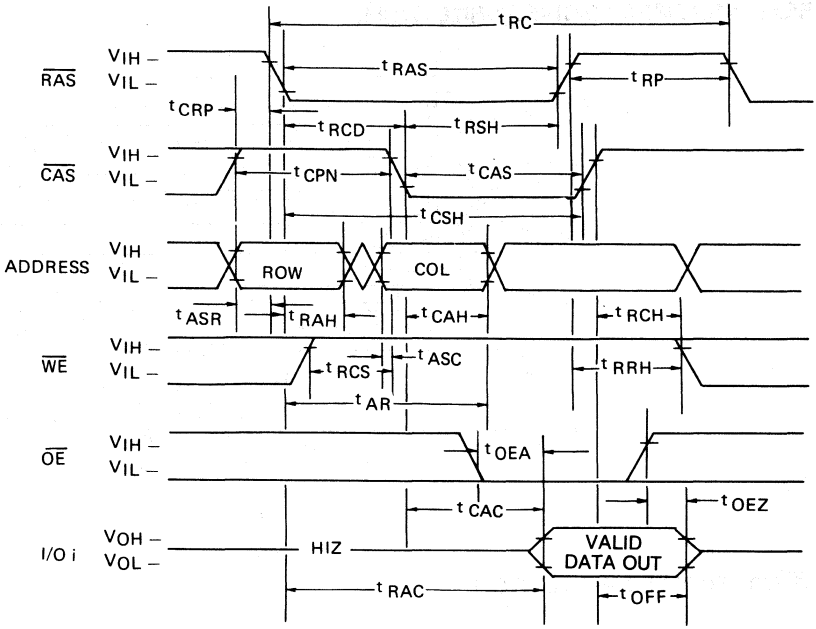
NOTES:

1. All voltages referenced to GND.
2. An initial pause of 100 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
3. AC measurements assume $t_T = 5$ ns.
4. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by any cycle.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
15. Applies for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

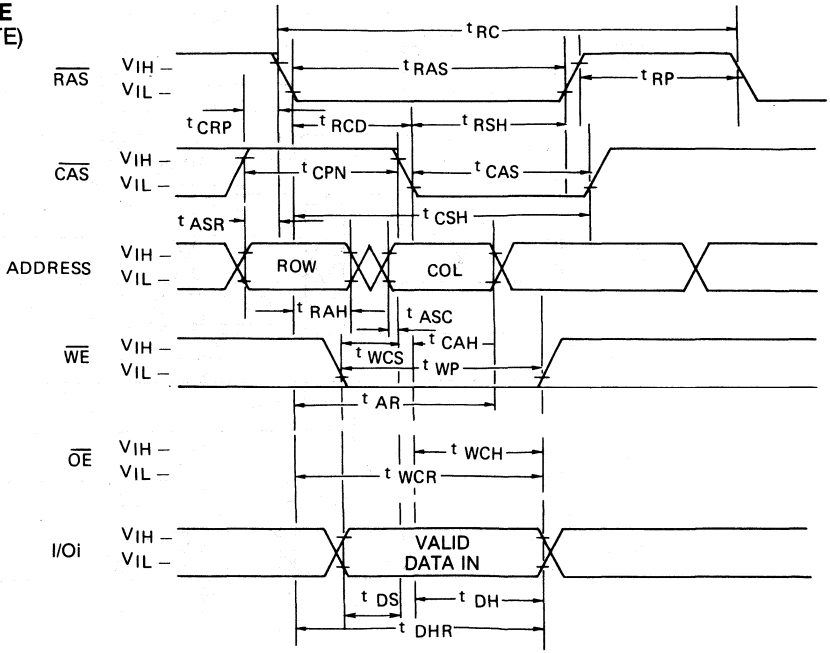
A.C. Electrical characteristics
(0°C ≦ Ta ≦ 70°C) (V_{CC} = 5.0 V ± 10 %)

CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance ($A_0 \sim A_7$)	C_{I1}		5	pF	
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}		8	pF	
Input/Output Capacitance, data ports	C_O		7	pF	

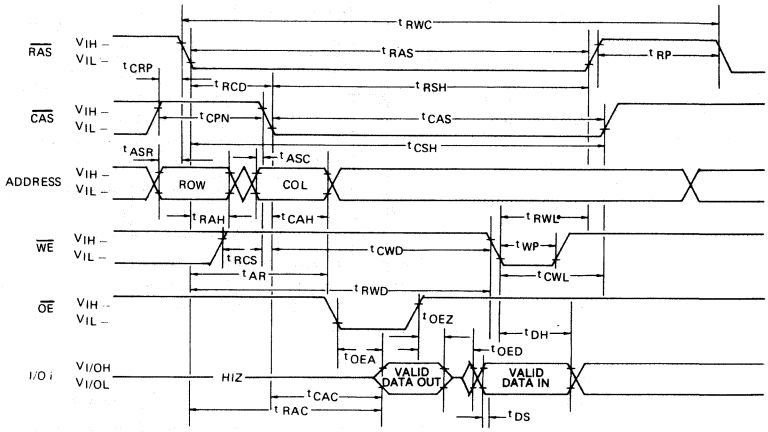
READ CYCLE



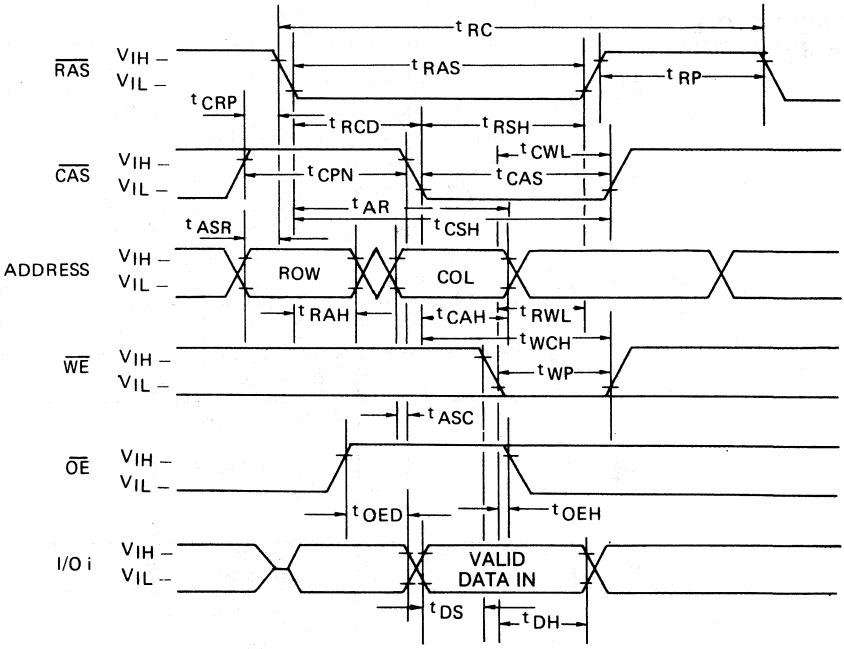
WRITE CYCLE
(EARLY WRITE)



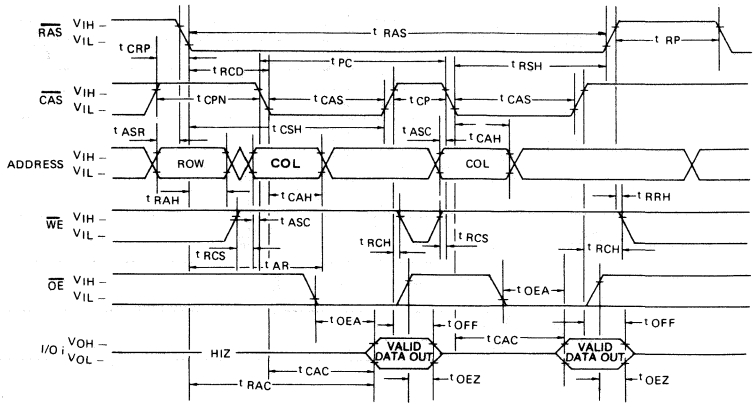
READ-WRITE/READ-MODIFY-WRITE CYCLE



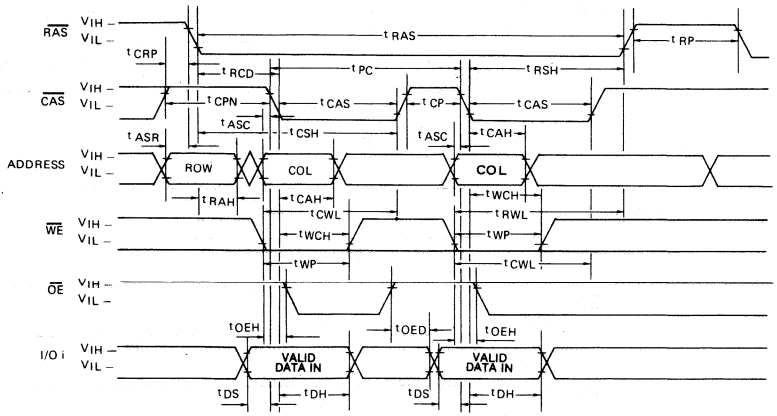
OE CONTROLLED WRITE CYCLE



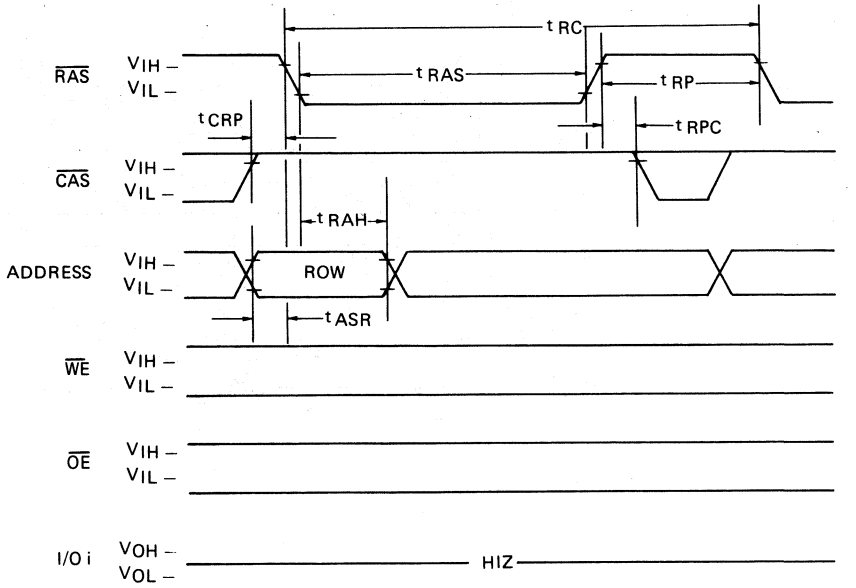
PAGE MODE READ CYCLE



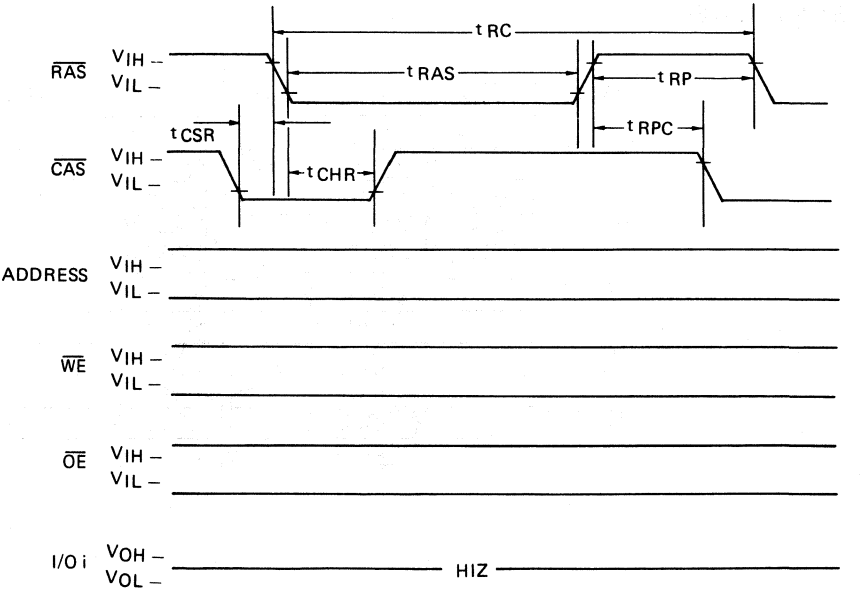
PAGE MODE WRITE CYCLE
(EARLY WRITE)



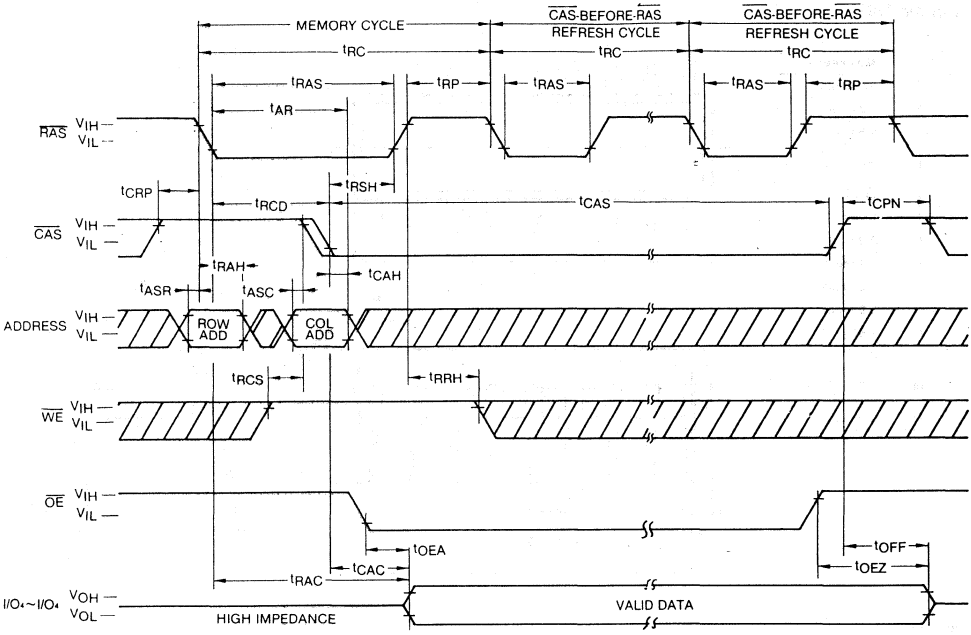
„$\overline{RAS}$ ONLY" REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH



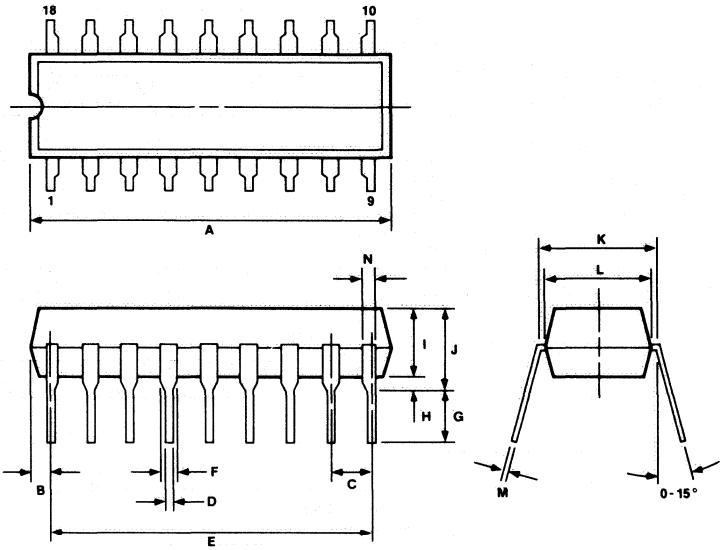
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

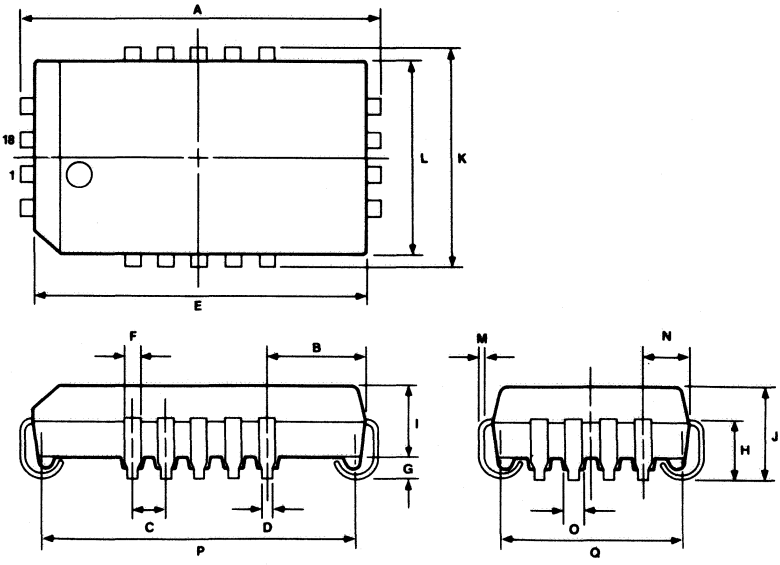
Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.7
M	.25 $^{+.10}_{-.05}$
N	1.0 min



PLCC

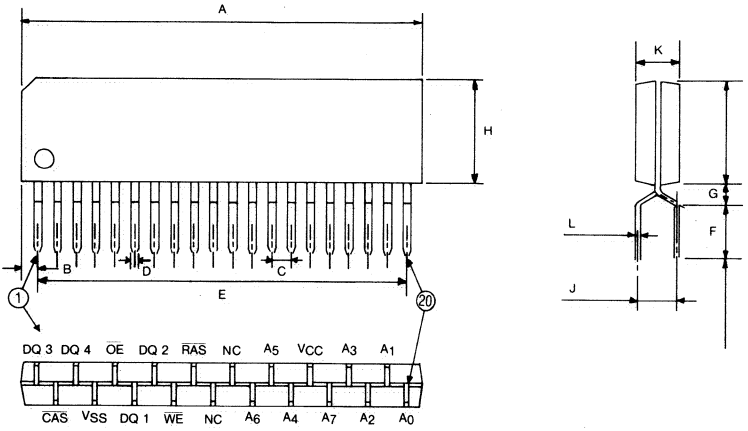
Item	Millimeters
A	13.4 ± .20
B	3.71 ± .15
C	1.27
D	.40 ± .10
E	12.5
F	.60
G	.8 min
H	2.40 ± .20
I	2.6
J	3.50 ± .20
K	8.30 ± .20
L	7.40
M	.20 $^{+.10}_{-.05}$
N	1.80 ± .20
O	.70
P	11.68 ± .20
Q	6.6 ± .20



PACKAGE DIMENSIONS (Cont.)

ZIP

Item	Millimeters
A	26,67 max.
B	1,27 max.
C	1,27 (TP)
D	.50±.10
E	24,13
F	3,3 ± 0,5
G	1,0 min.
H	7,0 max.
I	8,3 max.
J	2,54 (TP)
K	2,8 ± 0,2
L	.25 +0.10 −0.05



32768 x 8-BIT CMOS PSEUDO-STATIC RAM

DESCRIPTION

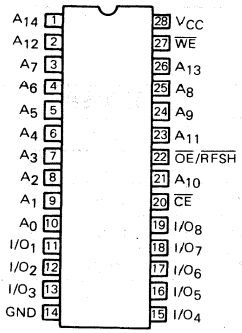
The NEC μPD42832 is a 32,768-words by 8 bits MIX-MOS pseudo-static RAM, designed to operate from a single +5V power supply. Advanced MIX-MOS dynamic circuitry, including sense amplifires, provides wide operating margins and low power dissipation while maintaining high performance.
The μPD42832 is capable of pulse refresh and self refresh. These modes are accomplished by utilizing $\overline{OE}/\overline{RFSH}$ input that will enable the internal generation of refresh address.
The μPD42832 is available in a standard 28-pin plastic package. (μPD42832C and μPD42832C-L) and a 28-pin plastic miniflat package (μPD42832G and μPD42832G-L).

FEATURES

Device	$\overline{CE}$ Access Time	R/W Cycle Time	Power Supply Current	Self Refresh Current
μPD42832-12	120 ns	190 ns	50 mA	1.5 mA/100 μA
μPD42832-15	150 ns	235 ns	40 mA	1.5 mA/100 μA

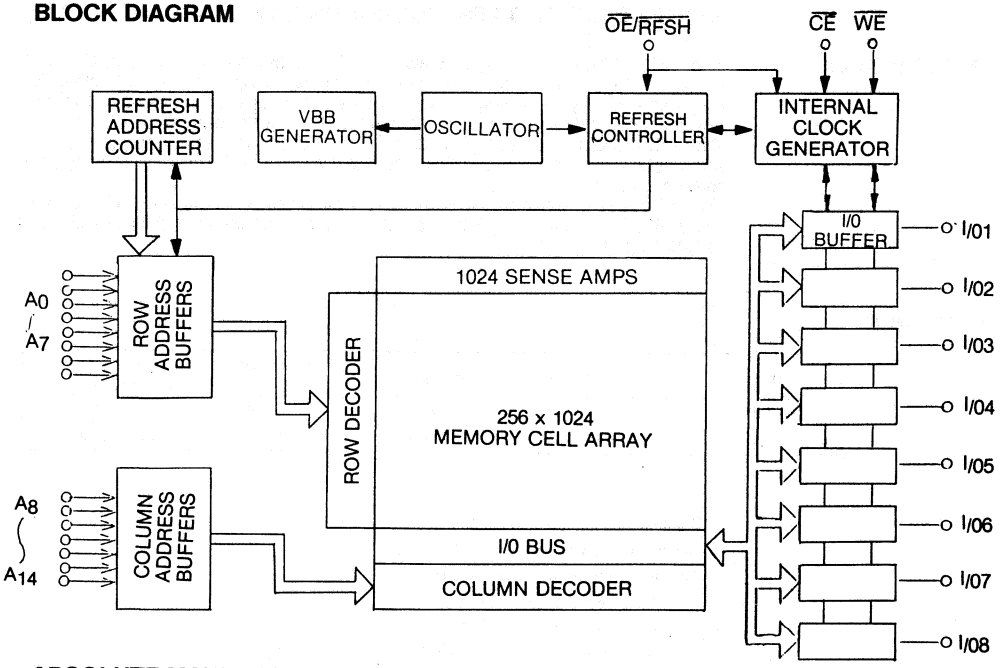
- Organization 32 K words x 8 bits
- Power supply V_{CC} = 5 V ±10 %
- 2 mode refresh by using $\overline{OE}/\overline{RFSH}$
  Pulse refresh, Self refresh
- Low power dissipation
  Stand-by..... 0.5 mA (MAX.)
  Self refresh ... 100 μA (MAX.) μPD42832C/G-L
  1.5 mA (MAX.) μPD42832C/G
- 256 refresh cycles (/4 ms)
- TTL compatible

PIN CONFIGURATION (Top View)



A_0~A_{14}	:	Address Inputs
I/O_1~I/O_8	:	Data Inputs/Outputs
$\overline{CE}$	:	Chip Enable
$\overline{WE}$	:	Write Enable
$\overline{OE}/\overline{RFSH}$	:	Output Enable/Refresh
V_{CC}	:	+5 V Power Supply
GND	:	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Supply Voltage on any Pin except VCC	VT	-1.0 to + 7.0	V
Supply Voltage	VCC	-1.0 to + 7.0	V
Short Circuit Output Current	I0	50	mA
Power Dissipation	Pd	1	W
Operating Temperature	Topt	0 to + 70	°C
Storage Temperature	Tstg	-55 to + 125	°C

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE/RFSH}$	I/O PIN	MODE
High	—	High	High Z	Standby
High	—	Low	High Z	Refresh
Low	High	Low	Dout	Read
Low	High	High	High Z	External Refresh
Low	Low	High	Din	Write

Recommended DC Operating Conditions

(T_a = 0~70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input High Voltage	VIH	2.4		5.5	V
Input Low Voltage	VIL	-1.0		0.8	V

DC Characteristics

(V_{CC} = 5V±10%, T_a = 0~70°C

Parameter	Symbol	Min.	Tip.	Max.	Units	Test Condition
VCC Supply Current Standby Standby	 ICC2 ICC2			 1.0 0.5	 mA mA	 $\overline{CE}$ = $\overline{OE/RFSH}$ = VIH $\overline{CE}$ = $\overline{OE/RFSH}$ = VDD
Self Refresh	ICC3			NOTE	μA	$\overline{OE/RFSH}$ = 0V
Input Leakage Current	$I_{I(L)}$	-10		10	μA	
Output Leakage Current	$I_{O(L)}$	-10		10	μA	
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 4.0mA
Output High Voltage	V_{OH}	2.4		VCC	V	I_{OH} = -1.0mA

Capacitance

(T_a = 25°C, f = 1MHZ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
I/O Capacitance	$C_{I/O}$			10	PF	
Input Capacitance	C_I			7	PF	

NOTE: μPD42832C/G-12/15: ICC3= 1,5mA
μPD42832C/G-12L/15L: ICC3= 0,1mA

AC Characteristics

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

Parameter	Symbol	μPD42832-12		μPD42832-15		Unit
		Min.	Max.	Min.	Max.	
Operating supply current *1	I_{CC1}		50		40	mA
Refresh supply current *2	I_{CC4}		50		40	mA
Pulse refresh supply current *3	I_{CC5}		50		40	mA
Random read or write cycle time	t_{RC}	190		235		ns
Access time from $\overline{CE}$	t_{CEA}		120		150	ns
Chip disable to output in HZ	t_{CHZ}	0	35	0	40	ns
Access time form $\overline{OE}$	t_{OEA}		35		40	ns
Output disable to output in HZ	t_{OHZ}	0	35	0	40	ns
Chip enable to output in LZ	t_{CLZ}	10		10		ns
Output enable to output in LZ	t_{OLZ}	5		5		ns
Chip enable pulse width	t_{CE}	120	10.000	150	10.000	ns
Chip enable precharge time	t_P	60		75		ns
Address set-up time before $\overline{CE}$ low	t_{ASC}	0		0		ns
Address hold time after $\overline{CE}$ low	t_{AHC}	30		40		ns
$\overline{OE}$ hold time after $\overline{CE}$ low	t_{OHC}	0		0		ns
$\overline{OE}$ set-up time before $\overline{CE}$ low	t_{OSC}	0		0		ns
Read command set-up time before $\overline{CE}$ low	t_{RCS}	0		0		ns
Read command hold time after $\overline{CE}$ high	t_{RCH}	0		0		ns
Transition time (rise and fall)	t_T	3	50	3	50	ns
Write command hold time after $\overline{CE}$ low	t_{WCH}	85		105		ns
Write command to $\overline{CE}$ Lead time	t_{CWL}	85		105		ns
Write pulse width	t_{WP}	85		105		ns
Data set-up time before $\overline{WE}$ High	t_{DSW}	75		95		ns
Data hold -time after $\overline{WE}$ high	t_{DHW}	0		0		ns
Data set-up time before $\overline{CE}$ high	t_{DSC}	75		95		ns
Data hold time after $\overline{CE}$ high	t_{DHC}	0		0		ns
Refresh period	t_{REF}		4		4	ms

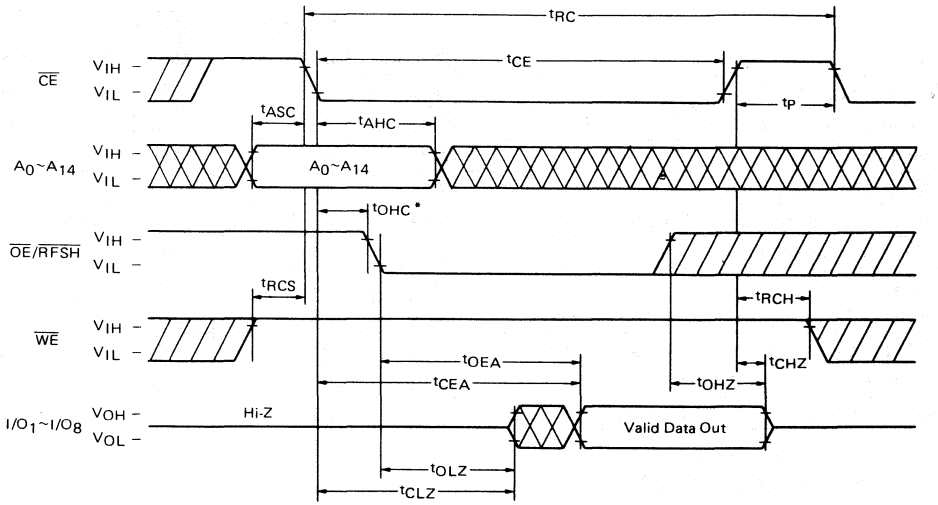
AC Characteristics

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

Parameter	Symbol	μPD42832-12		μPD42832-15		Unit
		Min.	Max.	Min.	Max.	
$\overline{WE}$ to Output in HZ	t_{WHZ}	0	35	0	40	ns
Output active from end of Write	t_{WLZ}	10		10		ns
Read Write Cycle Time	t_{RWC}	295		365		ns
$\overline{CE}$ to $\overline{RFSH}$ Delay Time	t_{RFD}	60		75		ns
$\overline{RFSH}$ Pulse Width in Pulse Refresh	t_{FAP}	80	1000	80	1000	ns
$\overline{RFSH}$ Precharge Time	t_{FP}	30		30		ns
Pulse Refresh Cycle Time	t_{FC}	190		235		ns
$\overline{RFSH}$ to $\overline{CE}$ Set-up time after Pulse Refresh	t_{FCE}	225		275		ns
$\overline{RFSH}$ to $\overline{OE}$ Delay Time after Pulse Refresh	t_{FSR}	95		115		ns
$\overline{RFSH}$ Pulse Width in Self Refresh	t_{FAS}	8000		8000		ns
$\overline{RFSH}$ to $\overline{CE}$ Delay Time after Self Refresh	t_{FRS}	225		275		ns

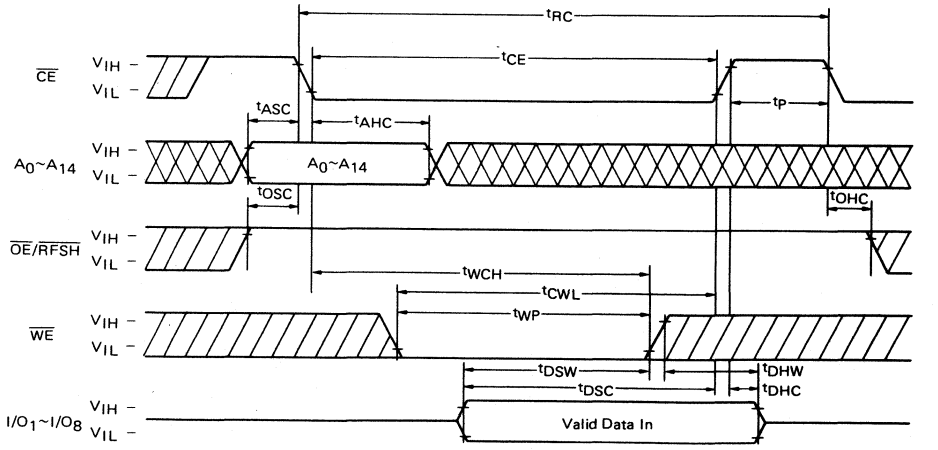
*1 t_{RC} = t_{RC} Min., I_O = 0mA
*2 t_{RC} = t_{RC} Min., $\overline{OE}/\overline{RFSH}$ = $\overline{WE}$ = V_{IH}
*3 t_{FC} = t_{FC} Min., $\overline{CE}$ = V_{IH}

READ CYCLE



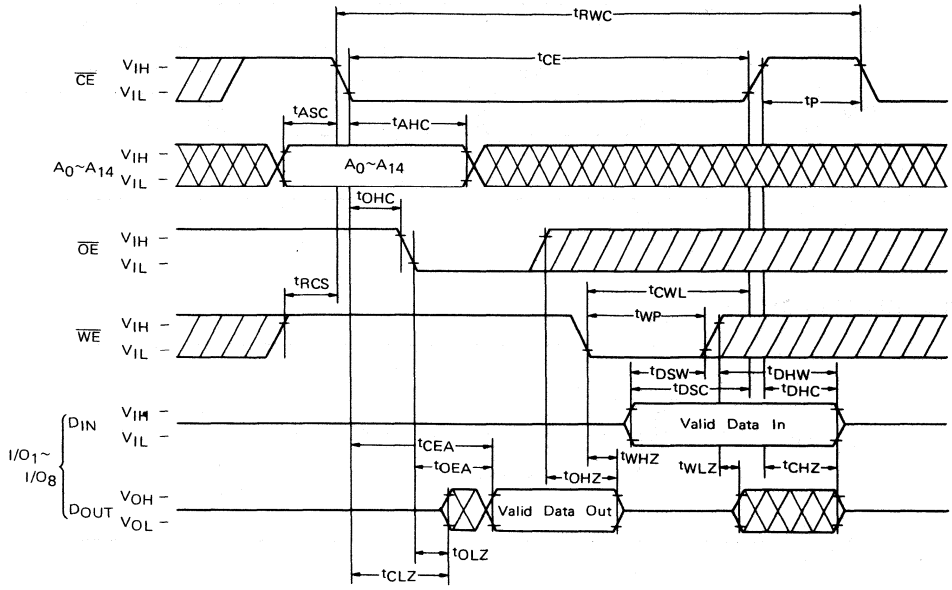
* If Read cycle is following after Pulse or Self refresh cycle, t_{FCE}, t_{FSR} and t_{FAP} are defined.

WRITE CYCLE

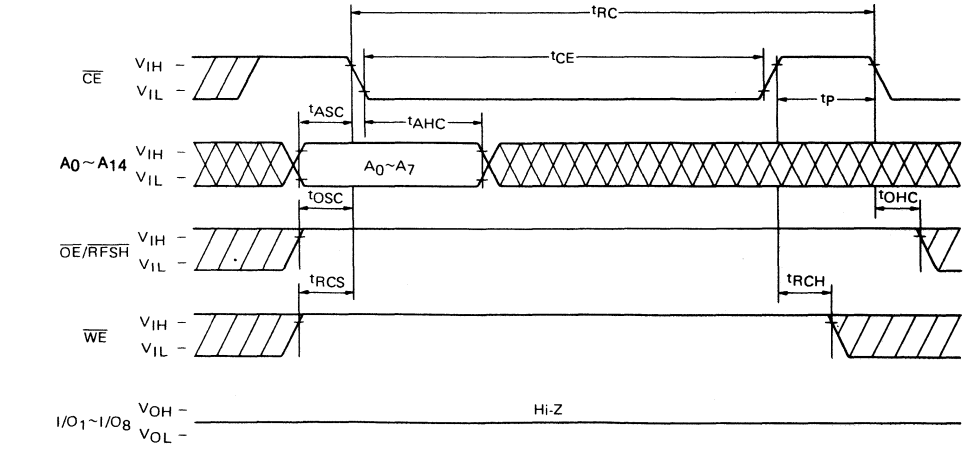


* If Write cycle is following after Pulse or Self refresh cycle, t_{OSC} is defined by t_{FSR}, t_{FCE} and t_{FRS}.

READ MODIFY WRITE CYCLE

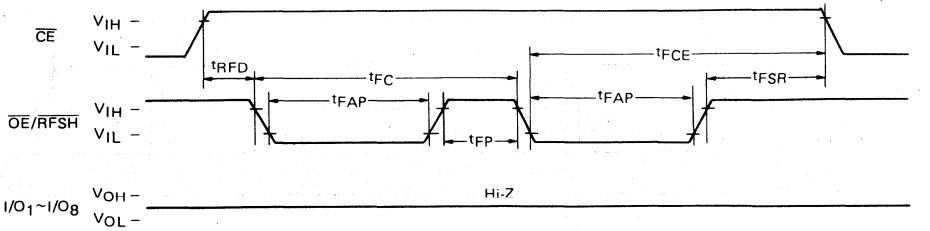


$\overline{CE}$ REFRESH CYCLE

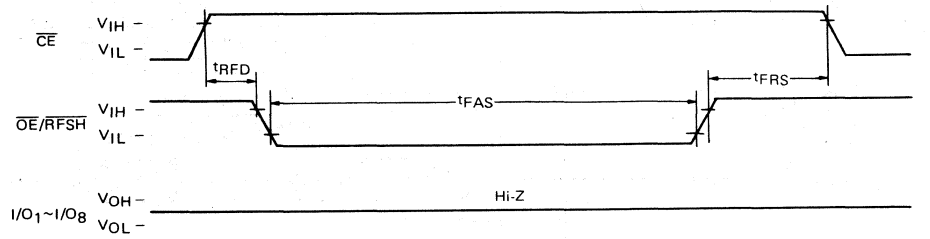


* $A_8 \sim A_{14}$ is not necessary to achieve $\overline{CE}$ Refresh cycle, but it is necessary for these address to keep t_{ASC}, t_{AHC} timing.

PULSE REFRESH CYCLE



SELF REFRESH CYCLE



TIMING FOR BASIC OPERATIONS

(1) Functions of Input Output Terminals

The input output terminals for μPD42832 $\overline{CE}$,$\overline{WE}$,$\overline{OE}$/$\overline{RFSH}$ and A0~A14. I/O1~I/O8.

- Address Input (AO~A14)
  μPD42832 consists of 32K words x8 bits.
  15 address input lines are necessary to select one word data from the 32K words data.
  The address input is taken into the chip at the rising edge of $\overline{CE}$ clock input. Therefore, set-up time and hold time (t_{ASC},t_{AHC}) are determined in accordance with $\overline{CE}$ clock input.
- Data Input Output (I/O1~I/O8)
  μPD42832 requires data control by $\overline{WE}$,$\overline{OE}$ input because it can be used for both input and output. At the write cycle, data is accepted at the rising edge of either $\overline{WE}$ or $\overline{CE}$ clock input, whichever is earlier, in the same way as an ordinary static RAM. At the read cycle access time (t_{CEA},t_{OEA}) is determined by inputting $\overline{CE}$ or $\overline{OE}$ clock.
- Chip Enable Input ($\overline{CE}$)
  This is a chip activate clock to carry out read, write and external refresh cycle by inputting external addresses. Address input is taken into the chip by the $\overline{CE}$ clock input. Also, $\overline{CE}$ clock refreshes 1024 bit (32K words x 8 bits = 262144 bits, 262144 bits divided by 256 cycle = 1024 bits) memory cells selected by the lower address input.
- Write Enable Input ($\overline{WE}$)
  Read, write action control input. μPD42832, unlike an ordinary DRAM, accepts the data input into the chip at the rising edge of $\overline{WE}$ input. This makes it easy to design the timing. Also, it is capable of utilizing the Read Modify Write Cycle which executes read and write consecutively during one cycle.
- Output Enable Input/Refresh Input ($\overline{OE}$/$\overline{RFSH}$)
  μPD42832 $\overline{OE}$/$\overline{RFSH}$ inputs are multiplexed with two functions, Data Input Output I/O1~I/O8, Output Timing Control and Refresh Control. The following chart shows the read and refresh actions by the $\overline{OE}$/$\overline{RFSH}$ inputs.

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$/$\overline{RFSH}$	Action Mode
H	–	L	Refresh
L	H	L	Read

This refreshing action by $\overline{OE}$/$\overline{RFSH}$ is capable of two modes, Pulse Refresh and Self Refresh. The pulse refresh is executed during a regular read/write cycle, 256 times per 4 ms are required. The self refresh is used to retain the data for a long time. The switching of the modes is achieved by the pulse width at the low level time of $\overline{OE}$/$\overline{RFSH}$. In particular, at the time of self refresh, $\overline{OE}$/$\overline{RFSH}$ is merely kept to the low level, therefore, it can be backed up by a low data retaining current (100 μA MAX.). This is the same small current needed for a CMOS static RAM.

(2) μPD42832 Actions

(a) Memory Access Cycle-Read, Write, Read Modify Write Cycle

- Read Cycle
  During the same cycle, $\overline{CE}$ clock, $\overline{OE}/\overline{RFSH}$ inputs are made active and $\overline{WE}$ input is made inactive to output data at t_{CEA} (or t_{OEA} depending on the $\overline{OE}$ input timing). At this time, it is necessary to delay $\overline{OE}/\overline{RFSH}$ input longer than t_{OHC} because μPD42832 multiplexes two functions—data output function and refresh control function. Also, the output data becomes uncertain at either $\overline{OE}$ clock or $\overline{CE}$ clock's rising edge whichever is earlier.
- Write Cycle
  A write cycle is executed when during same cycle $\overline{CE}$ clock and WE input are both active, and $\overline{OE}/\overline{RFSH}$ input is inactive.
  Unlike ordinary DRAMs, the write cycle of μPD42832 adopts the static RAM type write-in method which takes in data at the rising edge of either WE or $\overline{CE}$ whichever comes earlier. Therefore, it is extremely easy to connect it as an ordinary CPU memory.
- Read Modify Write Cycle
  μPD42832 is capable of read modify write cycle. This cycle, after executing a read cycle by inputting $\overline{OE}/\overline{RFSH}$, modifies the output data and writes it into the same address by $\overline{WE}$ input. This is done in one same cycle. At this time, if new data is to be written in, special care is required of the $\overline{OE}/\overline{RFSH}$ control to prevent short circuiting of the I/O bus.

(b) Memory Refresh Cycle—$\overline{CE}$ Refresh Cycle, $\overline{OE}/\overline{RFSH}$ Pulse Refresh, Self Refresh Cycle

μPD42832 uses one transistor dynamic memory cell and require refreshing. Refreshing means rewriting the electric charge of the memory cell that stores "H" "L" (or 1, 0) during the refresh period t_{REF}=4 ms when amplification by sense amp is possible. In the case of μPD42832 address locations 0~255 designated by A_0~A_7 need to be refreshed.
μPD42832 is capable of two modes: $\overline{CE}$ refresh which carries out refreshing by designating external addresses (A_0~A_7 and clocking $\overline{CE}$, Pulse Self Refresh which carries out refreshing by way of the refresh control circuit within the chip, when $\overline{OE}/\overline{RFSH}$ clock is made "L" while $\overline{CE}$ clock is made "H" (inactive).

- $\overline{CE}$ Refresh
  When $\overline{CE}$ clock input is active and $\overline{OE}/\overline{RFSH}$ input is inactive, I/O terminals hold high impedance. At this time, inputting the address designated by A0~A7 carries out refreshing. $\overline{CE}$ refresh action, by itself, is irrelevant to the state of I/O terminals, therefore read or write action may substitute refresh. (In application to the video RAM, etc., where the address is constantly incremented and decremented, new refresh action sometimes becomes necessary.)
- $\overline{OE}/\overline{RFSH}$ Refresh Cycle
  Refresh is executed via refresh control circuit within the chip when $\overline{OE}/\overline{RFSH}$ clock is made "L" after $\overline{CE}$ clock input is made "H". This refreshing by $\overline{OE}/\overline{RFSH}$ clock becomes pulse refresh mode when $\overline{OE}/\overline{RFSH}$ clock pulse width is less than 1 μs, and becomes self refresh mode when it is more than 8 μs. In particular, during the self refresh mode, the consumed current is less than 100 μA, which allows data back up with an extremely small current consumption.

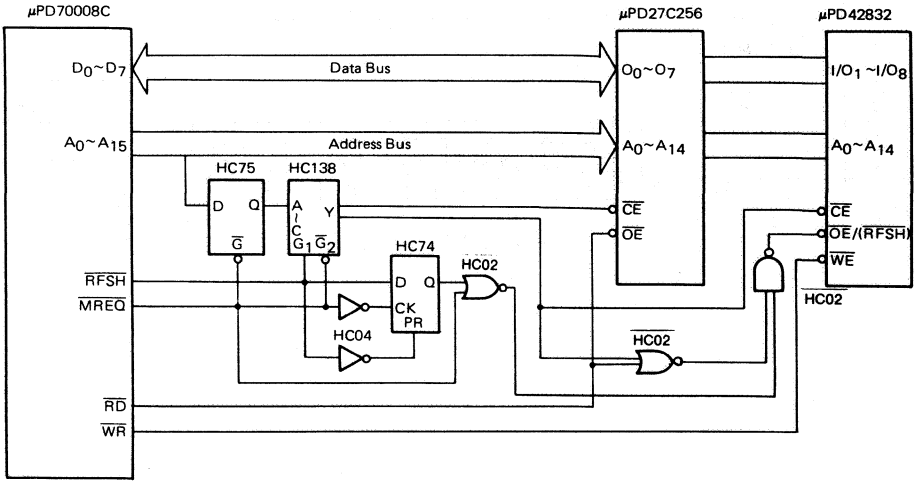
μPD42832 Application

–Coupling to 8 bit CMOS CPU μPD70008C–

μPD70008C is a general purpose 8 bit CPU designed and manufactured via CMOS process. In particular, μPD70008 is equipped with the stand-by mode which can reduce power consumption drastically.

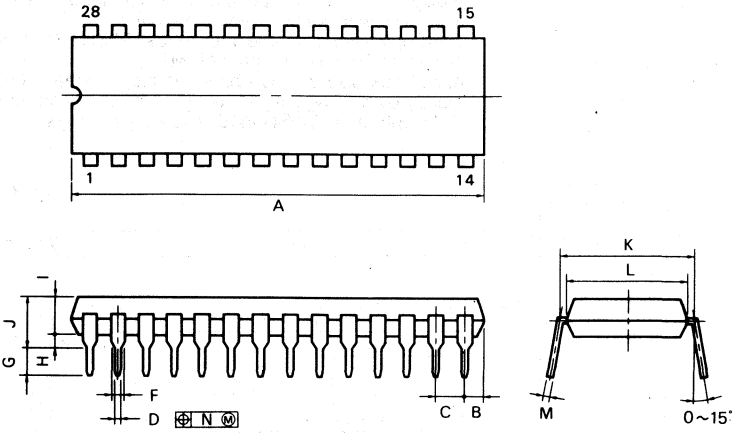
This application example uses refresh RFSH at the time of M1 cycle and carries out refresh at T_3 and T_4 states of M1.

Also, back up by Ni-Cd batteries etc, together with the CPU, is made possible merely by holding the CPU at stand-by condition by INT or NMI input and making HALT output $\overline{OE}/\overline{RFSH}$ input and keeping it low.



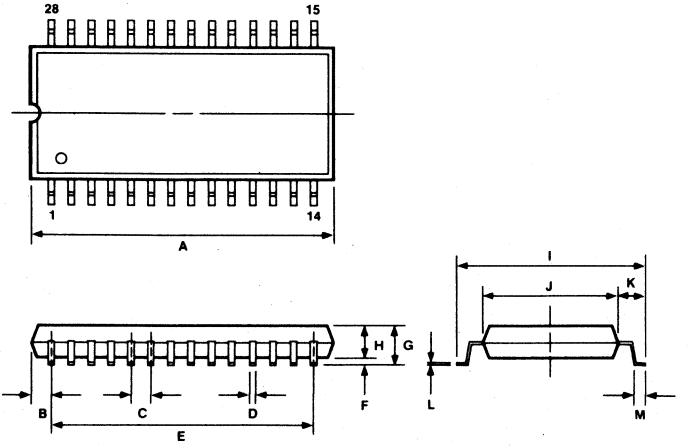
28 PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{\pm 0.10}$
F	1.2 MIN.
G	$3.6^{\pm 0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25



28 PIN PLASTIC MINIFLAT

Item	Millimeters
A	19.05 max
B	1.27 max
C	1.27 [TP]
D	.40 ± .10
E	16.51
F	$.1^{+.2}_{-.1}$
G	3.0 max
H	2.55
I	11.8 ± .3
J	8.4
K	1.7
L	$.15^{+.10}_{-.05}$
M	.7 ± .2



1,048,576 x 1-BIT DYNAMIC NMOS RAM

DESCRIPTION

The μPD411000C/LA is a page mode version 1,048,576-word by 1-bit dynamic N-channel MOS random access memory (RAM). It is designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally. The μPD411000C/LA utilizes advanced double-level polycide technology. The use of trench capacitors minimizes silicon area while providing high storage cell density, high performance, and high reliability. The device uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to the high-impedance state by returning $\overline{CAS}$ high. Hidden refresh allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh may be accomplished by using a $\overline{CAS}$ before $\overline{RAS}$ cycle, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or by a normal read or write cycle on the 512 address combinations of A_0-A_8 during the 8 ms refresh period.

FEATURES

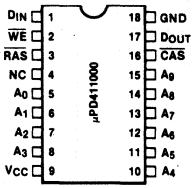
- ☐ 1,048,576-word by 1-bit organization
- ☐ Page mode operation
- ☐ High density 18-pin plastic DIP (μPD411000C) or 26/20-pin plastic SOJ (μPD411000LA)
- ☐ Single + 5 V ±10% power supply
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Low power dissipation:
  - 28 mW standby (max)
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Non-latched TTL-compatible three-state output
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during 8 ms period

PERFORMANCE RANGES

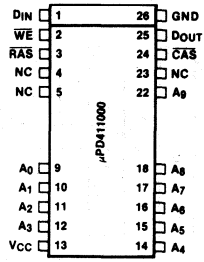
Device	Row Access Time (Max)	R/W Cycle (Min)	RMW Cycle (Min)	Page Mode Cycle (Min)
μPD411000-12	120 ns	220 ns	265 ns	120 ns
μPD411000-15	150 ns	260 ns	310 ns	145 ns

PIN CONFIGURATION

18-Pin Plastic DIP



26/20-Pin SOJ



PIN IDENTIFICATION

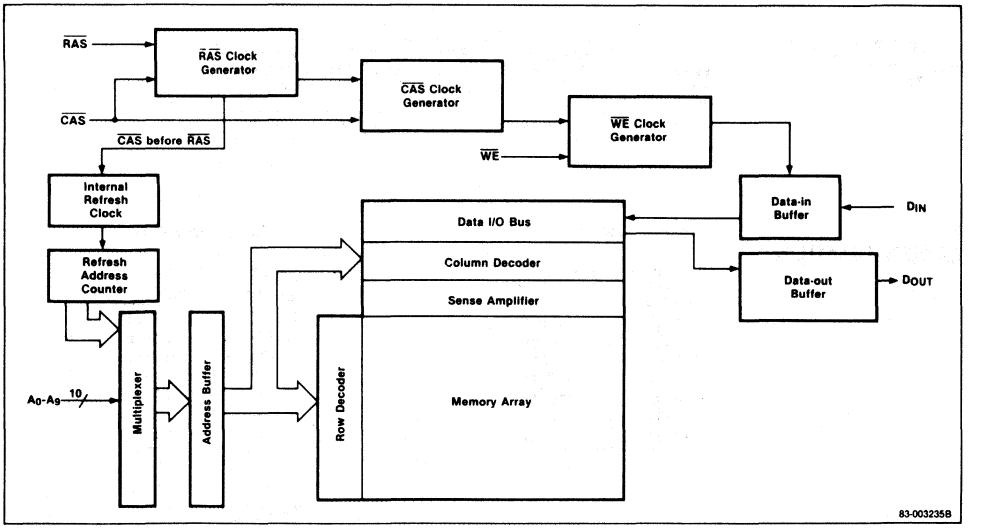
Plastic DIP

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4	NC	No connection
5-8, 10-15	A_0-A_9	Address inputs
9	V_{CC}	Power supply
16	$\overline{CAS}$	Column address strobe
17	D_{OUT}	Data output
18	GND	Ground

Plastic SOJ

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4, 5, 23	NC	No connection
6-8, 19-21	—	No external lead
9-12, 14-18, 22	A_0-A_9	Address inputs
13	V_{CC}	Power supply
24	$\overline{CAS}$	Column address strobe
25	D_{OUT}	Data output
26	GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = 25 °C, f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
Input capacitance	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

DC CHARACTERISTICS

T_A = 0 to +70 °C; V_{CC} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = Hi-Z
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Ouput high voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

AC CHARACTERISTICS

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411000-12 Min	Limits μPD411000-12 Max	Limits μPD411000-15 Min	Limits μPD411000-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		100		90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh mode, average	I_{CC3}		85		75	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode operation, average	I_{CC4}		85		75	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC6}		90		80	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		30		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

AC CHARACTERISTICS (cont)

$T_A = 0$ to +70°C; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits μPD411000-12 Min	Limits μPD411000-12 Max	Limits μPD411000-15 Min	Limits μPD411000-15 Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	25		30		ns	
Page cycle time	t_{PC}	120		145		ns	(Note 6)
$\overline{CAS}$ precharge time, page cycle	t_{CP}	50		60		ns	
Refresh period	t_{REF}		8		8	ms	Addresses A_0-A_8

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to +70°C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

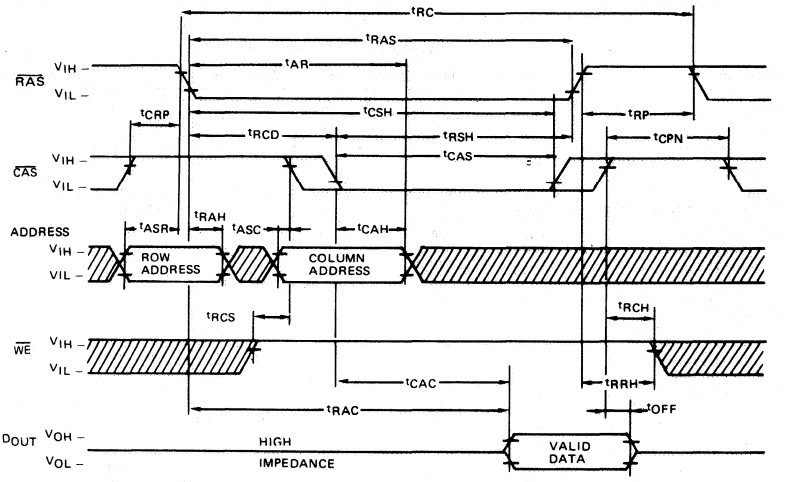
(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

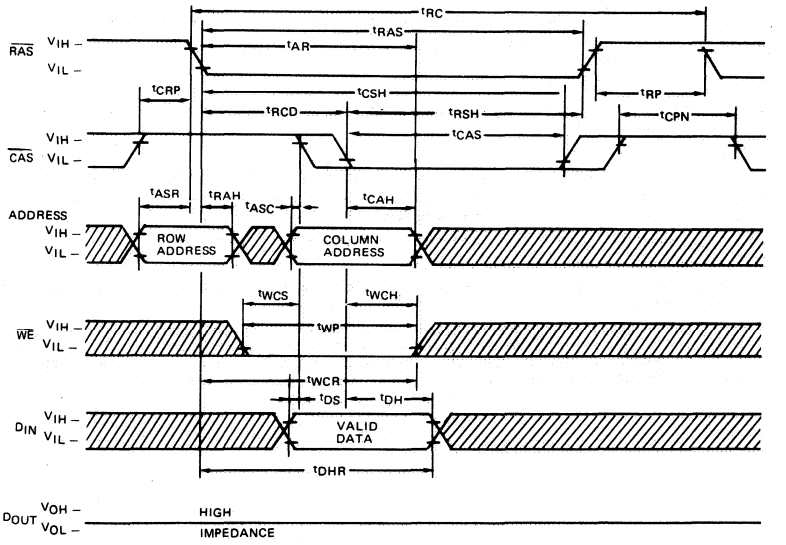
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

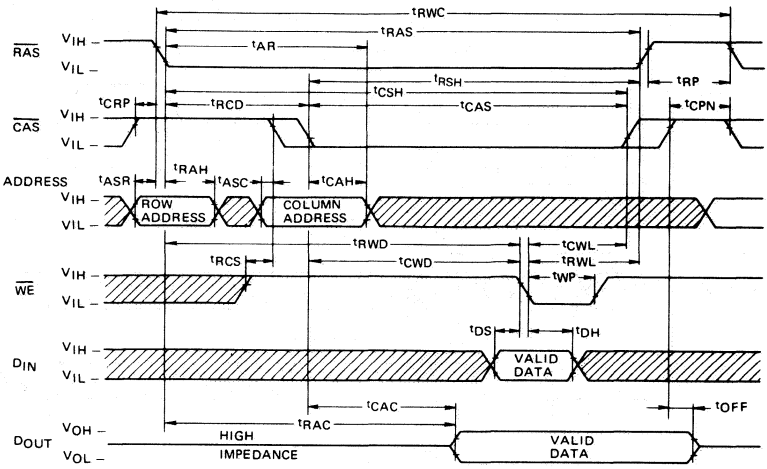
READ CYCLE



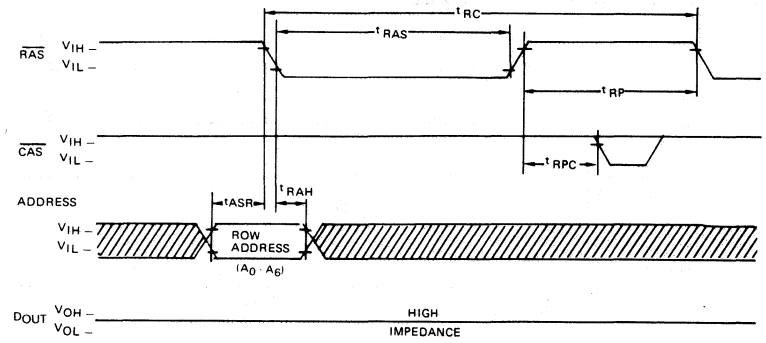
WRITE CYCLE
(EARLY WRITE)



READ-WRITE / READ-MODIFY-WRITE CYCLE

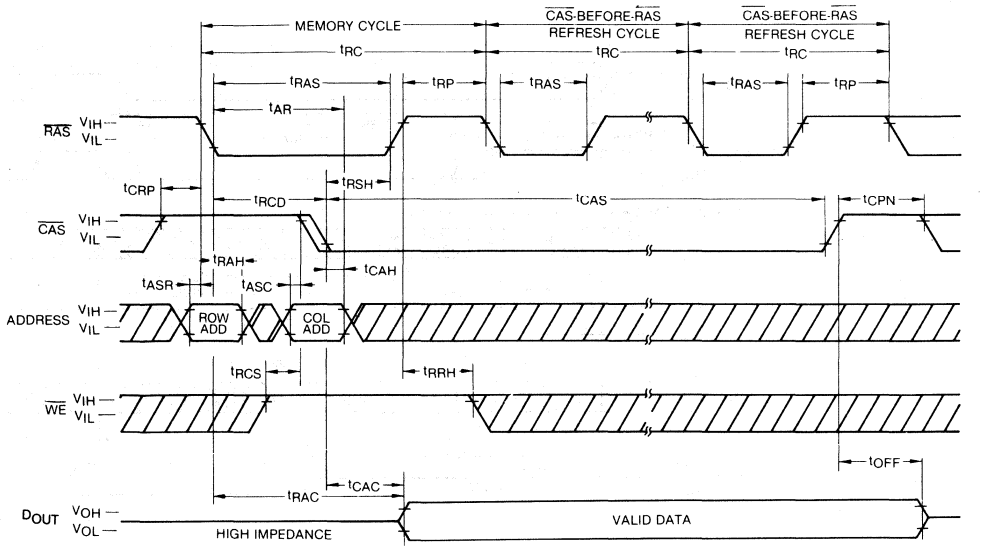


„RAS ONLY" REFRESH CYCLE

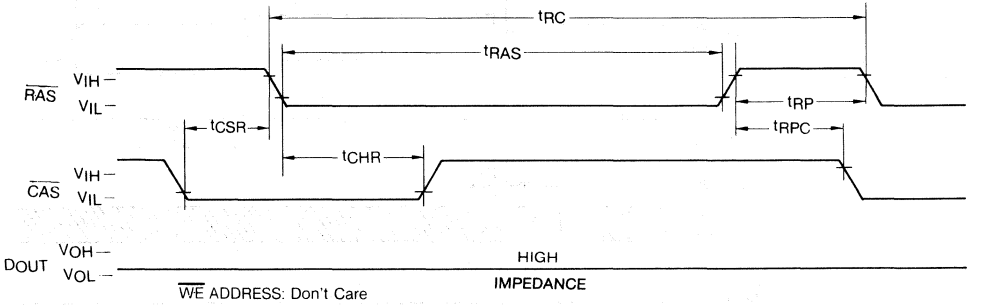


* $\overline{WE}$: Don't care

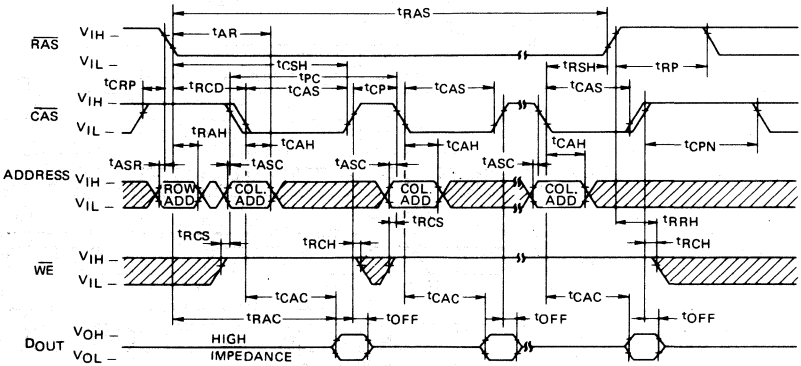
HIDDEN REFRESH CYCLE



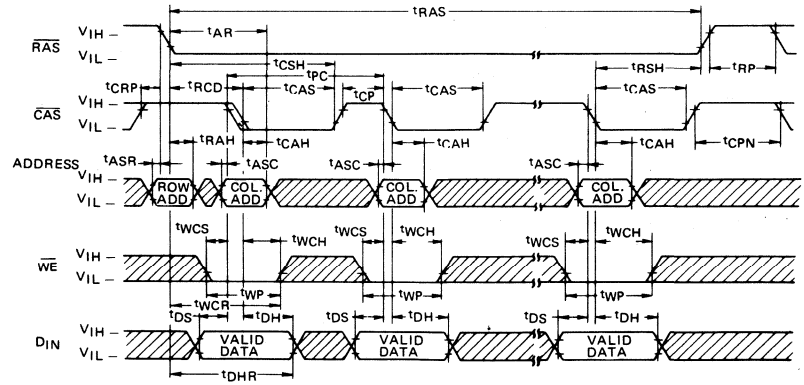
CAS Before RAS REFRESH Cycle



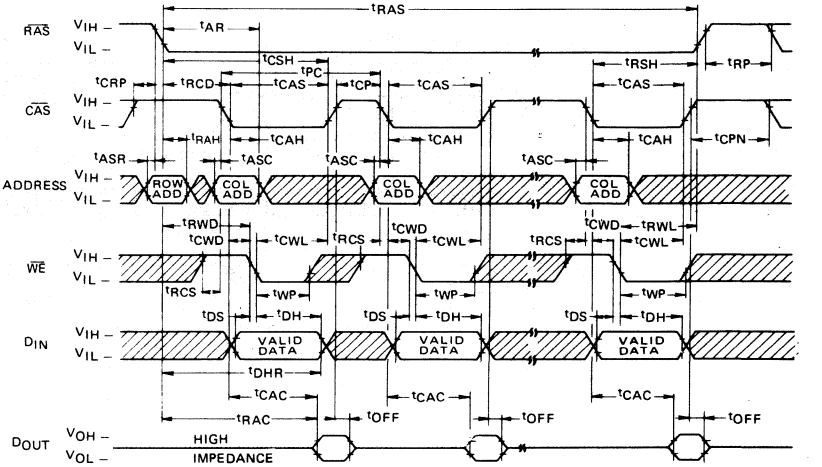
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE (EARLY WRITE)



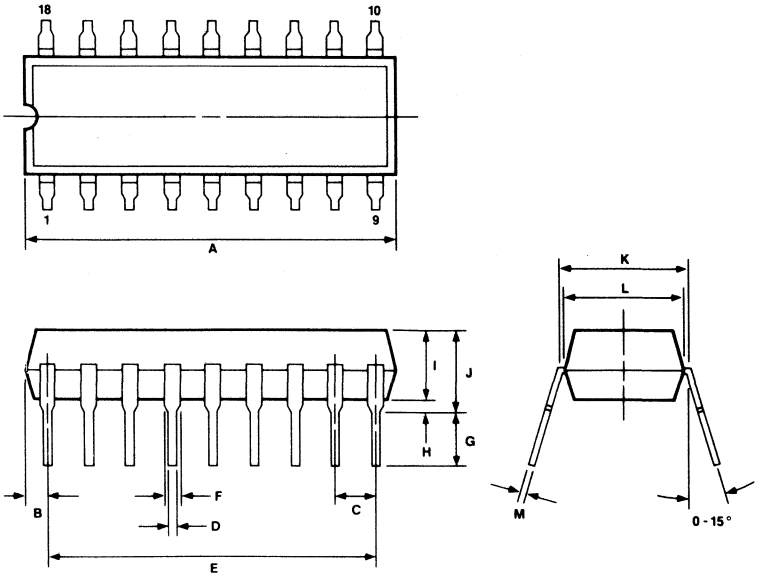
PAGE MODE READ-WRITE / READ-MODIFY-WRITE CYCLE



PACKAGE DIMENSIONS

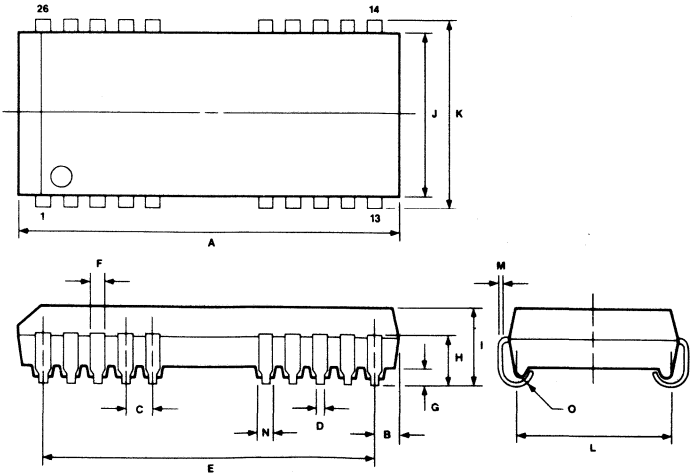
Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



Plastic SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



1,048,576 x 1-BIT DYNAMIC NMOS RAM

DESCRIPTION

The μPD411001C/LA is a nibble mode version, 1,048,576-word by 1-bit dynamic N-channel MOS random access memory (RAM). It is designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally. The μPD411001C/LA utilizes advanced double-level polycide technology. The use of trench capacitors minimizes silicon area while providing high storage cell density, high performance, and high reliability. The device uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to the high-impedance state by returning $\overline{CAS}$ high. Hidden refresh allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh may be accomplished by using a $\overline{CAS}$ before $\overline{RAS}$ cycle, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or by a normal read or write cycles on the 512 address combinations of A_0-A_8 during the 8 ms refresh period.

FEATURES

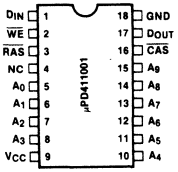
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single + V 10j% power supply
- ☐ Nibble mode operation
- ☐ High density 18-pin plastic DIP (μPD411001C) or 26/20-pin SOJ (μPD411001LA)
- ☐ Low power dissipation:
  - 28 mW standby (max)
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Non-latched TTL-compatible three-state output
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during 8 ms period

PERFORMANCE RANGES

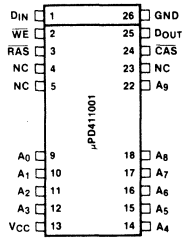
Device	Row Access Time (max)	Read/Write Cycle (min)	RMW Cycle (min)	Nibble Mode Access Time (max)
μPD411001-12	120 ns	220 ns	265 ns	30 ns
μPD411001-15	150 ns	260 ns	310 ns	35 ns

PIN CONFIGURATIONS

18-Pin Plastic DIP



26/20-Pin Plastic SOJ



PIN IDENTIFICATION

Plastic DIP

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4	NC	No connection
5-8, 10-15	A_0-A_9	Address inputs
9	V_{CC}	Power supply
16	$\overline{CAS}$	Column address strobe
17	D_{OUT}	Data output
18	GND	Ground

Plastic SOJ

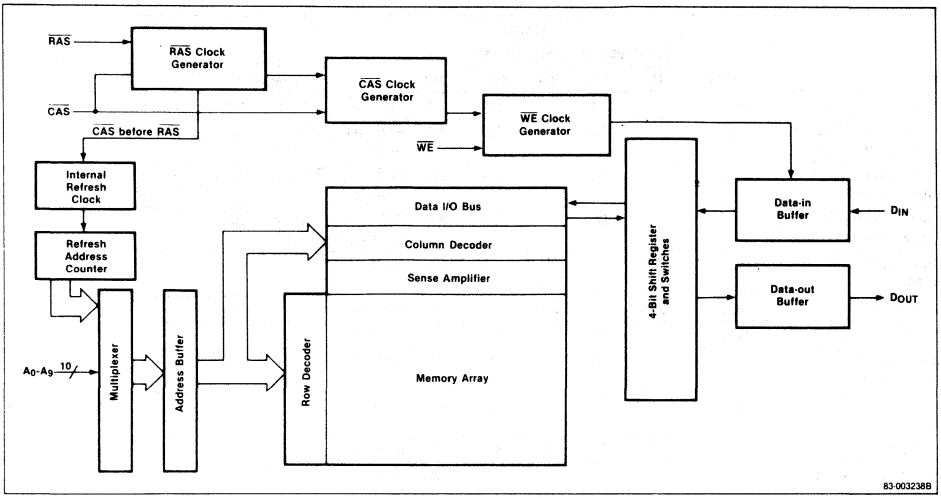
No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4, 5, 23	NC	No connection
6-8, 19-21	—	No external lead
9-12, 14-18, 22	A_0-A_9	Address inputs
13	V_{CC}	Power supply
24	$\overline{CAS}$	Column address strobe
25	D_{OUT}	Data output
26	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short circuit output current	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



DC CHARACTERISTICS

$T_A = 0$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = Hi-Z
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, $V_{OUT} = 0$ to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	$I_{OL} = 4.2$ mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -5$ mA

CAPACITANCE

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
Input capacitance	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

AC CHARACTERISTICS

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-12 Min	Limits μPD411001-12 Max	Limits μPD411001-15 Min	Limits μPD411001-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		100		90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh mode, average	I_{CC3}		85		75	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, nibble mode operation, average	I_{CC5}		40		35	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{NC} = t_{NC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC6}		90		80	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$. $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$, non-nibble cycle	t_{CAC}		60		75	ns	(Notes 7, 9)
Access time from $\overline{CAS}$, nibble mode cycle	t_{NAC}		30		35	ns	(Note 7)
Output buffer turn-off delay	t_{OFF}	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{RAS}$ hold time (nibble mode)	t_{NRSH}	30		35		ns	
$\overline{CAS}$ pulse width, non-nibble mode	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	

AC CHARACTERISTICS (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-12 Min	Limits μPD411001-12 Max	Limits μPD411001-15 Min	Limits μPD411001-15 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time	t_{CPN}	25		30		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time, non-nibble cycle	t_{CWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time, nibble mode cycle	t_{NCWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay, non-nibble cycle	t_{CWD}	60		75		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay, nibble mode cycle	t_{NCWD}	30		35		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	

AC CHARACTERISTICS (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-12 Min	Max	Limits μPD411001-15 Min	Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	25		30		ns	
Nibble mode cycle time	t_{NC}	65		70		ns	(Note 6)
$\overline{CAS}$ pulse width, nibble mode cycle	t_{NAS}	30	10000	35	10000	ns	
Refresh period	t_{REF}		8		8	ms	Addresses A_0-A_8

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC5}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

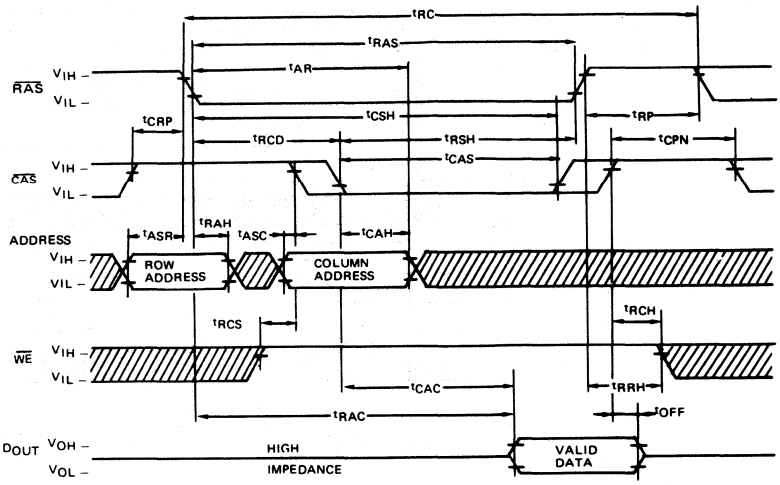
(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

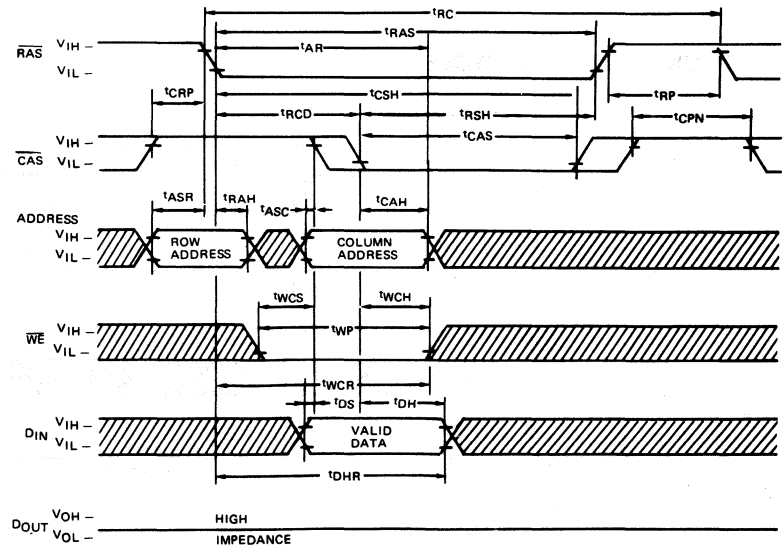
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{NCWD} are restrictive operating parameters in read-write/read-modify-write and nibble mode read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write or nibble mode early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble mode read-write cycle and the data output will contain data read from the selected cell. If none of the above conditions are met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

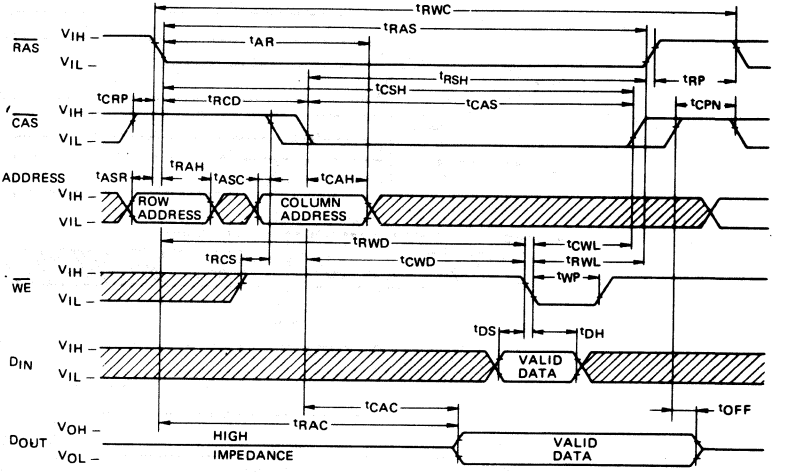
READ CYCLE



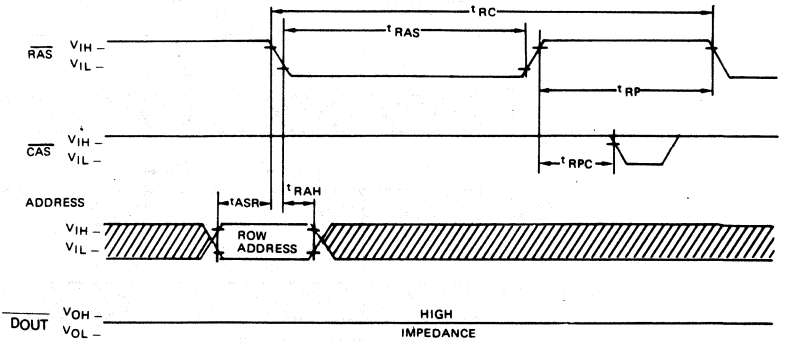
WRITE CYCLE
(EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

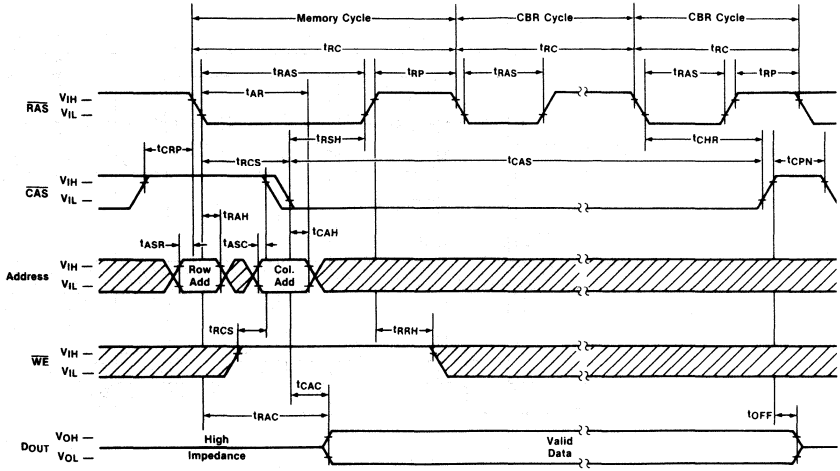


"RAS"-ONLY" REFRESH CYCLE

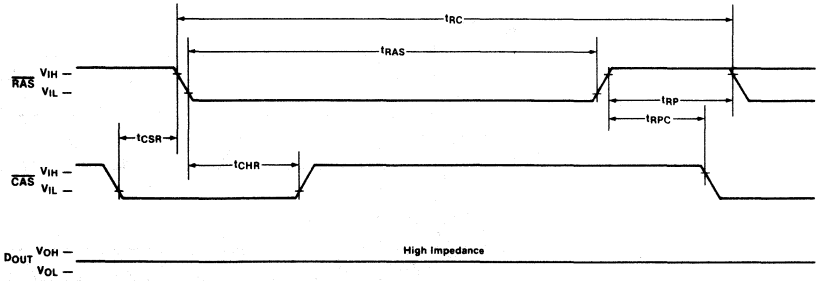


* $\overline{WE}$: Don't care

HIDDEN REFRESH CYCLE

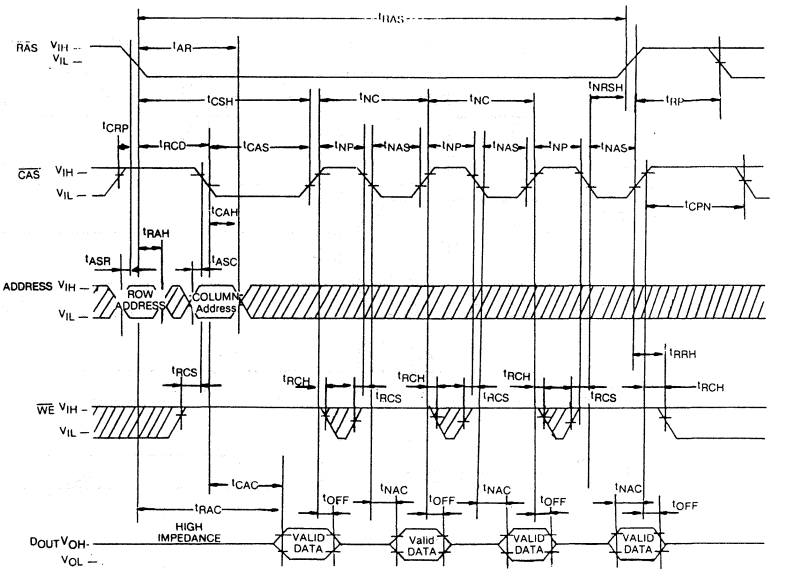


CAS BEFORE RAS REFRESH CYCLE

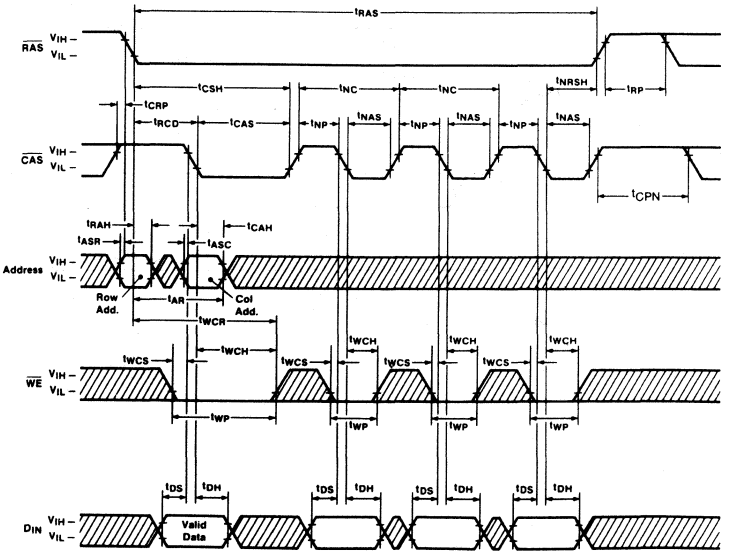


WE, Address: Don't Care.

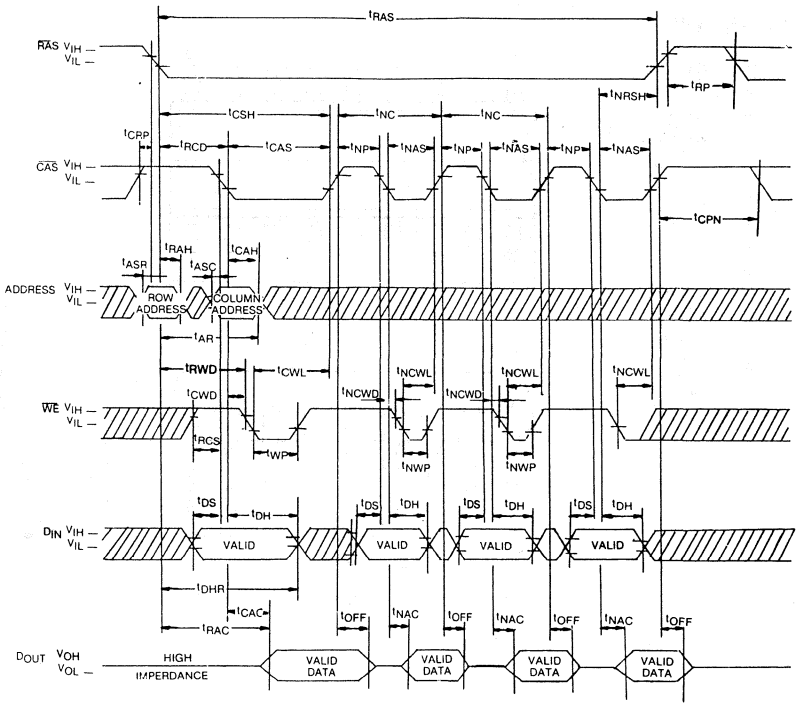
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)



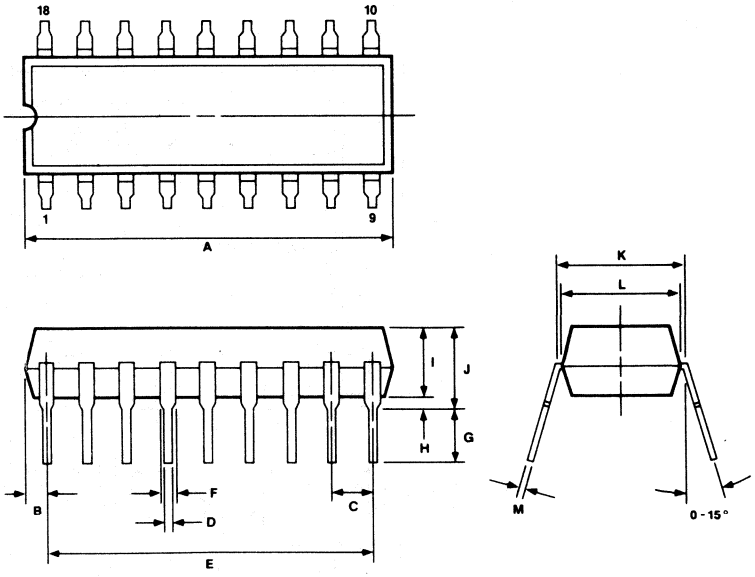
NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



PACKAGE DIMENSIONS

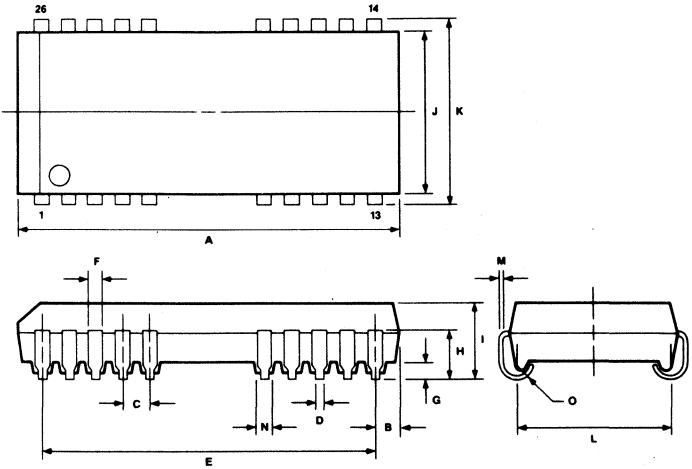
Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



Plastic SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



μPD421000 (FAST PAGE)

1.048.576W x 1 BIT DRAM

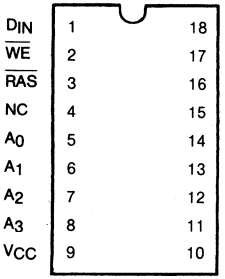
FEATURES

- 1.048.576 words by 1 bit organization
- low power dissipation CMOS DRAM
- single 5 V ± 10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- 512 cycle, 8 ms refresh
- High density 18-pin plastic DIP (μPD421000C) or 26/20-pin plastic SOJ (μPD421000LA)
- Fast Page mode

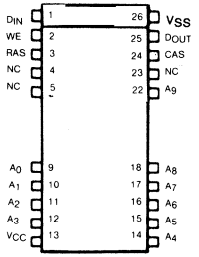
FAMILY	TRAC	TCAC	TAA	ICC1
μPD421000 - 8	80 ns	20 ns	45 ns	70 mA
μPD421000 - 10	100 ns	25 ns	55 ns	60 mA
μPD421000 - 12	120 ns	30 ns	65 ns	50 mA

PIN CONFIGURATION

18 PIN DIP



26/20 PIN SOJ



PIN NAMES

Ai	ADDRESS INPUT
DOUT	DATA OUTPUT
$\overline{DIN}$	DATA INPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
NC	NO CONNECTION
VCC	POWER SUPPLY
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to G_{ND}	−1.0 to + 7.0 V
Operating temperature, t_{OPT} (ambient)	0 to + 70 °C
Storage temperature, t_{STG} (ambient)	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation	1 W

DC CHARACTERISTICS (TA=0 to 70 °C, VCC=5V±10 %)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V	ALL VOLTAGES REFERENCED TO GND
HIGH LEVEL INPUT VOLTAGE	V_{IH}	2.4		5.5	V	
LOW LEVEL INPUT VOLTAGE	V_{IL}	−1.0		0.8	V	
STANDBY CURRENT	I_{CC2}			3.0	mA	RAS=VIH, Dout=HiZ
INPUT LEAKAGE CURRENT	$I_{I(L)}$	−10		10	μA	
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	−10		10	μA	
OUTPUT LOW VOLTAGE	V_{OL}	0		0.4	V	IOL=4.2 mA
OUTPUT HIGH VOLTAGE	V_{OH}	2.4		V_{CC}	V	IOH=−5 mA

CAPACITANCE (TA=25 °C, F=1 MHz)

PARAMETER	SYMBOL	MAX	UNITS
ADDRESS	C_{I1}	6	pF
RAS, CAS, WE	C_{I2}	8	pF
DOUT	C_D	7	pF

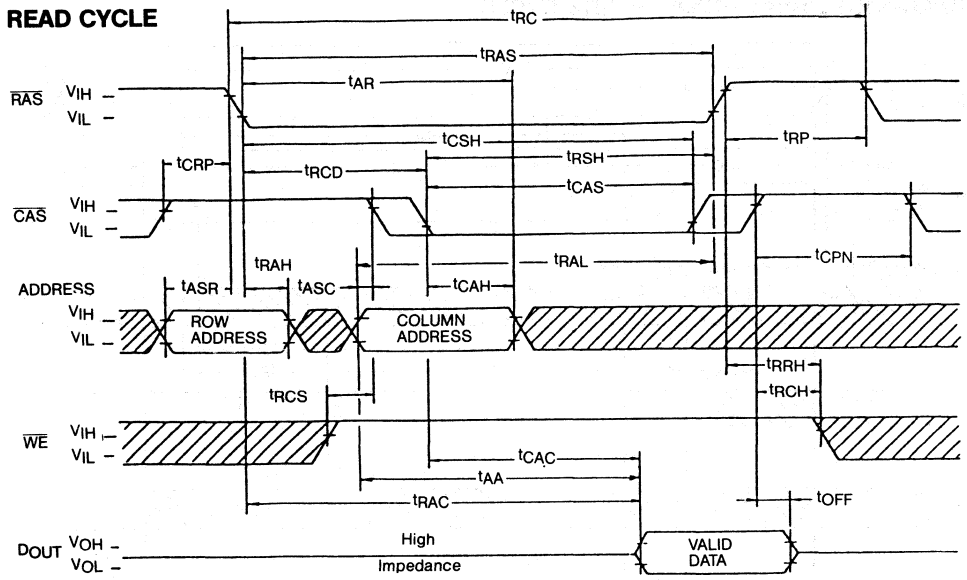
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD421000-8		μPD421000-10		μPD421000-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC OPERATING CURRENT	I_{CC1}		70		60		50	mA
VCC STANDBY CURRENT	I_{CC2}		3		3		3	mA
VCC $\overline{RAS}$ ONLY REFRESH CURRENT	I_{CC3}		60		50		40	mA
VCC CBR REFRESH CURRENT	I_{CC6}		60		50		40	mA
RANDOM READ OR WRITE CYCLE TIME	t_{RC}	170		190		220		ns
READ WRITE CYCLE TIME	t_{RWC}	215		235		265		ns
FAST PAGE MODE CYCLE TIME	t_{PC}	60		70		85		ns
ACCESS TIME FROM $\overline{RAS}$	t_{RAC}		80		100		120	ns
ACCESS TIME FROM $\overline{CAS}$	t_{CAC}		20		25		30	ns
ACCESS TIME FROM COLUMN ADDRESS	t_{AA}		45		55		65	ns
ACCESS TIME FROM $\overline{CAS}$ PRECHARGE	t_{ACP}		55		65		80	ns
OUTPUT BUFFER TURN-OFF DELAY	t_{OFF}	0	20	0	25	0	30	ns
TRANSITION TIME (RISE AND FALL)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ PRECHARGE TIME	t_{RP}	80		80		90		ns
$\overline{RAS}$ PULSE WIDTH	t_{RAS}	80	10000	100	10000	120	10000	ns
$\overline{RAS}$ HOLD TIME	t_{RSH}	20		20		25		ns
$\overline{CAS}$ PULSE WIDTH	t_{CAS}	20	10000	20	10000	25	10000	ns
$\overline{CAS}$ HOLD TIME	t_{CSH}	80		100		120		ns
$\overline{RAS}$ TO $\overline{CAS}$ DELAY TIME	t_{RCD}	20	60	25	75	25	90	ns
$\overline{CAS}$ TO $\overline{RAS}$ PRECHARGE TIME	t_{CRP}	10		10		10		ns
$\overline{CAS}$ PRECHARGE TIME	t_{CPN}	10	30	10	40	15	50	ns
ROW ADDRESS SET-UP TIME	t_{ASR}	0		0		0		ns
ROW ADDRESS HOLD TIME	t_{RAH}	15		15		15		ns
COLUMN ADDRESS SET-UP TIME	t_{ASC}	0	20	0	30	0	35	ns
COLUMN ADDRESS HOLD TIME	t_{CAH}	20		20		25		ns
COLUMN ADDRESS HOLD TIME REFERENCED TO $\overline{RAS}$	t_{AR}	60		70		85		ns

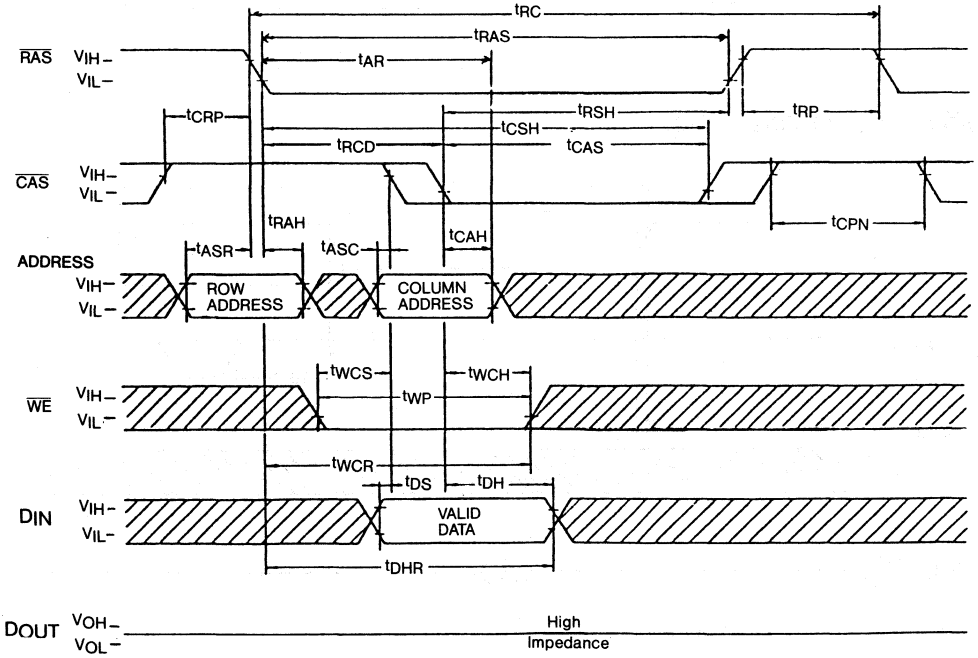
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD421000-8		μPD421000-10		μPD421000-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
COLUMN ADDRESS TO $\overline{RAS}$ LEAD TIME	t_{RAL}	45		55		65		ns
READ COMMAND SET-UP TIME	t_{RCS}	0		0		0		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{RRH}	10		10		10		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{CAS}$	t_{RCH}	0		0		0		ns
WRITE COMMAND HOLD TIME	t_{WCH}	20		20		25		ns
WRITE COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{WCR}	60		70		85		ns
WRITE COMMAND PULSE WIDTH	t_{WP}	20		20		25		ns
WRITE COMMAND TO $\overline{RAS}$ LEAD TIME	t_{RWL}	40		40		45		ns
WRITE COMMAND TO $\overline{CAS}$ LEAD TIME	t_{CWL}	20		20		25		ns
DATA-IN SET-UP TIME	t_{DS}	0		0		0		ns
DATA-IN HOLD TIME	t_{DH}	20		20		25		ns
DATA-IN HOLD TIME REFERENCED TO $\overline{RAS}$	t_{DHR}	60		70		85		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{WCS}	0		0		0		ns
$\overline{CAS}$ TO $\overline{WE}$ DELAY	t_{CWD}	20		20		25		ns
$\overline{RAS}$ TO $\overline{WE}$ DELAY	t_{RWD}	80		100		120		ns
COLUMN ADDRESS TO $\overline{WE}$ DELAY	t_{AWD}	45		55		65		ns
$\overline{CAS}$ SET-UP TIME FOR CBR REFRESH	t_{CSR}	10		10		10		ns
$\overline{CAS}$ HOLD TIME FOR CBR REFRESH	t_{CHR}	20		20		25		ns
$\overline{RAS}$ PRECHARGE $\overline{CAS}$ HOLD TIME	t_{RPC}	0		0		0		ns
REFRESH PERIOD	t_{REF}		8		8		8	ms

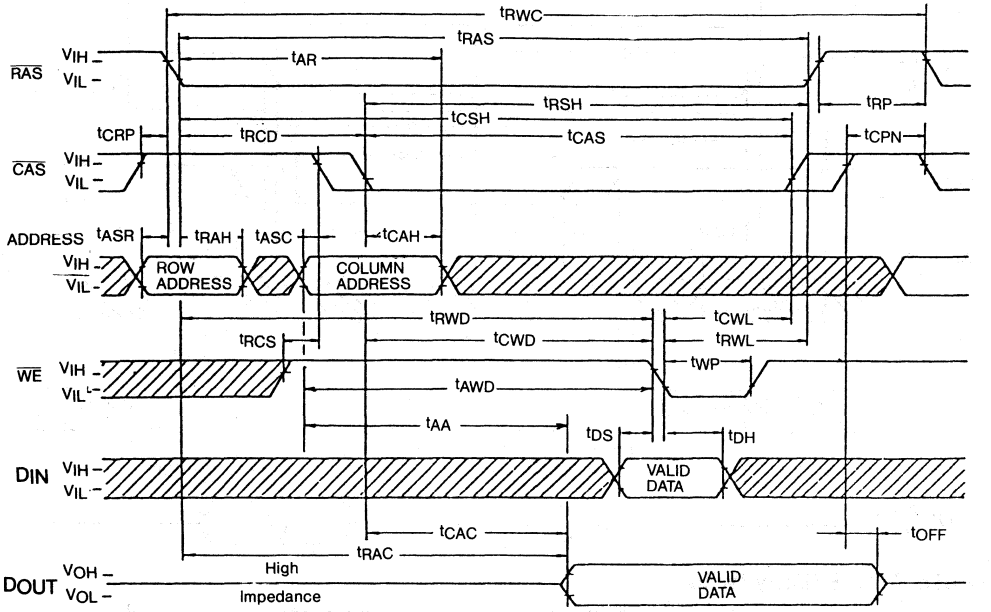
READ CYCLE



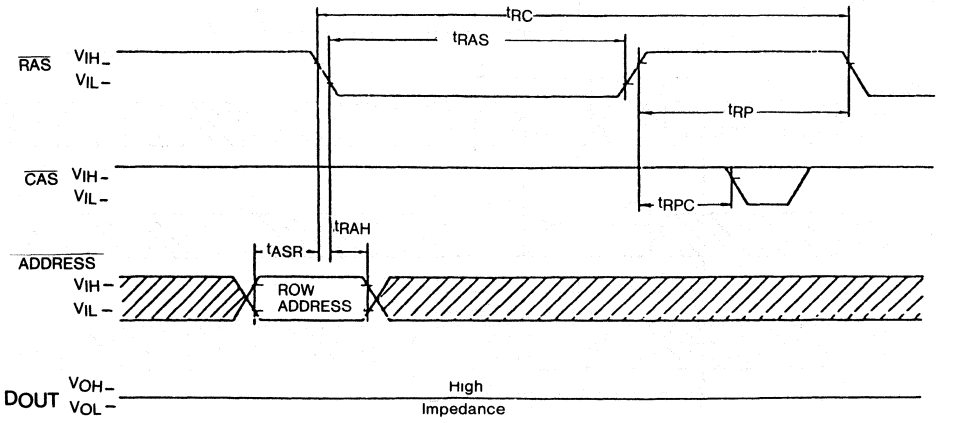
WRITE CYCLE (Early Write)



READ-WRITE/READ-MODIFY-WRITE CYCLE

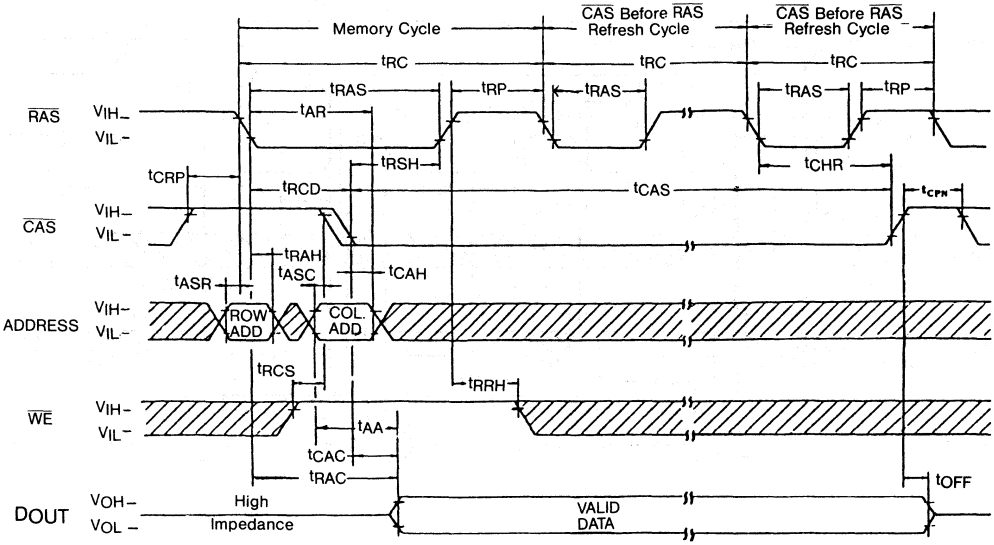


RAS ONLY REFRESH CYCLE

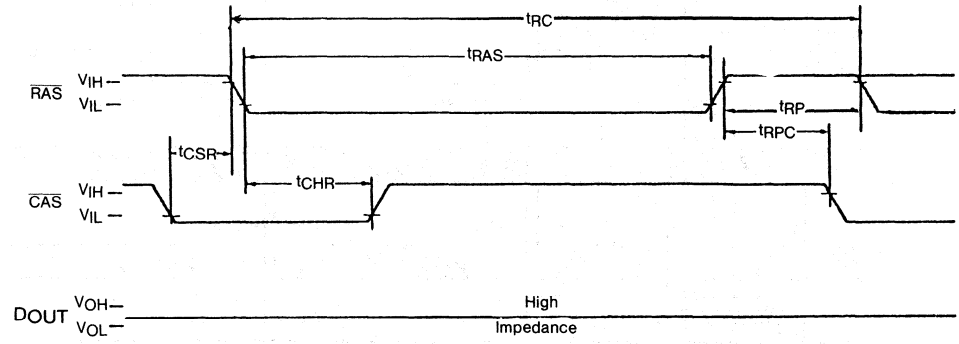


WE = Don't Care

HIDDEN REFRESH CYCLE

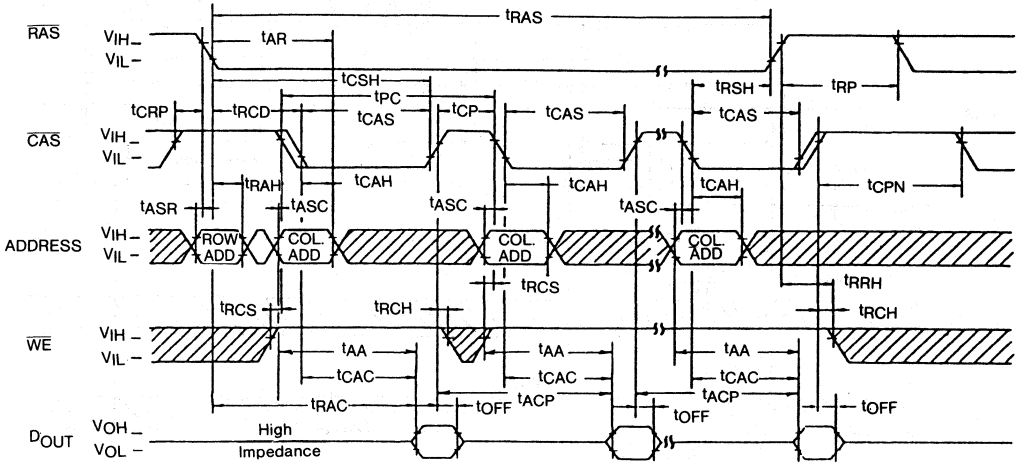


CAS BEFORE RAS REFRESH

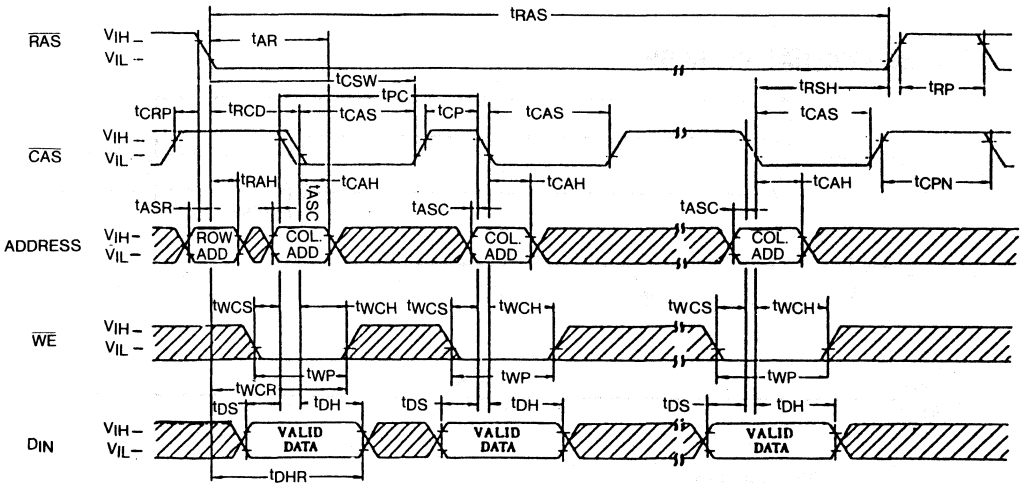


WE, ADDRESS: Don't Care

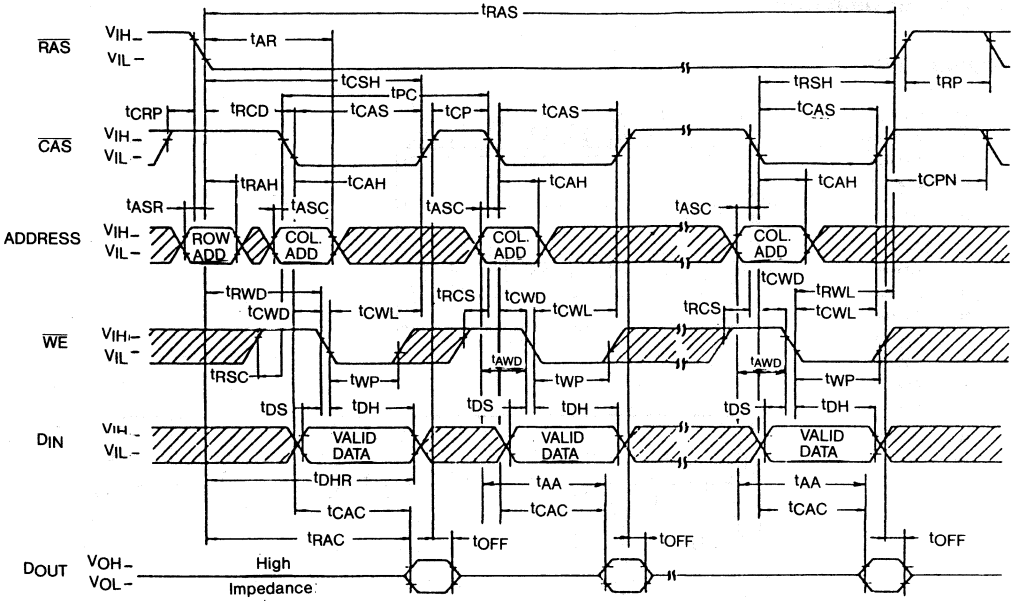
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



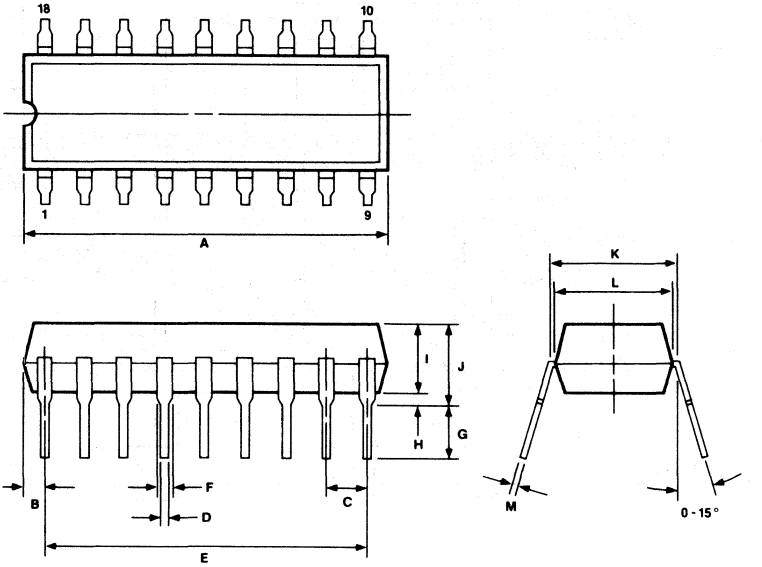
FAST PAGE MODE WRITE CYCLE (Early Write)



PACKAGE DIMENSIONS

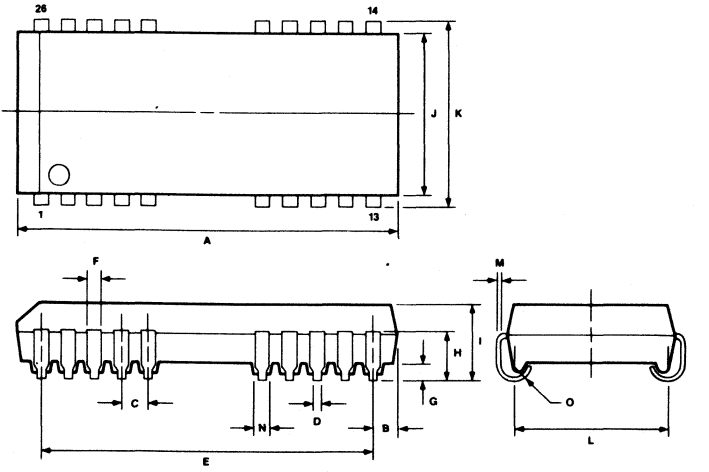
Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



Plastic SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.80
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



μPD421001 (NIBBLE)

1.048.576W x 1 BIT DRAM

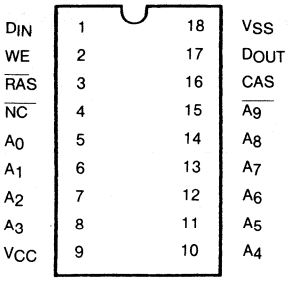
FEATURES

- 1.048.576 words by 1 bit organization
- low power dissipation CMOS DRAM
- single 5 V ± 10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- 512 cycle, 8ms refresh
- High density 18-pin plastic DIP (μPD421001C) or 26/20-pin plastic SOJ (μPD421001LA)
- 4-Bit nibble mode

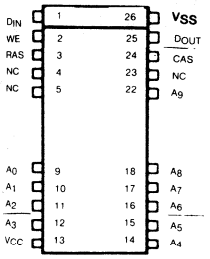
FAMILY	TRAC	TCAC	TNAC	ICC1
μPD421001 - 8	80 ns	20 ns	20 ns	70 mA
μPD421001 - 10	100 ns	25 ns	20 ns	60 mA
μPD421001 - 12	120 ns	30 ns	25 ns	50 mA

PIN CONFIGURATION

18 PIN DIP



26/20 PIN SOJ



PIN NAMES

Ai	ADDRESS INPUT
DOUT	DATA OUTPUT
DIN	DATA INPUT
RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
NC	NO CONNECTION
VCC	POWER SUPPLY
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to G_{ND}	−1.0 to + 7.0 V
Operating temperature, t_{OPT} (ambient)	0 to + 70 °C
Storage temperature, t_{STG} (ambient)	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation	1 W

DC CHARACTERISTICS (TA=0 to 70 °C, VCC=5V±10 %)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V	ALL VOLTAGES REFERENCED TO GND
HIGH LEVEL INPUT VOLTAGE	V_{IH}	2.4		5.5	V	
LOW LEVEL INPUT VOLTAGE	V_{IL}	−1.0		0.8	V	
STANDBY CURRENT	I_{CC2}			3.0	mA	RAS=VIH, Dout=HiZ
INPUT LEAKAGE CURRENT	$I_{I(L)}$	−10		10	μA	
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	−10		10	μA	
OUTPUT LOW VOLTAGE	V_{OL}	0		0.4	V	IOL=4.2 mA
OUTPUT HIGH VOLTAGE	V_{OH}	2.4		V_{CC}	V	IOH=−5 mA

CAPACITANCE (TA=25 °C, F=1 MHz)

PARAMETER	SYMBOL	MAX	UNITS
ADDRESS	C_{I1}	6	pF
RAS, CAS, WE	C_{I2}	8	pF
DOUT	C_D	7	pF

AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYM-BOL	μPD421001 - 8		μPD421001 - 10		μPD421001 - 12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC OPERATING CURRENT	I_{CC1}		70		60		50	mA
VCC STANDBY CURRENT	I_{CC2}		3		3		3	mA
VCC $\overline{RAS}$ ONLY REFRESH CURRENT	I_{CC3}		60		50		40	mA
VCC CBR REFRESH CURRENT	I_{CC6}		60		50		40	mA
RANDOM READ OR WRITE CYCLE TIME	t_{RC}	170		190		220		ns
READ WRITE CYCLE TIME	t_{RWC}	215		235		265		ns
ACCESS TIME FROM $\overline{RAS}$	t_{RAC}		80		100		120	ns
ACCESS TIME FROM $\overline{CAS}$	t_{CAC}		20		25		30	ns
ACCESS TIME FROM COLUMN ADDRESS	t_{AA}		45		55		65	ns
OUTPUT BUFFER TURN-OFF DELAY	t_{OFF}	0	20	0	25	0	30	ns
TRANSITION TIME (RISE AND FALL)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ PRECHARGE TIME	t_{RP}	80		80		90		ns
$\overline{RAS}$ PULSE WIDTH	t_{RAS}	80	10000	100	10000	120	10000	ns
$\overline{RAS}$ HOLD TIME	t_{RSH}	20		20		25		ns
$\overline{CA}$ PULSE WIDTH	t_{CAS}	20	10000	20	10000	25	10000	ns
$\overline{CAS}$ HOLD TIME	t_{CSH}	80		100		120		ns
$\overline{RAS}$ TO $\overline{CAS}$ DELAY TIME	t_{RCD}	20	60	25	75	25	90	ns
$\overline{CAS}$ TO $\overline{RAS}$ PRECHARGE TIME	t_{CRP}	10		10		10		ns
$\overline{CAS}$ PRECHARGE TIME	t_{CPN}	10		10		15		ns
ROW ADDRESS SET-UP TIME	t_{ASR}	0		0		0		ns
ROW ADDRESS HOLD TIME	t_{RAH}	15		15		15		ns
COLUMN ADDRESS SET-UP TIME	t_{ASC}	0	20	0	30	0	35	ns
COLUMN ADDRESS HOLD TIME	t_{CAH}	20		20		25		ns
COLUMN ADDRESS HOLD TIME REFERENCED TO $\overline{RAS}$	t_{AR}	60		70		85		ns
COLUMN ADDRESS TO $\overline{RAS}$ LEAD TIME	t_{RAL}	45		55		65		ns
READ COMMAND SET-UP TIME	t_{RCS}	0		0		0		ns

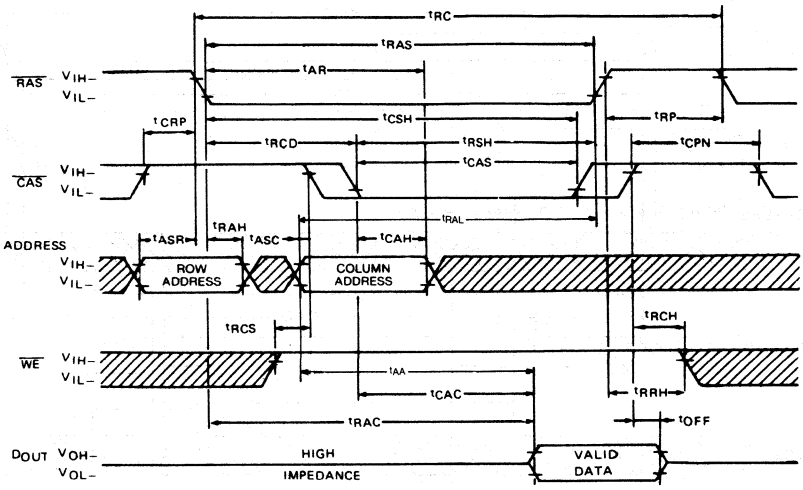
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD421001-8		μPD421001-10		μPD421001-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{RRH}	10		10		10		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{CAS}$	t_{RCH}	0		0		0		ns
WRITE COMMAND HOLD TIME	t_{WCH}	20		20		25		ns
WRITE COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{WCR}	60		70		85		ns
WRITE COMMAND PULSE WIDTH	t_{WP}	20		20		25		ns
WRITE COMMAND TO $\overline{RAS}$ LEAD TIME	t_{RWL}	40		40		45		ns
WRITE COMMAND TO $\overline{CAS}$ LEAD TIME	t_{CWL}	20		20		25		ns
DATA-IN SET-UP TIME	t_{DS}	0		0		0		ns
DATA-IN HOLD TIME	t_{DH}	20		20		25		ns
DATA-IN HOLD TIME REFERENCED TO $\overline{RAS}$	t_{DHR}	60		70		85		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{WCS}	0		0		0		ns
$\overline{CAS}$ TO $\overline{WE}$ DELAY	t_{CWD}	20		20		25		ns
$\overline{RAS}$ TO $\overline{WE}$ DELAY	t_{RWD}	80		100		120		ns
COLUMN ADDRESS TO $\overline{WE}$ DELAY	t_{AWD}	45		55		65		ns
$\overline{CAS}$ SET-UP TIME FOR CBR REFRESH	t_{CSR}	10		10		10		ns
$\overline{CAS}$ HOLD TIME FOR CBR REFRESH	t_{CHR}	20		20		25		ns
$\overline{RAS}$ PRECHARGE $\overline{CAS}$ HOLD TIME	t_{RPC}	0		0		0		ns
REFRESH PERIOD	t_{REF}		8		8		8	ms

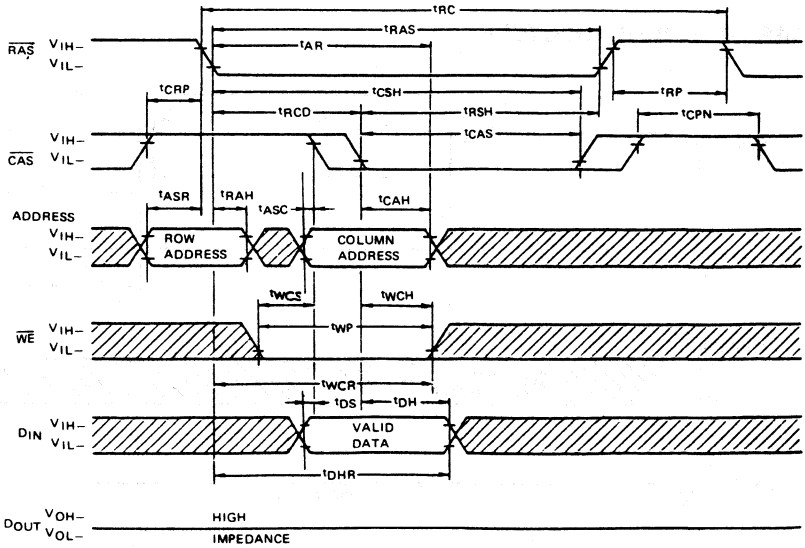
AC CHARACTERISTICS (NIBBLE MODE)

VCC NIBBLE CURRENT	I_{CC5}		50		40		30	mA
NIBBLE CYCLE TIME	t_{NC}	45		45		50		ns
NIBBLE ACCESS TIME	t_{NAC}		20		20		25	ns
$\overline{CAS}$ PRECHARGE TIME	t_{NP}	15		15		15		ns
$\overline{CAS}$ SET-UP TIME	t_{NAS}	20		20		25		ns
$\overline{RAS}$ HOLD TIME (READ CYCLE)	t_{NRSH}	20		20		25		ns
$\overline{CAS}$ TO $\overline{WE}$ DELAY TIME	t_{NCWD}	20		20		25		ns
$\overline{WE}$ COMMAND TO $\overline{CAS}$ LEAD TIME	t_{NCWL}	20		20		25		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{NWCS}	20		20		25		ns

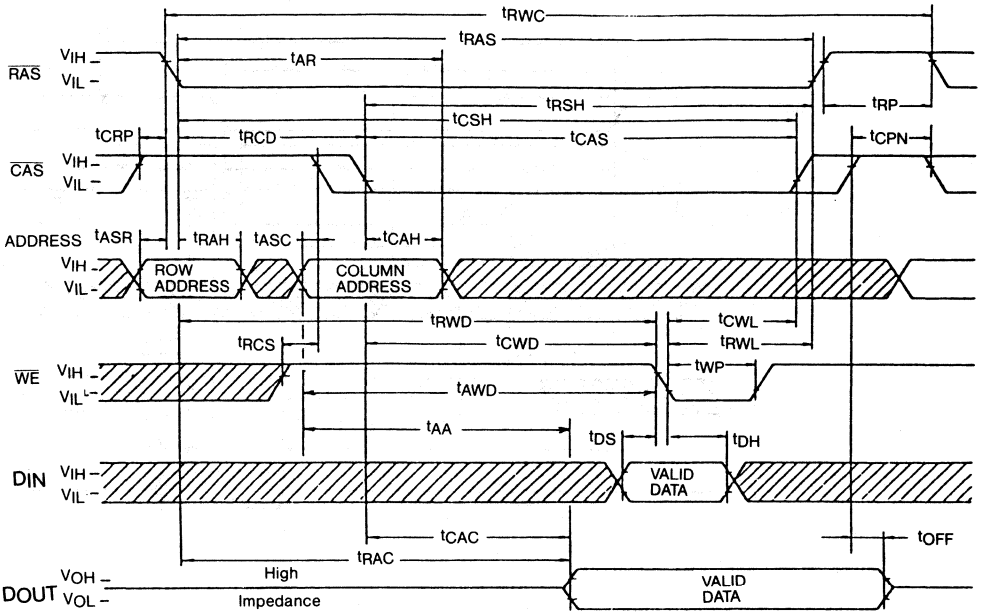
READ CYCLE



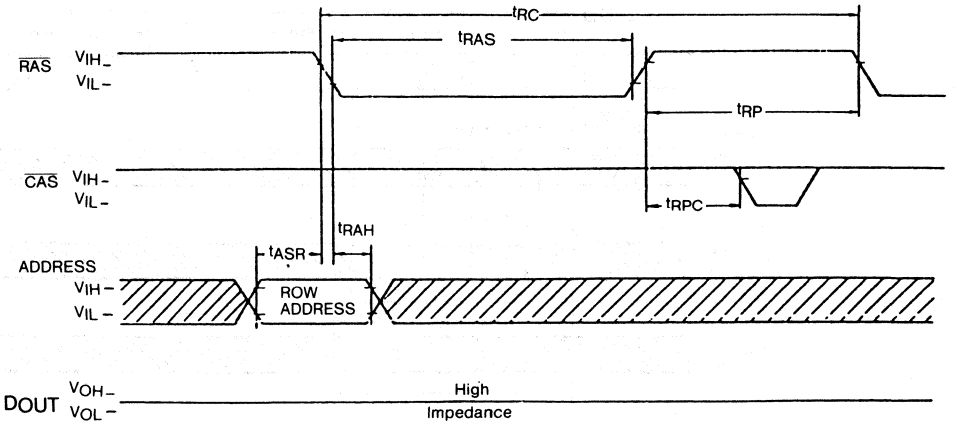
WRITE CYCLE
(Early Write)



READ-WRITE/READ-MODIFY-WRITE CYCLE

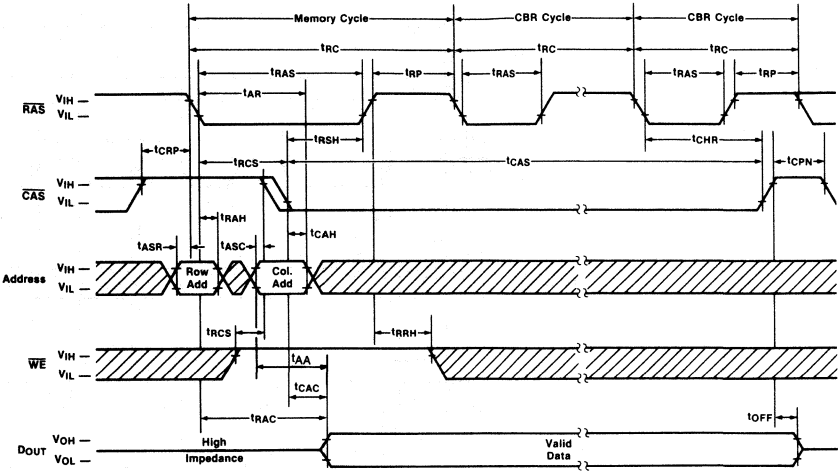


RAS ONLY REFRESH CYCLE

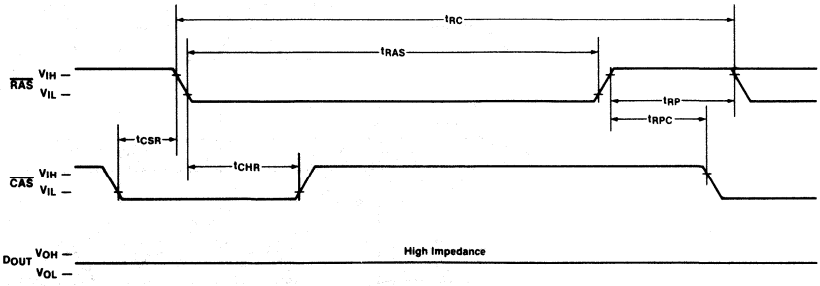


WE = Don't Care

HIDDEN REFRESH CYCLE

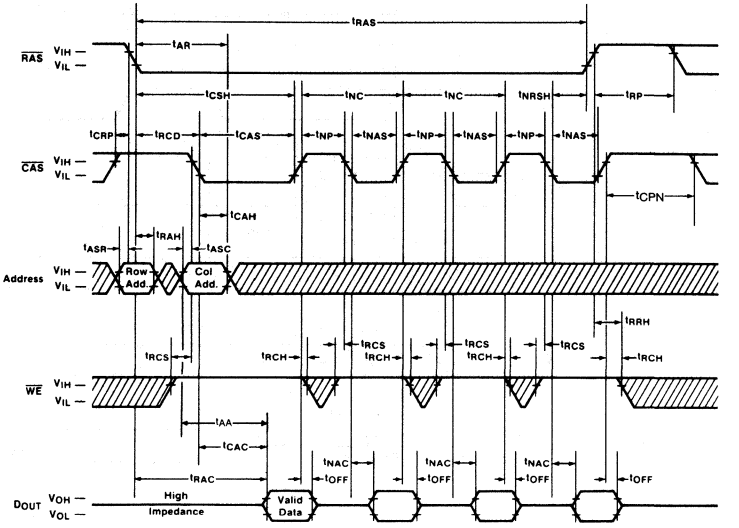


CAS BEFORE RAS REFRESH CYCLE

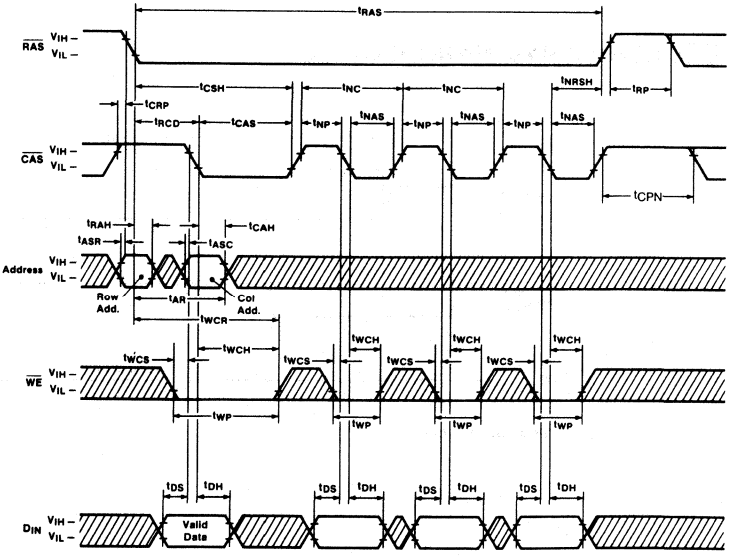


WE, Address: Don't Care.

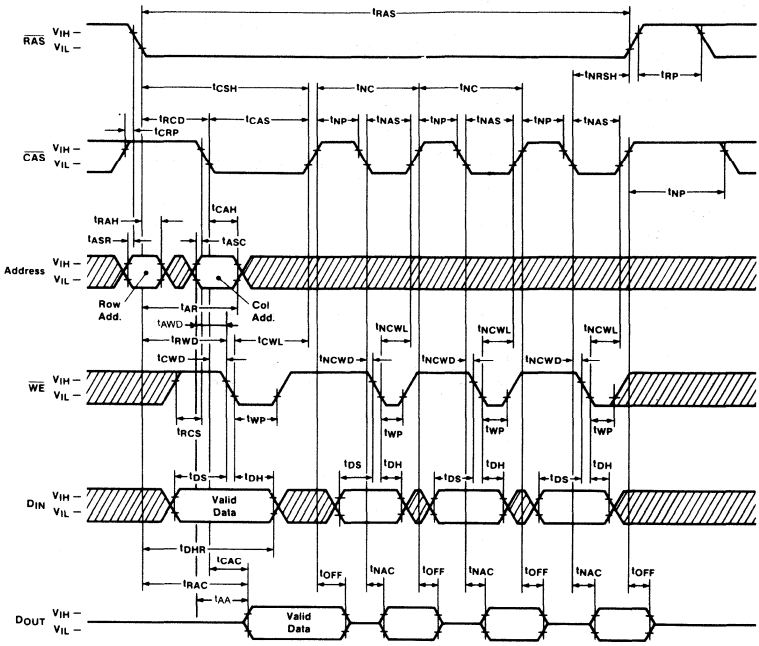
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)



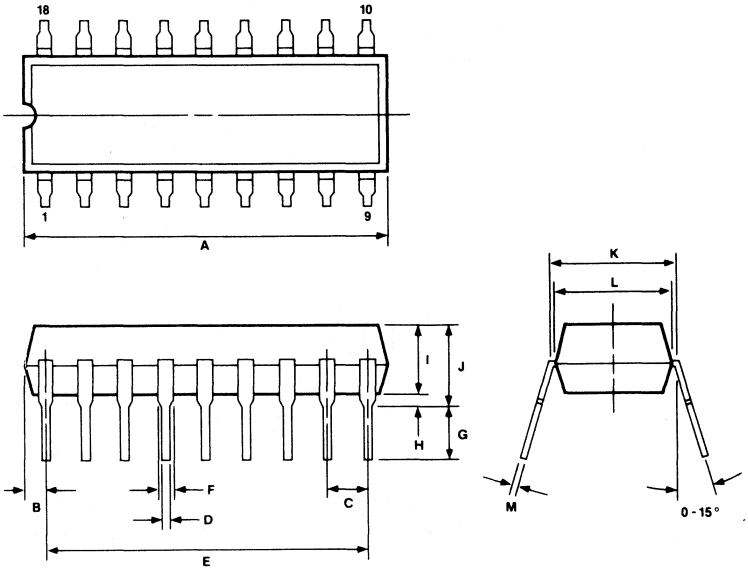
NIBBLE MODE READ-WRITE / READ-MODIFY-WRITE CYCLE



PACKAGE DIMENSIONS

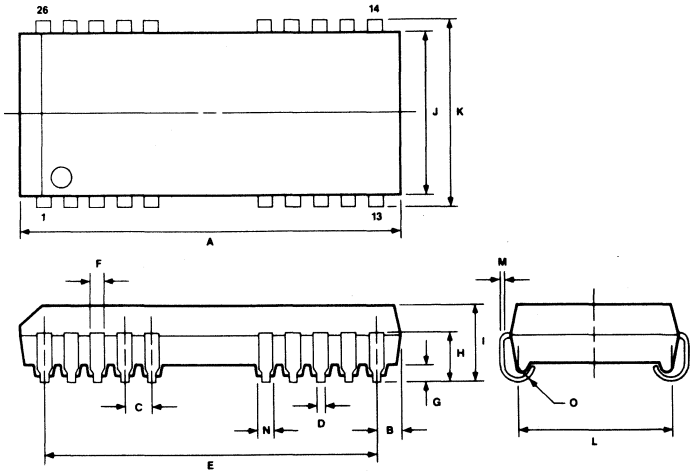
PLASTIC DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



PLASTIC SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



μPD421002 (STATIC COLUMN)

1.048.576W x 1 BIT DRAM

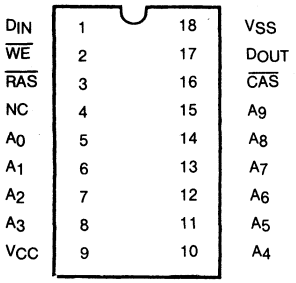
FEATURES

- 1.048.576 words by 1 bit organization
- low power dissipation CMOS DRAM
- single 5 V ± 10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- 512 cycle, 8 ms refresh
- High density 18-pin plastic DIP (μPD421002C) or 26/20-pin plastic SOJ (μPD421002LA)
- Static Column mode

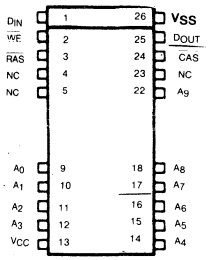
FAMILY	TRAC	TCAC	TAA	ICC1
μPD421002 - 8	80 ns	20 ns	45 ns	70 mA
μPD421002 - 10	100 ns	25 ns	55 ns	60 mA
μPD421002 - 12	120 ns	30 ns	65 ns	50 mA

PIN CONFIGURATION

18 PIN DIP



26/20 PIN SOJ



PIN NAMES

Ai	ADDRESS INPUT
DOUT	DATA OUTPUT
DIN	DATA INPUT
RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
NC	NO CONNECTION
VCC	POWER SUPPLY
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to G_{ND}	−1.0 to + 7.0 V
Operating temperature, t_{OPT} (ambient)	0 to + 70 °C
Storage temperature, t_{STG} (ambient)	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation	1 W

DC CHARACTERISTICS (TA=0 to 70 °C, VCC=5V±10 %)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V	ALL VOLTAGES REFERENCED TO GND
HIGH LEVEL INPUT VOLTAGE	V_{IH}	2.4		5.5	V	
LOW LEVEL INPUT VOLTAGE	V_{IL}	−1.0		0.8	V	
STANDBY CURRENT	I_{CC2}			3.0	mA	RAS=VIH, Dout=HiZ
INPUT LEAKAGE CURRENT	$I_{I(L)}$	−10		10	μA	
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	−10		10	μA	
OUTPUT LOW VOLTAGE	V_{OL}	0		0.4	V	IOL=4.2 mA
OUTPUT HIGH VOLTAGE	V_{OH}	2.4		V_{CC}	V	IOH=−5 mA

CAPACITANCE (TA=25 °C, F=1 MHz)

PARAMETER	SYMBOL	MAX	UNITS
ADDRESS	C_{I1}	6	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	8	pF
DOUT	C_D	7	pF

AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5 V ± 10 %)

PARAMETER	SYMBOL	μPD421002-8		μPD421002-10		μPD421002-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC OPERATING CURRENT	I_{CC1}		70		60		50	mA
VCC STANDBY CURRENT	I_{CC2}		3		3		3	mA
VCC $\overline{RAS}$ ONLY REFRESH CURRENT	I_{CC3}		60		50		40	mA
VCC CBR REFRESH CURRENT	I_{CC6}		60		50		40	mA
RANDOM READ OR WRITE CYCLE TIME	t_{RC}	170		190		220		ns
READ WRITE CYCLE TIME	t_{RWC}	215		235		265		ns
ACCESS TIME FROM $\overline{RAS}$	t_{RAC}		80		100		120	ns
ACCESS TIME FROM $\overline{CAS}$	t_{CAC}		20		25		30	ns
ACCESS TIME FROM COLUMN ADDRESS	t_{AA}		45		55		65	ns
OUTPUT BUFFER TURN-OFF DELAY	t_{OFF}	0	20	0	25	0	30	ns
TRANSITION TIME (RISE AND FALL)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ PRECHARGE TIME	t_{RP}	80		80		90		ns
$\overline{RAS}$ PULSE WIDTH	t_{RAS}	80	10000	100	10000	120	10000	ns
$\overline{RAS}$ HOLD TIME	t_{RSH}	20		20		25		ns
$\overline{CAS}$ PULSE WIDTH	t_{CAS}	20	10000	20	10000	25	10000	ns
$\overline{CAS}$ HOLD TIME	t_{CSH}	80		100		120		ns
$\overline{RAS}$ TO $\overline{CAS}$ DELAY TIME	t_{RCD}	20	60	25	75	25	90	ns
$\overline{RAS}$ TO COLUMN ADDRESS DELAY TIME	t_{RAD}	20	35	20	45	20	55	ns
$\overline{CAS}$ TO $\overline{RAS}$ PRECHARGE TIME	t_{CRP}	10		10		10		ns
$\overline{CAS}$ PRECHARGE TIME	t_{CP}	10		10		15		ns
ROW ADDRESS SET-UP TIME	t_{ASR}	0		0		0		ns
ROW ADDRESS HOLD TIME	t_{RAH}	15		15		15		ns
COLUMN ADDRESS SET-UP TIME	t_{ASC}	0	20	0	30	0	35	ns
COLUMN ADDRESS HOLD TIME	t_{CAH}	20		20		25		ns
COLUMN ADDRESS HOLD TIME REFERENCED TO $\overline{RAS}$	t_{AR}	80		100		120		ns

AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

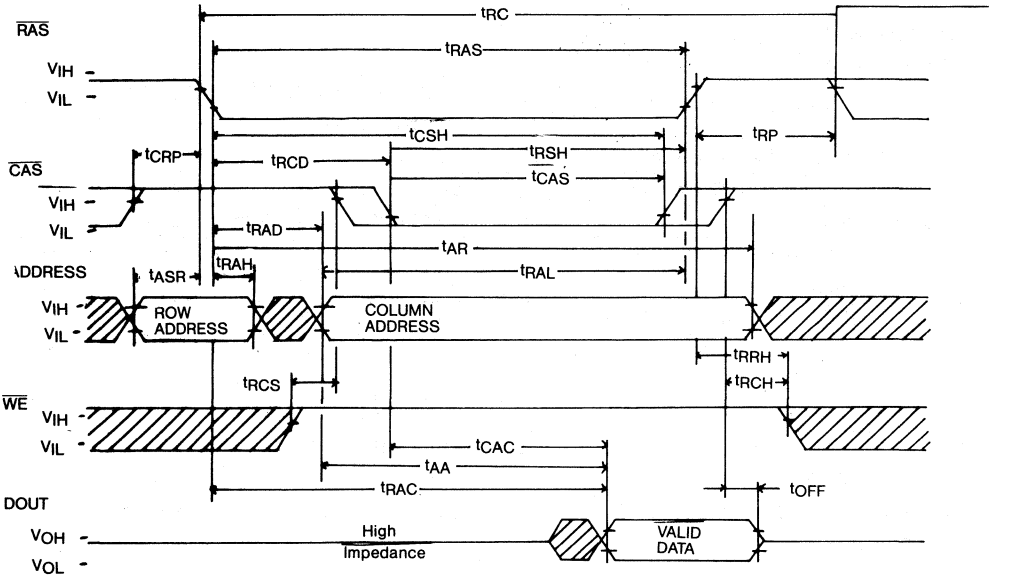
PARAMETER	SYMBOL	μPD421002-8		μPD421002-10		μPD421002-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{RAS}$ TO COLUMN ADDRESS HOLD TIME	t_{AH}	15		15		15		ns
COLUMN ADDRESS TO $\overline{RAS}$ LEAD TIME	t_{RAL}	45		55		65		ns
READ COMMAND SET-UP TIME	t_{RCS}	0		0		0		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{RRH}	10		10		10		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{CAS}$	t_{RCH}	0		0		0		ns
COLUMN ADDRESS HOLD TIME TO $\overline{RAS}$ ON WRITE	t_{AWR}	60		70		85		ns
WRITE COMMAND HOLD TIME	t_{WCH}	20		20		25		ns
WRITE COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{WCR}	60		70		85		ns
WRITE COMMAND PULSE WIDTH	t_{WP}	20		20		25		ns
WRITE COMMAND TO $\overline{RAS}$ LEAD TIME	t_{RWL}	40		40		45		ns
WRITE COMMAND TO $\overline{CAS}$ LEAD TIME	t_{CWL}	20		20		25		ns
DATA-IN SET-UP TIME	t_{DS}	0		0		0		ns
DATA-IN HOLD TIME	t_{DH}	20		20		25		ns
DATA-IN HOLD TIME REFERENCED TO $\overline{RAS}$	t_{DHR}	60		70		85		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{WCS}	0		0		0		ns
$\overline{CAS}$ TO $\overline{WE}$ DELAY	t_{CWD}	20		20		25		ns
$\overline{RAS}$ TO $\overline{WE}$ DELAY	t_{RWD}	80		100		120		ns
COLUMN ADDRESS TO $\overline{WE}$ DELAY	t_{AWD}	45		55		65		ns
OUTPUT HOLD TIME FROM $\overline{WE}$	t_{OHW}	10		10		10		ns
$\overline{CAS}$ SET-UP TIME FOR CBR REFRESH	t_{CSR}	10		10		10		ns
$\overline{CAS}$ HOLD TIME FOR CBR REFRESH	t_{CHR}	20		20		25		ns
$\overline{RAS}$ PRECHARGE $\overline{CAS}$ HOLD TIME	t_{RPC}	0		0		0		ns
REFRESH PERIOD	t_{REF}		8		8		8	ms

STATIC COLUMN MODE

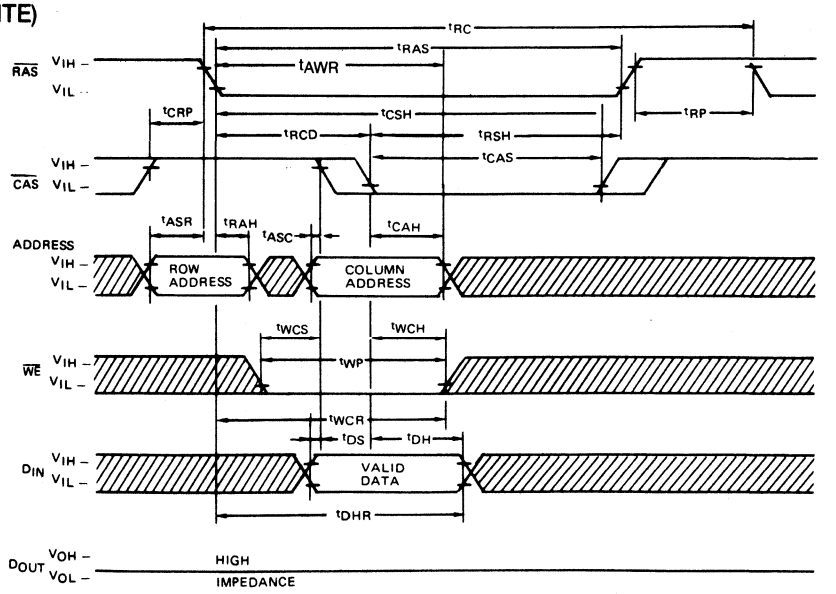
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD421002-8		μPD421002-10		μPD421002-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SC MODE CYCLE TIME ON READ	t_{RSC}	50		60		70		ns
SC MODE CYCLE TIME ON WRITE	t_{WSC}	50		60		70		ns
SC MODE $\overline{RAS}$ PULSE WIDTH	t_{RASC}	80	140000	100	140000	120	140000	ns
$\overline{RAS}$ TO SECOND $\overline{WE}$ DELAY TIME	t_{RSW}	85		105		125		ns
WRITE INVALID TIME	t_{WI}	10		10		10		ns
OUTPUT HOLD TIME FROM ADDRESS	t_{OH}	5		5		5		ns
SC MODE CYCLE TIME ON READ-WRITE	t_{RWSC}	95		115		135		ns
ACCESS TIME FROM PREVIOUS $\overline{WE}$	t_{PWA}		90		110		130	ns
PREVIOUS $\overline{WE}$ TO COLUMN ADDRESS DELAY TIME	t_{WAD}	25	45	25	55	30	65	ns
COLUMN ADDRESS HOLD TIME TO PREVIOUS $\overline{WE}$	t_{PWH}	90		110		130		ns

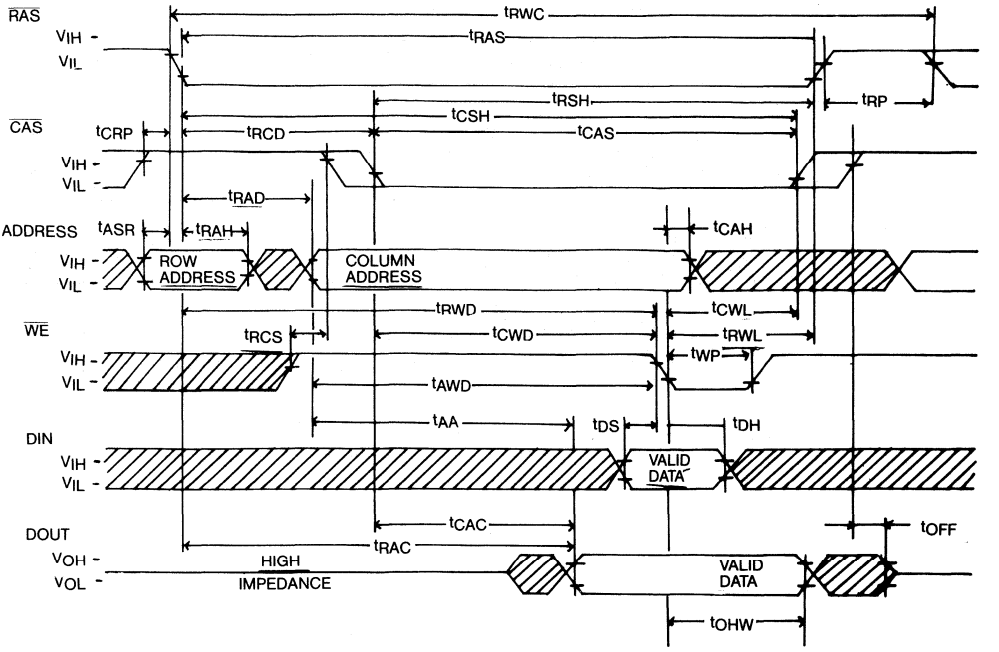
READ CYCLE



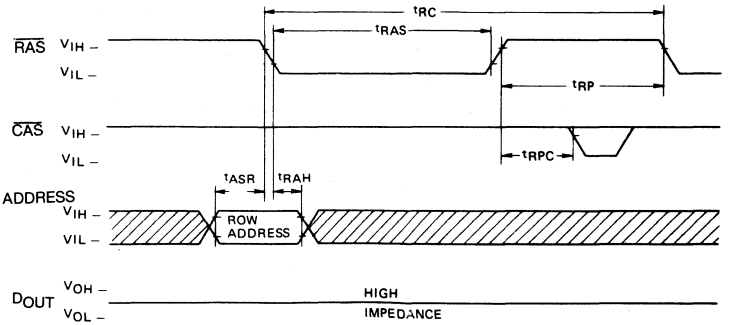
WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

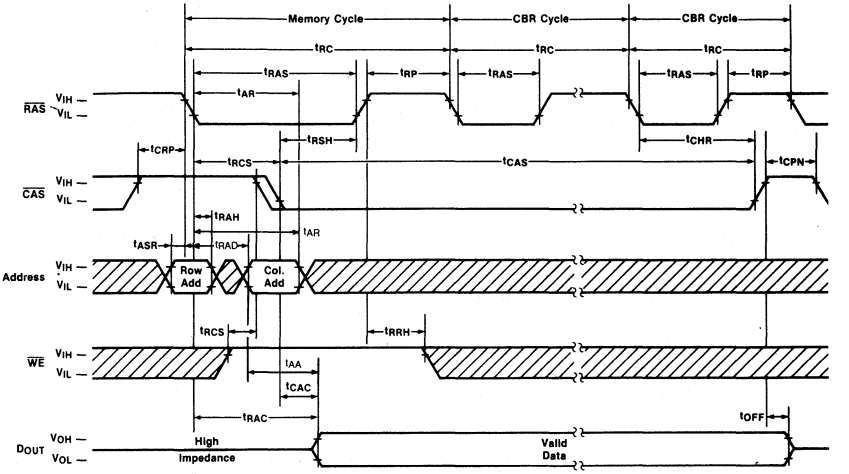


„RAS ONLY" REFRESH CYCLE

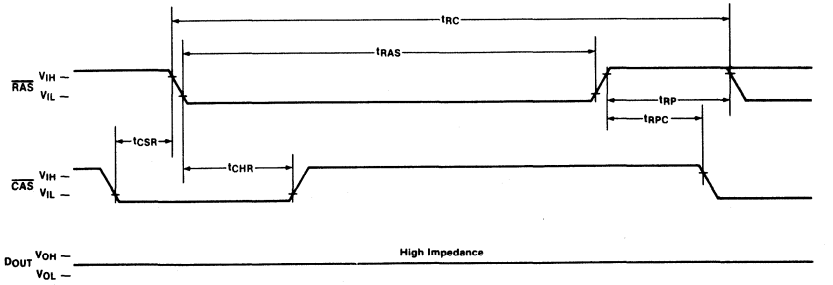


WE = Don't Care

HIDDEN REFRESH CYCLE

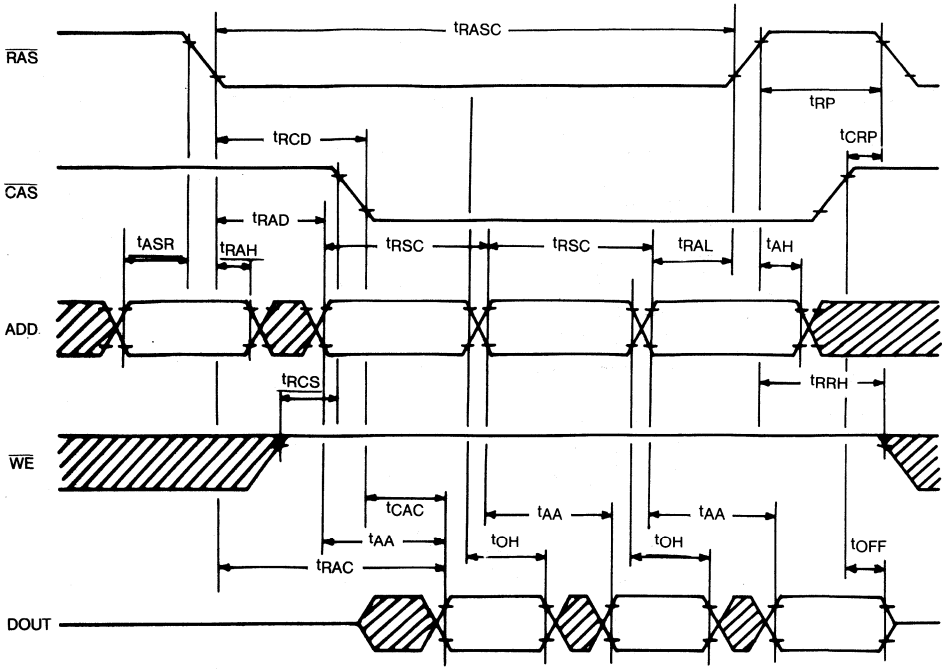


CAS BEFORE RAS REFRESH CYCLE.

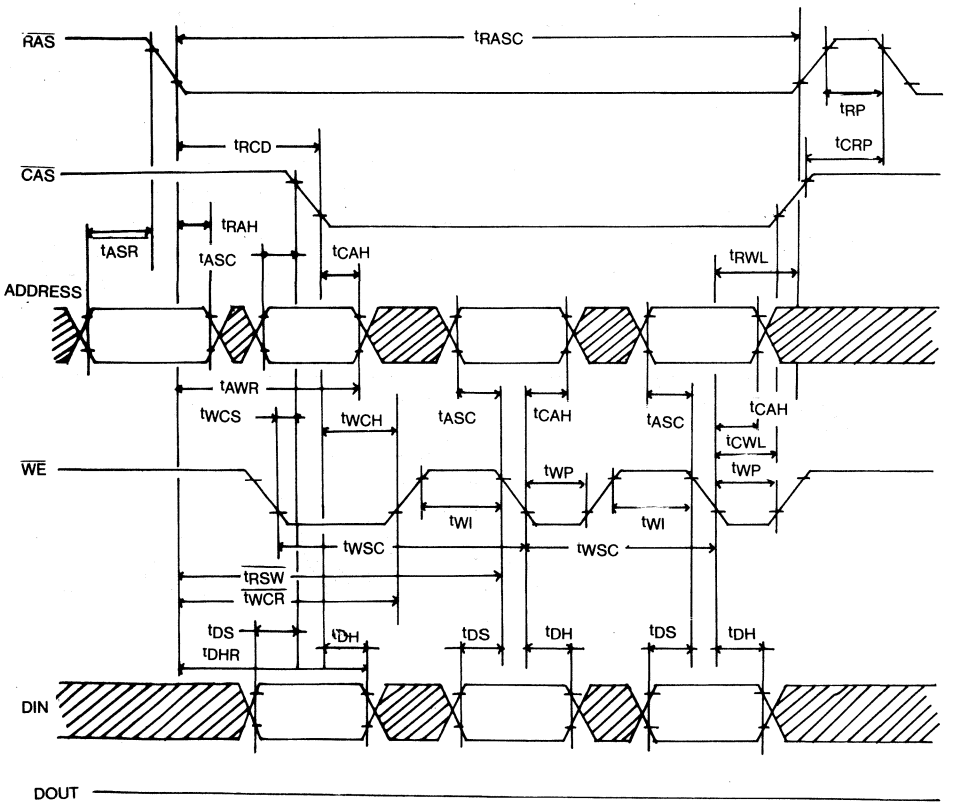


WE, Address: Don't Care.

STATIC COLUMN MODE READ CYCLE



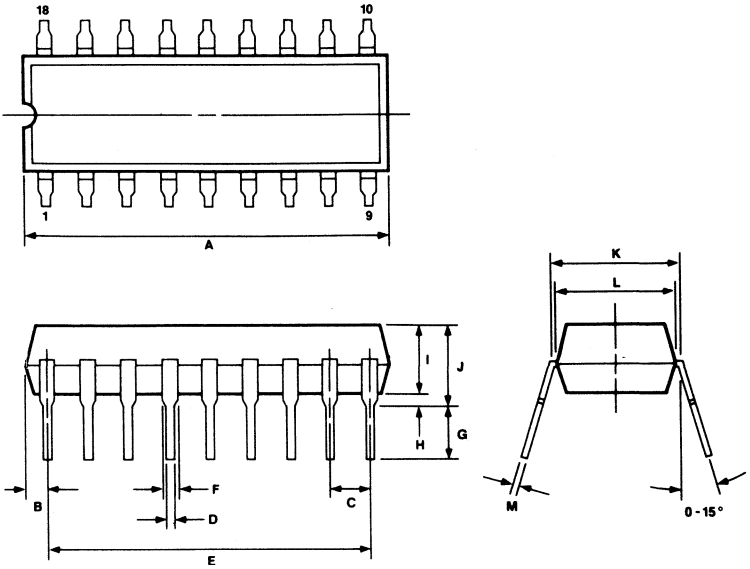
STATIC COLUMN MODE WRITE CYCLE



PACKAGE DIMENSIONS

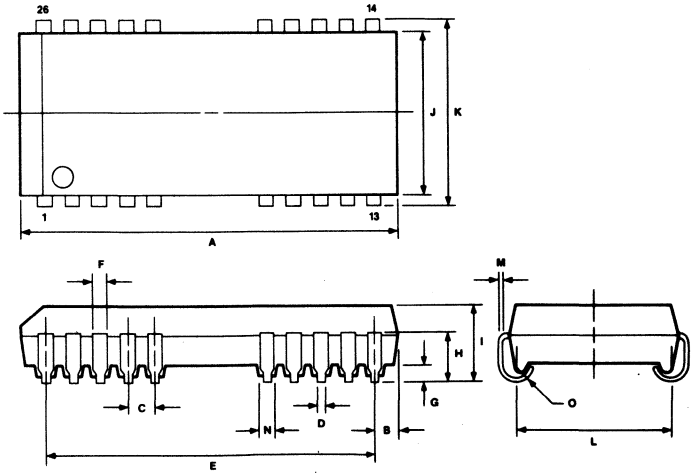
PLASTIC DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.35
M	$.25^{+.10}_{-.05}$



PLASTIC SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



μPD424256 (FAST PAGE)
262.144 W x 4 BIT DRAM

FEATURES

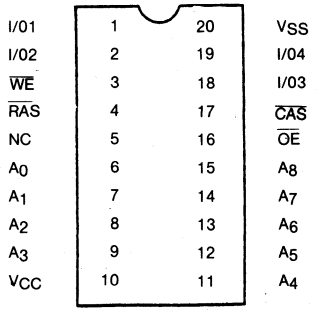
- 262.144 words by 4 bit organization
- I ow power dissipation CMOS DRAM
- Single 5 V ± 10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- 512 cycle, 8 ms refresh
- High density 20-pin plastic DIP (μPD424256C) or 26/20-pin plastic SOJ (μPD424256LA)
- Fast page mode

FAMILY	TRAC	TCAC	TAA	ICC1
μPD424256 - 8	80 ns	20 ns	45 ns	70 mA
μPD424256 - 10	100 ns	25 ns	55 ns	60 mA
μPD424256 - 12	120 ns	30 ns	65 ns	50 mA

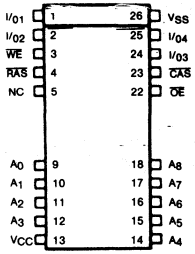
* tCAC = tOEA

PIN CONFIGURATION

20 PIN DIP



26/20 PIN SOJ



Ai	ADDRESS INPUT
I/0i	DATA INPUT/OUTPUT
$\overline{CAS}$	COLUMN ADDRESS STROBE
RAS	ROW ADDRESS STROBE
$\overline{OE}$	OUTPUT ENABLE
WE	WRITE ENABLE
NC	NO CONNECTION
VCC	POWER SUPPLY
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to G_{ND}	−1.0 to + 7.0 V
Operating temperature, t_{OPT} (ambient)	0to + 70 °C
Storage temperature, t_{STG} (ambient)	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation	1 W

DC CHARACTERISTICS (TA=0 to 70 °C, VCC=5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V	ALL VOLTAGES REFERENCED TO GND
HIGH LEVEL INPUT VOLTAGE	V_{IH}	2.4		5.5	V	
LOW LEVEL INPUT VOLTAGE	V_{IL}	−1.0		0.8	V	
STANDBY CURRENT	I_{CC2}			3.0	mA	$\overline{RAS}=\overline{CS}=VIH$
				1.0	mA	$\overline{RAS}=\overline{CAS}$ =VCC−0.2 V
INPUT LEAKAGE CURRENT	$I_{I(L)}$	−10		10	μA	
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	−10		10	μA	
OUTPUT LOW VOLTAGE	V_{OL}	0		0.4	V	IOL=4.2 mA
OUTPUT HIGH VOLTAGE	V_{OH}	2.4		V_{CC}		IOH=−5 mA

CAPACITANCE (TA=25 °C, F=1 MHz)

PARAMETER	SYMBOL	MAX	UNITS
ADDRESS	C_{I1}	6	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	8	pF
INPUT/OUTPUT	C_D	7	pF

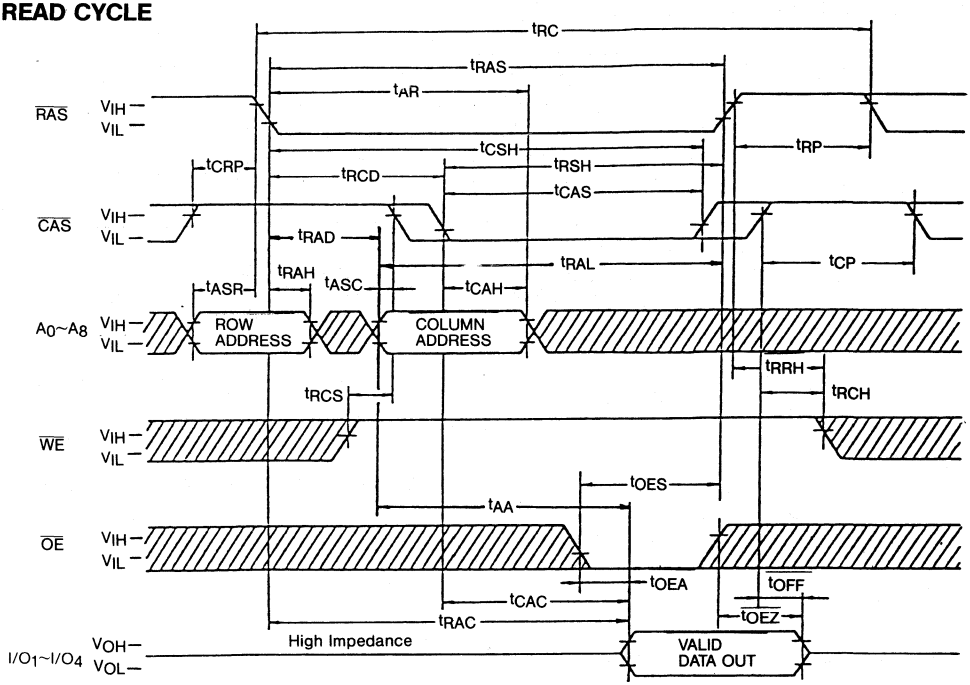
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD424256-8		μPD424256-10		μPD424256-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC OPERATING CURRENT	I_{CC1}		70		60		50	mA
VCC $\overline{RAS}$ ONLY REFRESH CURRENT	I_{CC3}		60		50		40	mA
VCC OPERATING CURRENT (PAGE MODE)	I_{CC4}		60		50		40	mA
VCC CBR REFRESH CURRENT	I_{CC6}		60		50		40	mA
RANDOM READ OR WRITE CYCLE TIME	t_{RC}	170		190		220		ns
READ WRITE CYCLE TIME	t_{RWC}	240		265		305		ns
FAST PAGE MODE CYCLE TIME	t_{PC}	60		70		85		ns
ACCESS TIME FROM $\overline{RAS}$	t_{RAC}		80		100		120	ns
ACCESS TIME FROM $\overline{CAS}$	t_{CAC}		20		25		30	ns
ACCESS TIME FROM COLUMN ADDRESS	t_{AA}		45		55		65	ns
ACCESS TIME FROM $\overline{CAS}$ PRECHARGE	t_{ACP}		55		65		80	ns
OUTPUT BUFFER TURN-OFF DELAY	t_{OFF}	0	20	0	25	0	30	ns
TRANSITION TIME (RISE AND FALL)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ PRECHARGE TIME	t_{RP}	80		80		90		ns
$\overline{RAS}$ PULSE WIDTH	t_{RAS}	80	10000	100	10000	120	10000	ns
$\overline{RAS}$ HOLD TIME	t_{RSH}	20		20		25		ns
$\overline{CAS}$ PULSE WIDTH	t_{CAS}	20	10000	20	10000	25	10000	ns
$\overline{CAS}$ HOLD TIME	t_{CSH}	80		100		120		ns
$\overline{RAS}$ TO $\overline{CAS}$ DELAY TIME	t_{RCD}	25	60	25	75	25	90	ns
$\overline{RAS}$ TO COLUMN ADDRESS DELAY TIME	t_{RAD}	20	35	20	45	20	55	ns
$\overline{CAS}$ TO $\overline{RAS}$ PRECHARGE TIME	t_{CRP}	10		10		10		ns
$\overline{CAS}$ PRECHARGE TIME	t_{CP}	10		10		15		ns
ROW ADDRESS SET-UP TIME	t_{ASR}	0		0		0		ns
ROW ADDRESS HOLD TIME	t_{RAH}	15		15		15		ns
COLUMN ADDRESS SET-UP TIME	t_{ASC}	0	20	0	30	0	35	ns

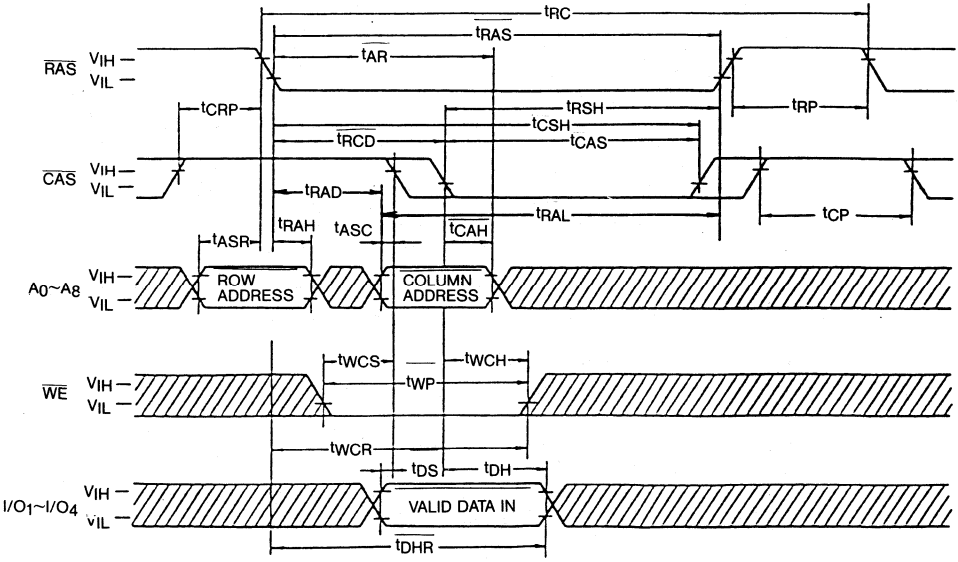
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD424256-8		μPD424256-10		μPD424256-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
COLUMN ADDRESS HOLD TIME	t_{CAH}	20		20		25		ns
COLUMN ADDRESS HOLD TIME REFERENCED TO $\overline{RAS}$	t_{AR}	60		70		85		ns
COLUMN ADDRESS TO $\overline{RAS}$ LEAD TIME	t_{RAL}	45		55		65		ns
READ COMMAND SET-UP TIME	t_{RCS}	0		0		0		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{RRH}	10		10		10		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{CAS}$	t_{RCH}	0		0		0		ns
WRITE COMMAND HOLD TIME	t_{WCH}	20		20		25		ns
WRITE COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{WCR}	60		70		85		ns
WRITE COMMAND PULSE WIDTH	t_{WP}	20		20		25		ns
WRITE COMMAND TO $\overline{RAS}$ LEAD TIME	t_{RWL}	40		40		45		ns
WRITE COMMAND TO $\overline{CAS}$ LEAD TIME	t_{CWL}	20		20		25		ns
DATA-IN SET-UP TIME	t_{DS}	0		0		0		ns
DATA-IN HOLD TIME	t_{DH}	20		20		25		ns
DATA-IN HOLD TIME REFERENCED TO $\overline{RAS}$	t_{DHR}	60		70		85		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{WCS}	0		0		0		ns
$\overline{CAS}$ TO $\overline{WE}$ DELAY	t_{CWD}	45		50		60		ns
$\overline{RAS}$ TO $\overline{WE}$ DELAY	t_{RWD}	105		130		155		ns
COLUMN ADDRESS TO $\overline{WE}$ DELAY	t_{AWD}	70		85		100		ns
$\overline{CAS}$ SET-UP TIME FOR CBR REFRESH	t_{CSR}	10		10		10		ns
$\overline{CAS}$ HOLD TIME FOR CBR REFRESH	t_{CHR}	20		20		25		ns
$\overline{RAS}$ PRECHARGE $\overline{CAS}$ HOLD TIME	t_{RPC}	0		0		0		ns
REFRESH PERIOD	t_{REF}		8		8		8	ms
ACCESS TIME FROM $\overline{OE}$	t_{OEA}		20		20		25	ns
DATA DELAY TIME	t_{OED}	20		25		30		ns
$\overline{OE}$ COMMAND HOLD TIME	t_{OEH}	0		0		0		ns
OUTPUT TURN-OFF DELAY TO $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{OE}$ TO $\overline{RAS}$ INACTIVE SET-UP TIME	t_{OES}	10		10		10		ns

READ CYCLE

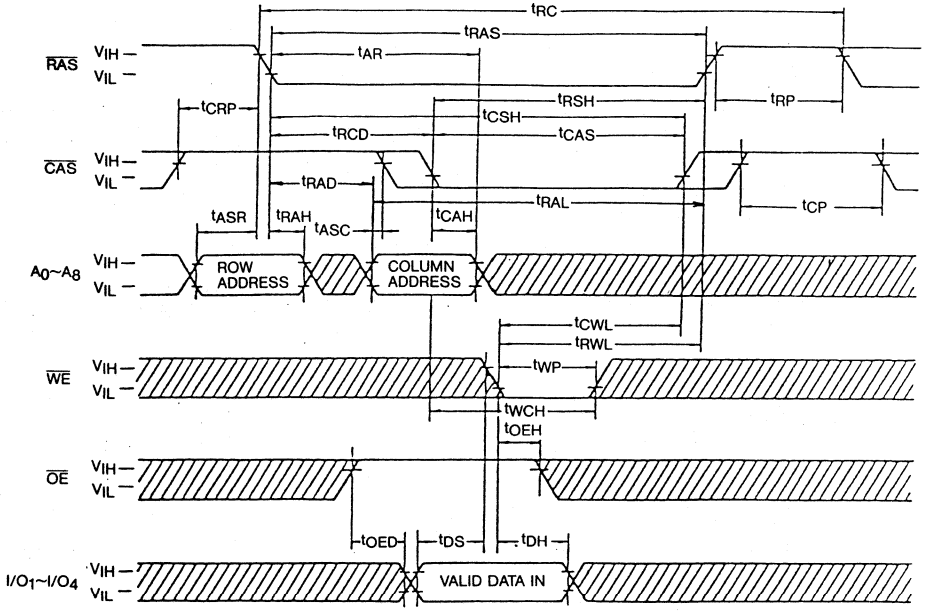


WRITE CYCLE (Early Write)

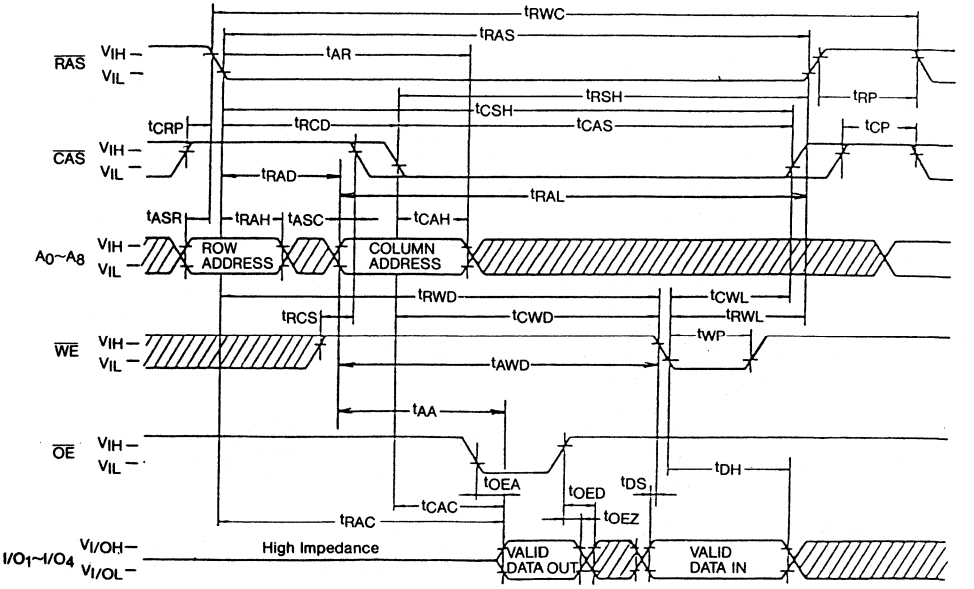


OE: Don't Care

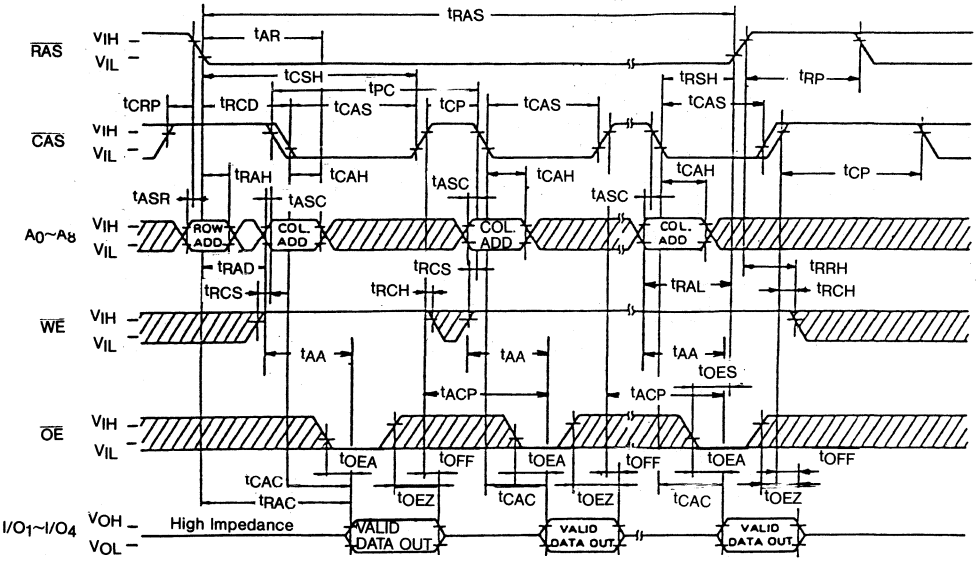
OE CONTROLLED WRITE CYCLE



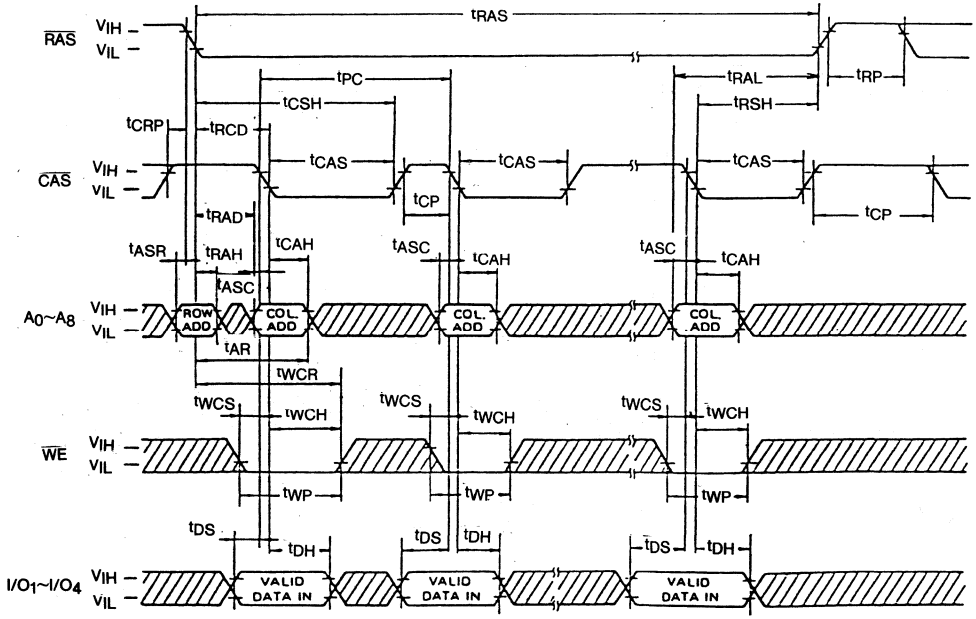
READ-WRITE/READ-MODIFY-WRITE CYCLE



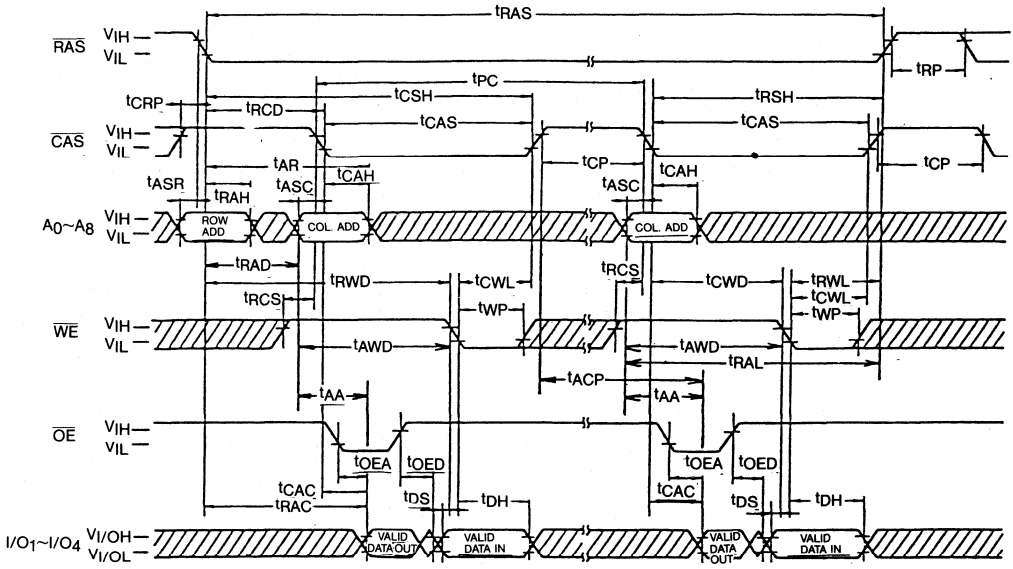
FAST PAGE MODE READ CYCLE



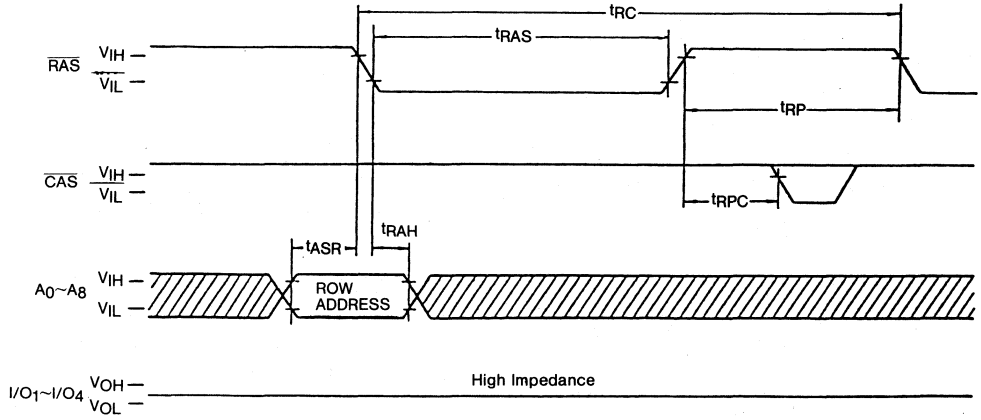
FAST PAGE MODE WRITE CYCLE (Early Write)



FAST PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE

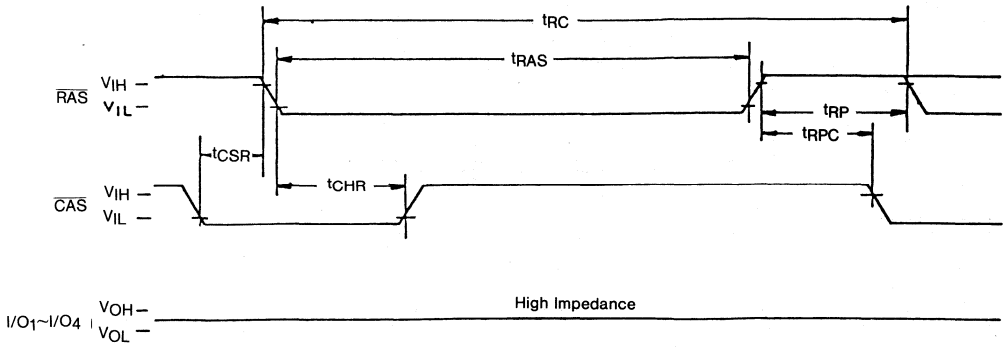


RAS ONLY REFRESH CYCLE



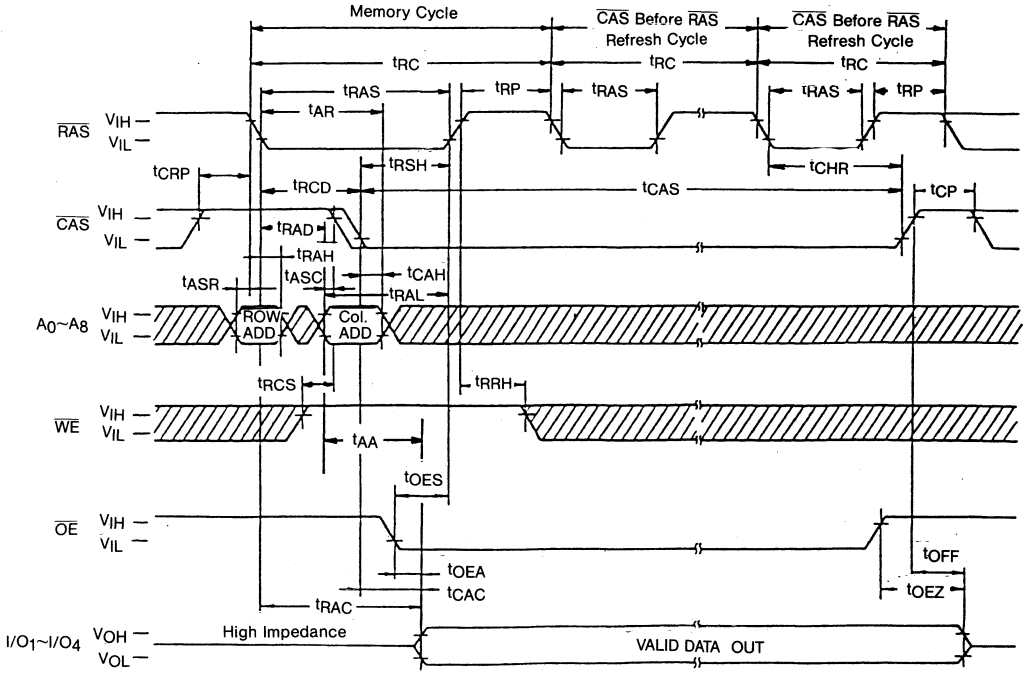
WE, OE: Don-t Care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE.



$\overline{WE}$, $\overline{OE}$, ADDRESS: Don't Care

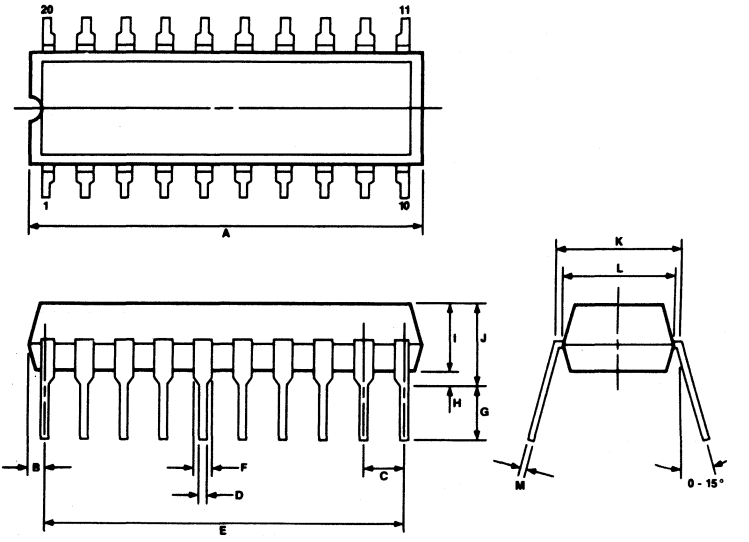
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

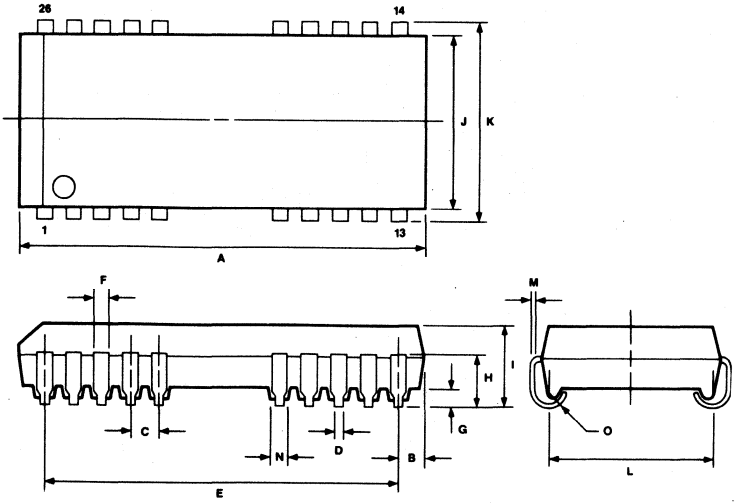
PLASTIC DIP

Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.25
M	$.25^{+.10}_{-.05}$



PLASTIC SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



μPD424258 (STATIC COLUMN)
262.144 W x 4 BIT DRAM

FEATURES

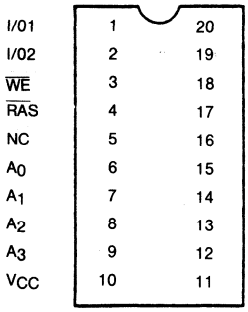
- 262.144 words by 4 bit organization
- Low power dissipation CMOS DRAM
- Single 5 V ± 10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- 512 cycle, 8 ms refresh
- High density 20-pin plastic DIP (μPD424258C) or 26/20-pin plastic SOJ (μPD424258LA)
- Static column mode

FAMILY	TRAC	TCAC	TAA	ICC1
μPD424258 - 8	80 ns	20 ns	45 ns	70 mA
μPD424258 - 10	100 ns	25 ns	55 ns	60 mA
μPD424258 - 12	120 ns	30 ns	65 ns	50 mA

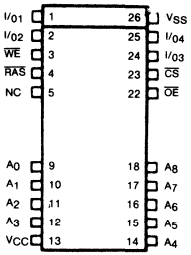
* tCAC = tOEA

PIN CONFIGURATION

20 PIN DIP



26/20 PIN SOJ



Ai	ADDRESS INPUT
I/0i	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CS}$	CHIP SELECT INPUT
$\overline{OE}$	OUTPUT ENABLE
WE	WRITE ENABLE
NC	NO CONNECTION
VCC	POWER SUPPLY
VSS	GROUND

AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD424258-8		μPD424258-10		μPD424258-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC OPERATING CURRENT	I_{CC1}		70		60		50	mA
VCC $\overline{RAS}$ ONLY REFRESH CURRENT	I_{CC3}		60		50		40	mA
VCC OPERATING CURRENT (STATIC COLUMN MODE)	I_{CC4}		60		50		40	mA
VCC CBR REFRESH CURRENT	I_{CC6}		60		50		40	mA
RANDOM READ OR WRITE CYCLE TIME	t_{RC}	170		190		220		ns
READ WRITE CYCLE TIME	t_{RWC}	240		265		305		ns
ACCESS TIME FROM $\overline{RAS}$	t_{RAC}		80		100		120	ns
ACCESS TIME FROM $\overline{CS}$	t_{CAC}		20		25		30	ns
ACCESS TIME FROM COLUMN ADDRESS	t_{AA}		45		55		65	ns
OUTPUT BUFFER TURN-OFF DELAY	t_{OFF}	0	20	0	25	0	30	ns
TRANSITION TIME (RISE AND FALL)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ PRECHARGE TIME	t_{RP}	80		80		90		ns
$\overline{RAS}$ PULSE WIDTH	t_{RAS}	80	10000	100	10000	120	10000	ns
$\overline{RAS}$ HOLD TIME	t_{RSH}	20		20		25		ns
$\overline{CS}$ PULSE WIDTH	t_{CS}	20	10000	20	10000	25	10000	ns
$\overline{CS}$ HOLD TIME	t_{CSH}	80		100		120		ns
$\overline{RAS}$ TO $\overline{CS}$ DELAY TIME	t_{RCD}	25	60	25	75	25	90	ns
$\overline{RAS}$ TO COLUMN ADDRESS DELAY TIME	t_{RAD}	20	35	20	45	20	55	ns
$\overline{CS}$ TO $\overline{RAS}$ PRECHARGE TIME	t_{CRP}	10		10		10		ns
$\overline{CS}$ PRECHARGE TIME	t_{CP}	10		10		15		ns
ROW ADDRESS SET-UP TIME	t_{ASR}	0		0		0		ns
ROW ADDRESS HOLD TIME	t_{RAH}	15		15		15		ns
COLUMN ADDRESS SET-UP TIME	t_{ASC}	0	20	0	30	0	35	ns
COLUMN ADDRESS HOLD TIME	t_{CAH}	20		20		25		ns
COLUMN ADDRESS HOLD TIME REFERENCED TO $\overline{RAS}$	t_{AR}	80		100		120		ns

AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD424258-8		μPD424258-10		μPD424258-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{RAS}$ TO COLUMN ADDRESS HOLD TIME	t_{AH}	15		15		15		ns
COLUMN ADDRESS TO $\overline{RAS}$ LEAD TIME	t_{RAL}	45		55		65		ns
READ COMMAND SET-UP TIME	t_{RCS}	0		0		0		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{RRH}	10		10		10		ns
READ COMMAND HOLD TIME REFERENCED TO $\overline{CS}$	t_{RCH}	0		0		0		ns
COLUMN ADDRESS HOLD TIME TO $\overline{RAS}$ ON WRITE	t_{AWR}	60		70		85		ns
WRITE COMMAND HOLD TIME	t_{WCH}	20		20		25		ns
WRITE COMMAND HOLD TIME REFERENCED TO $\overline{RAS}$	t_{WCR}	60		70		85		ns
WRITE COMMAND PULSE WIDTH	t_{WP}	20		20		25		ns
WRITE COMMAND TO $\overline{RAS}$ LEAD TIME	t_{RWL}	40		40		45		ns
WRITE COMMAND TO $\overline{CS}$ LEAD TIME	t_{CWL}	20		20		25		ns
DATA-IN SET-UP TIME	t_{DS}	0		0		0		ns
DATA-IN HOLD TIME	t_{DH}	20		20		25		ns
DATA-IN HOLD TIME REFERENCED TO $\overline{RAS}$	t_{DHR}	60		70		85		ns
$\overline{WE}$ COMMAND SET-UP TIME	t_{WCS}	0		0		0		ns
$\overline{CS}$ TO $\overline{WE}$ DELAY	t_{CWD}	45		50		60		ns
$\overline{RAS}$ TO $\overline{WE}$ DELAY	t_{RWD}	105		130		155		ns
COLUMN ADDRESS TO $\overline{WE}$ DELAY	t_{AWD}	70		85		100		ns
$\overline{CS}$ SET-UP TIME FOR CBR REFRESH	t_{CSR}	10		10		10		ns
$\overline{CS}$ HOLD TIME FOR CBR REFRESH	t_{CHR}	20		20		25		ns
$\overline{RAS}$ PRECHARGE $\overline{CS}$ HOLD TIME	t_{RPC}	0		0		0		ns
REFRESH PERIOD	t_{REF}		8		8		8	ms
ACCESS TIME FROM $\overline{OE}$	t_{OEA}		20		20		25	ns
DATA DELAY TIME	t_{OED}	20		25		30		ns

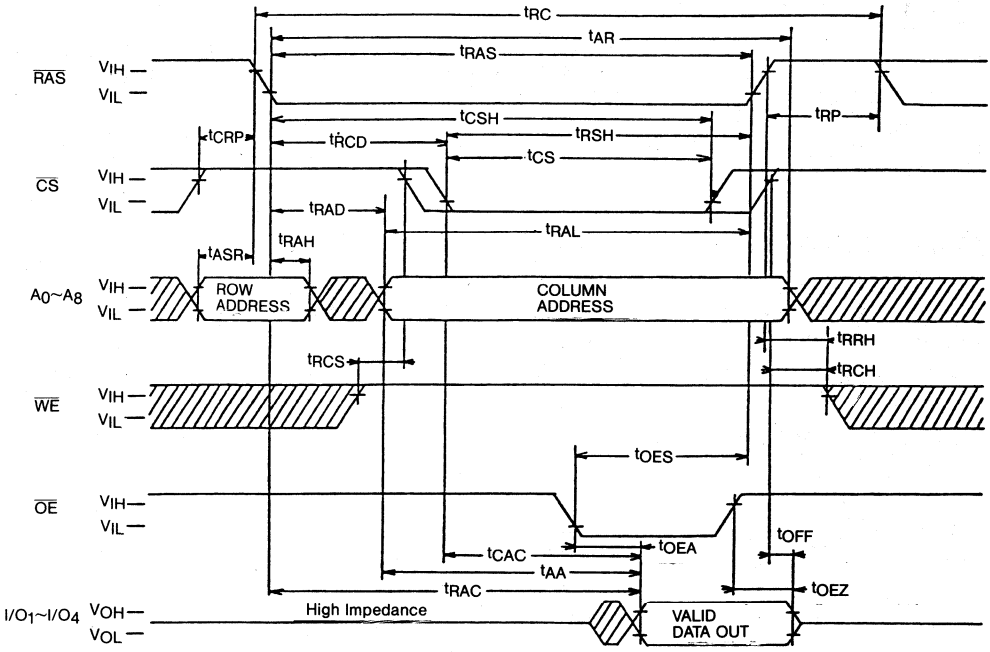
AC CHARACTERISTICS
(TA = 0 °C to 70 °C, VCC = 5V ± 10 %)

PARAMETER	SYMBOL	μPD424258-8		μPD424258-10		μPD424258-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{OE}$ COMMAND HOLD TIME	t_{OEH}	0		0		0		ns
OUTPUT TURN-OFF DELAY TO $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{OE}$ TO $\overline{RAS}$ INACTIVE SET-UP TIME	t_{OES}	10		10		10		ns

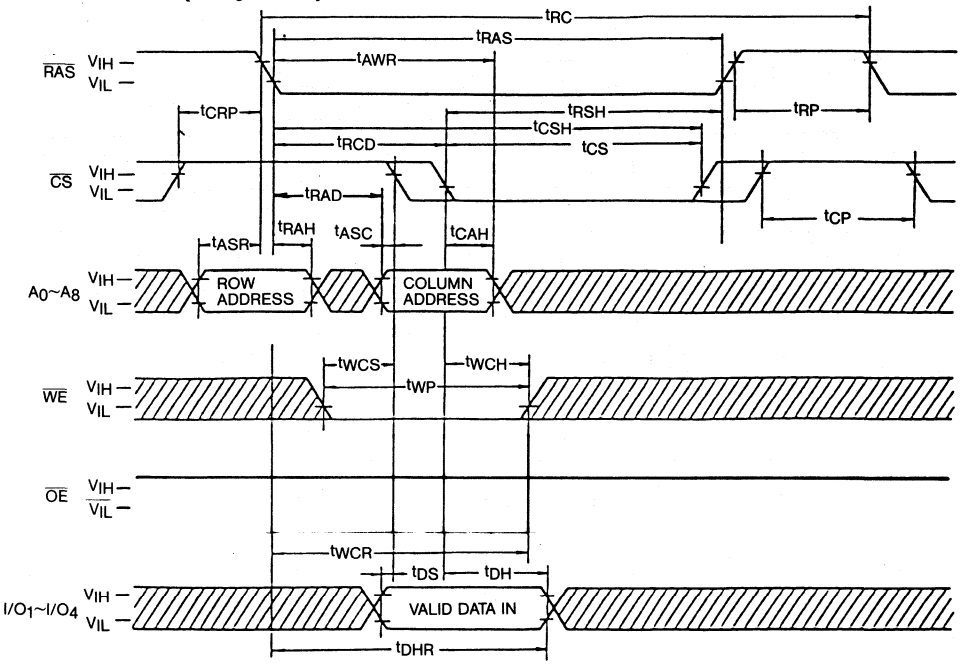
STATIC COLUMN MODE

SC MODE CYCLE TIME ON READ	t_{RSC}	50		60		70		ns
SC MODE CYCLE TIME ON WRITE	t_{WSC}	50		60		70		ns
SC MODE $\overline{RAS}$ PULSE WIDTH	t_{RASC}	80	140000	100	140000	120	140000	ns
$\overline{RAS}$ TO SECOND $\overline{WE}$ DELAY TIME	t_{RSW}	85		105		125		ns
WRITE INVALID TIME	t_{WI}	10		10		10		ns
OUTPUT HOLD TIME FROM ADDRESS	t_{OH}	5		5		5		ns
SC MODE CYCLE TIME ON READ-WRITE	t_{RWSC}	120		145		170		ns
ACCESS TIME FROM PREVIOUS $\overline{WE}$	t_{PWA}		90		110		130	ns
PREVIOUS $\overline{WE}$ TO COLUMN ADDRESS DELAY TIME	t_{WAD}	25	45	25	55	30	65	ns
COLUMN ADDRESS HOLD TIME TO PREVIOUS $\overline{WE}$	t_{PWH}	120		140		160		ns

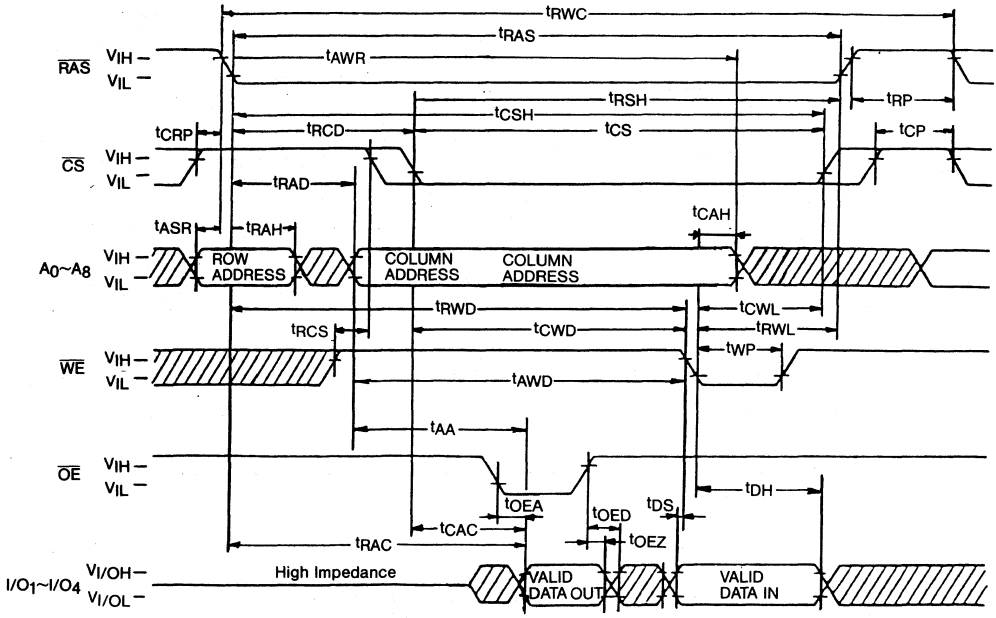
READ CYCLE


tRC
tAR
tRAS
RAS
VIH
VIL
tCSH
tRP
tCRP
tRCD
tRSH
tCS
CS
tRAD
tRAL
tRAH
tASR
A0~A8
ROW ADDRESS
COLUMN ADDRESS
tRRH
tRCS
tRCH
WE
tOES
OE
tOFF
tCAC
tOEA
tAA
tRAC
tOEZ
I/O1~I/O4
VOH
VOL
High Impedance
VALID DATA OUT

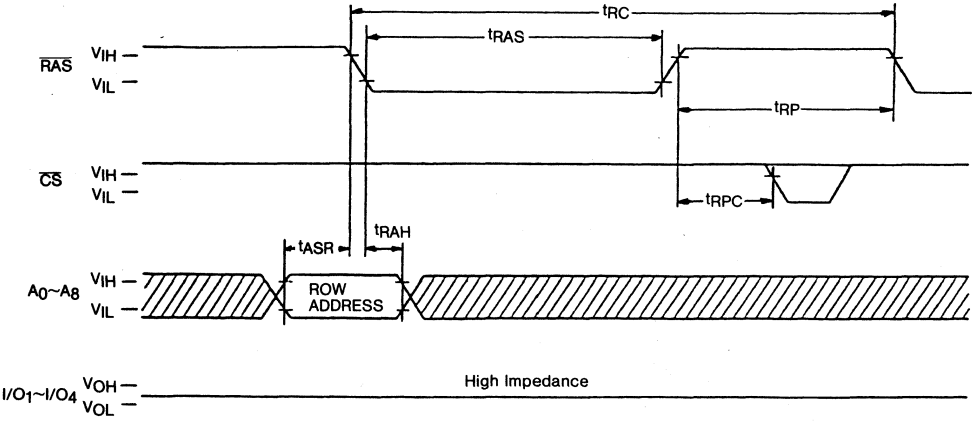
WRITE CYCLE (Early Write)



READ-WRITE/READ-MODIFY-WRITE CYCLE

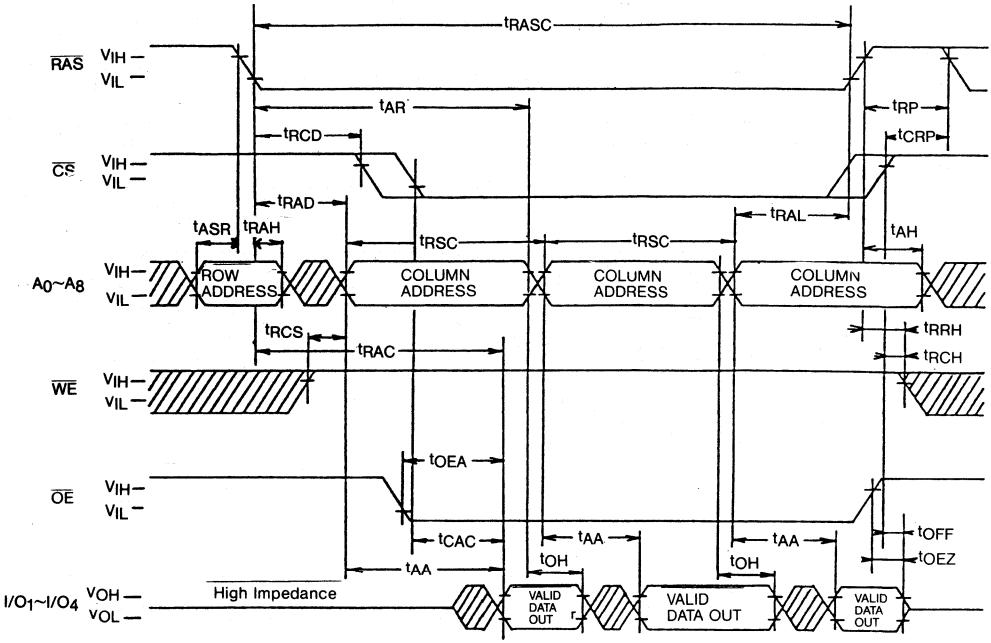


RAS ONLY REFRESH CYCLE

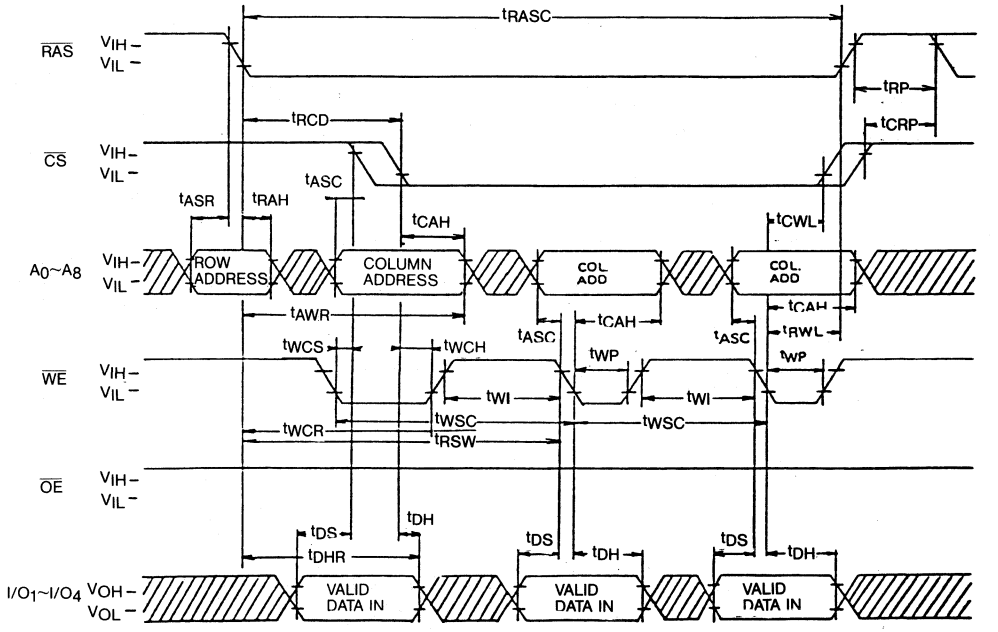


WE, OE: Don-t Care

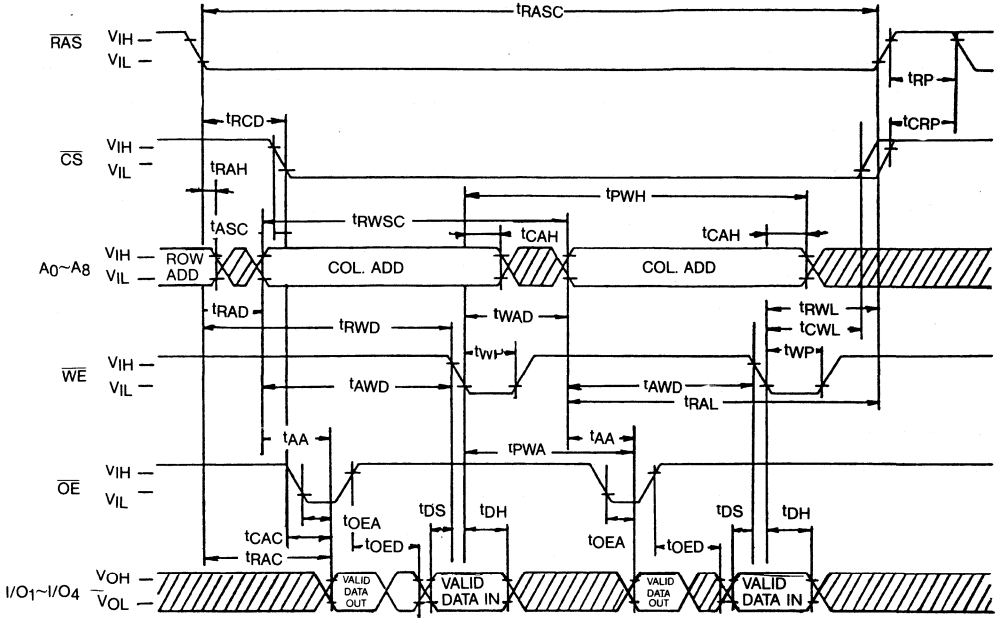
STATIC COLUMN MODE READ CYCLE



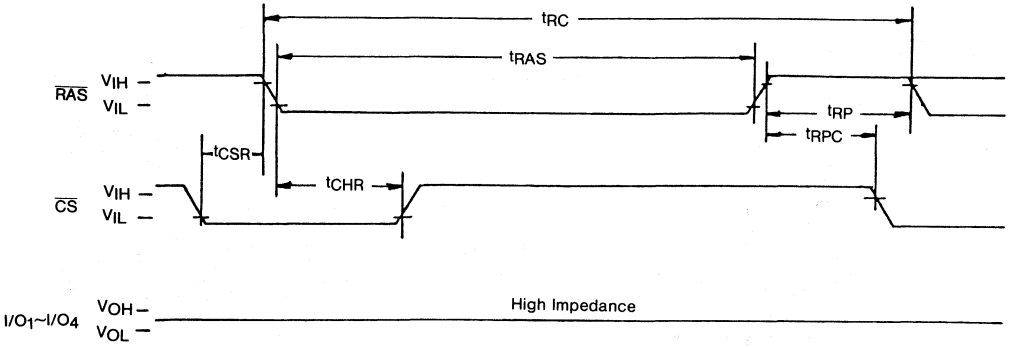
STATIC COLUMN MODE WRITE CYCLE



STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

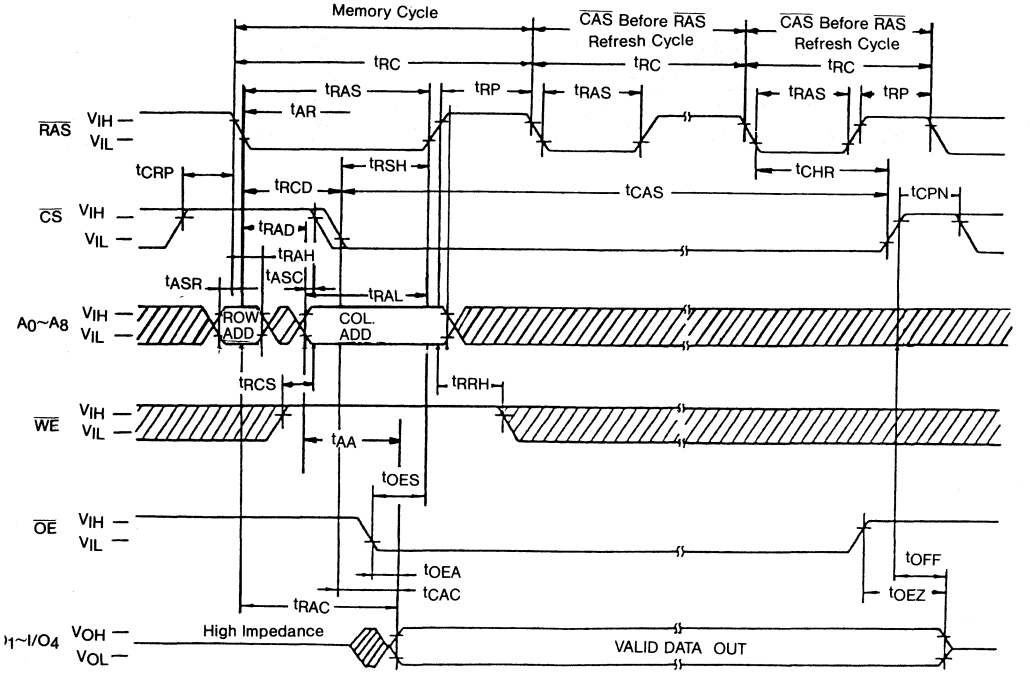


$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



$\overline{WE}$, $\overline{OE}$, ADDRESS: Don't Care

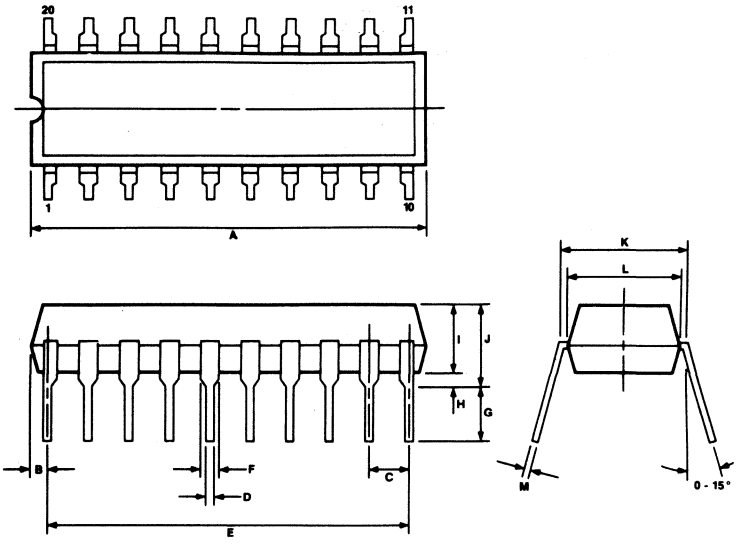
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

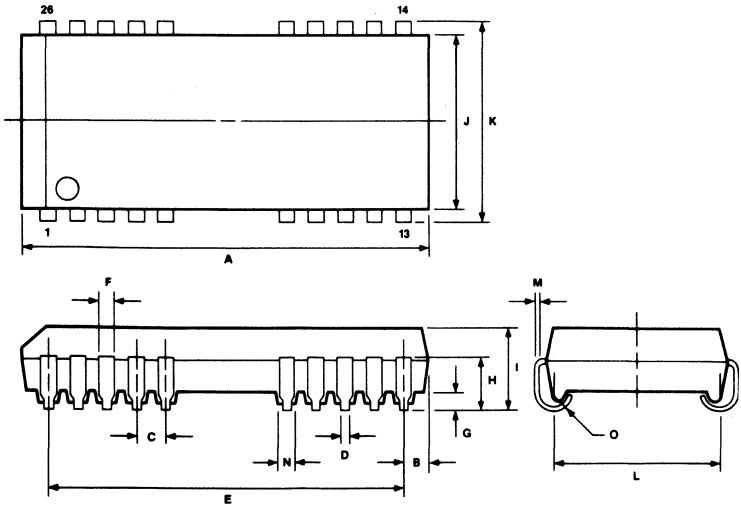
PLASTIC DIP

Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	7.25
M	$.25^{+.10}_{-.05}$



PLASTIC SOJ

Item	Millimeters
A	17.35 ± .25
B	1.08 ±.15
C	1.27
D	.40 ± .10
E	15.24
F	.60
G	.8 min
H	2.4 ± .2
I	3.5 ± .2
J	7.57
K	8.47 ± .2
L	6.73 ± .2
M	$.20^{+.10}_{-.05}$
N	.07
O	.85 rad



910 x 8-BIT FIFO MEMORY

Description

This device is a 910-word by 8-bit first-in first-out biport memory fabricated with the N-channel silicon gate process. The device helps to create an NTSC flicker-free television picture (noninterlace conversion) by providing intermediate storage and very high speed read and write operations.

The μPD41101C can also be used as a digital delay line. The delay length is variable from 10 to 910 bits.

Features

- ☐ 910-word x 8-bit organization
- ☐ FIFO (first-in first-out) biport memory
- ☐ Suitable for NTSC, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operations
- ☐ Can be used as a 1H (910-bit) delay line
- ☐ TTL compatible
- ☐ Three-state outputs
- ☐ Single 5 V ± 10% power supply
- ☐ 24-pin, 300 mil DIP package

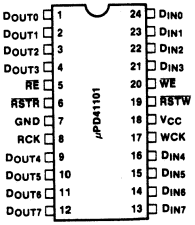
Performance Ranges

Device	Read Cycle Time (Min)	Read Access Time (Max)	Write Cycle Time (Min)
μPD41101-3	34 ns	27 ns	34 ns
μPD41101-2	34 ns	27 ns	69 ns
μPD41101-1	69 ns	49 ns	69 ns

Pin Identification

No.	Symbol	Function
1-4, 9-12	D_{OUT0}-D_{OUT7}	Read data outputs
5	$\overline{RE}$	Read enable input
6	$\overline{RSTR}$	Read address reset input
7	GND	Ground
8	RCK	Read clock input
13-16, 21-24	D_{IN0}-D_{IN7}	Write data inputs
17	WCK	Write clock input
18	V_{CC}	5 V power supply
19	$\overline{RSTW}$	Write address reset input
20	$\overline{WE}$	Write enable input

Pin Configuration



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]
In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]
These tri-state outputs are used to access the stored information. In a simple digital delay line application, a minimum delay of 10 clock cycles is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ [Write Address Reset Input]
Bringing this signal to a low level resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ [Read Address Reset Input]
Strobed by the rising edge of RCK, this signal resets the internal read address to 0.

$\overline{WE}$ [Write Enable Input]
This input controls write operations. If $\overline{WE}$ is at a low level, all write operations proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]
This signal is similar to $\overline{WE}$ but controls read operations. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]
All write operations are performed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK [Read Clock Input]
All read operations are performed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts the internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram

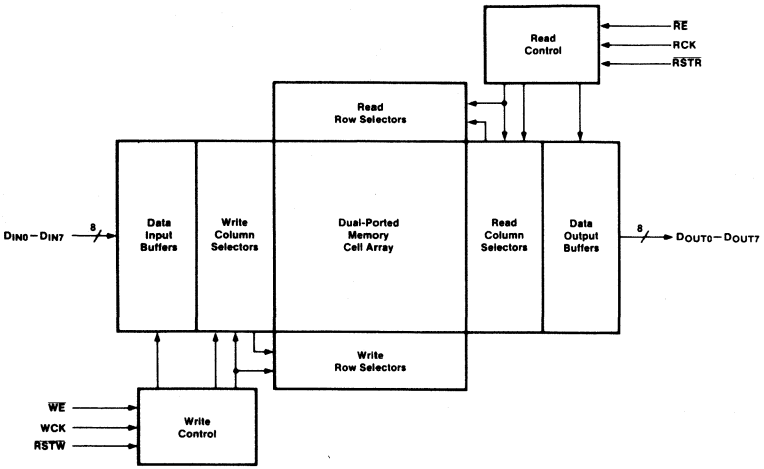
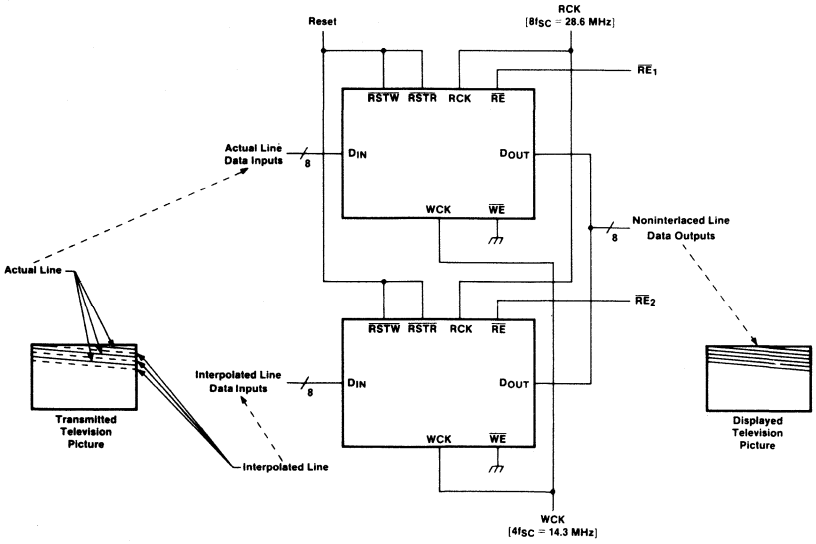


Figure 1. Connection for Noninterlace Conversion



Recommended DC Operating Conditions

$T_A = -20$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Ground	GND	0	0	0	V	
Input voltage high	V_{IH}	2.4		5.5	V	
Input voltage low	V_{IL}	−1.5		0.8	V	

Capacitance

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Note:
(1) These parameters are sampled and not 100% tested.

DC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/Read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} is disabled; $V_O = 0$ to 5.5 V
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2$ mA

Note:
(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Symbol	Parameter	Limits μPD41101-3 Min	Limits μPD41101-3 Max	Limits μPD41101-2 Min	Limits μPD41101-2 Max	Limits μPD41101-1 Min	Limits μPD41101-1 Max	Unit	Test Conditions
t_{WCK}	Write clock cycle time	34	1090	69	1090	69	1090	ns	
t_{WCW}	WCK pulse width	14		25		25		ns	
t_{WCP}	WCK precharge time	14		25		25		ns	
t_{RCK}	Read clock cycle time	34	1090	34	1090	69	1090	ns	
t_{RCW}	RCK pulse width	14		14		25		ns	
t_{RCP}	RCK precharge time	14		14		25		ns	
t_{AC}	Access time		27		27		49	ns	
t_{ACR}	Access time after a reset cycle		49		49		49	ns	
t_{OH}	Output hold time	5		5		5		ns	
t_{OHR}	Output hold time after a reset cycle	5		5		5		ns	(Note 7)
t_{LZ}	Output active time	5	27	5	27	5	49	ns	(Note 4)
t_{HZ}	Output disable time	5	27	5	27	5	49	ns	(Note 4)
t_{DS}	Data-in set-up time	14		18		18		ns	
t_{DH}	Data-in hold time	5		5		5		ns	
t_{RS}	Reset active set-up time	14		14		20		ns	(Note 8)
t_{RH}	Reset active hold time	5		5		5		ns	(Note 8)
t_{RN1}	Reset inactive hold time	5		5		5		ns	(Note 9)
t_{RN2}	Reset inactive set-up time	14		14		20		ns	(Note 9)
t_{WES}	Write enable set-up time	14		20		20		ns	(Note 10)
t_{WEH}	Write enable hold time	5		5		5		ns	(Note 10)
t_{WEN1}	Write enable high delay from WCK	5		5		5		ns	(Note 11)
t_{WEN2}	Write enable low delay to WCK	14		20		20		ns	(Note 11)
t_{RES}	Read enable set-up time	14		14		20		ns	(Note 10)
t_{REH}	Read enable hold time	5		5		5		ns	(Note 10)
t_{REN1}	Read enable high delay from RCK	5		5		5		ns	(Note 11)
t_{REN2}	Read enable low delay to RCK	14		14		20		ns	(Note 11)
t_{WEW}	Write disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{REW}	Read disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTW}	Write reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTR}	Read reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_T	Transition time	3	35	3	35	3	35	ns	

Note:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ± 200 mv from the steady state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Note [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910t_{WCK} \leq 1$ ms
$t_{REW} + t_{RSTR} + 910t_{RCK} \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (910 Bit) Delay Line

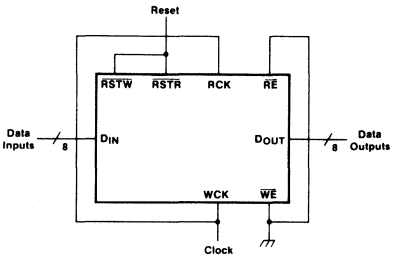


Figure 3. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

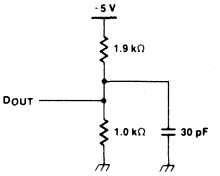
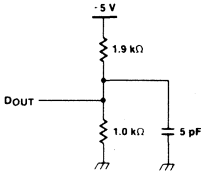
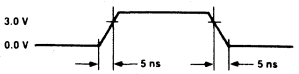


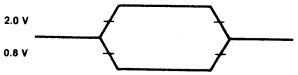
Figure 4. Output Load for t_{LZ} and t_{HZ}



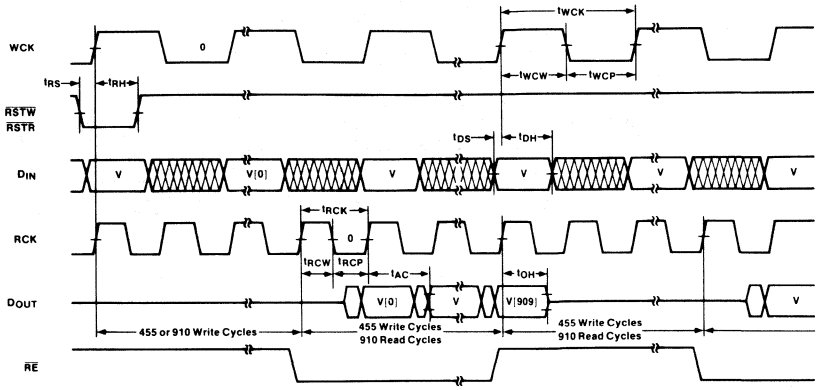
AC Input Timing Reference Waveform



AC Output Timing Reference Waveform



Basic Timing for Noninterlace Conversion



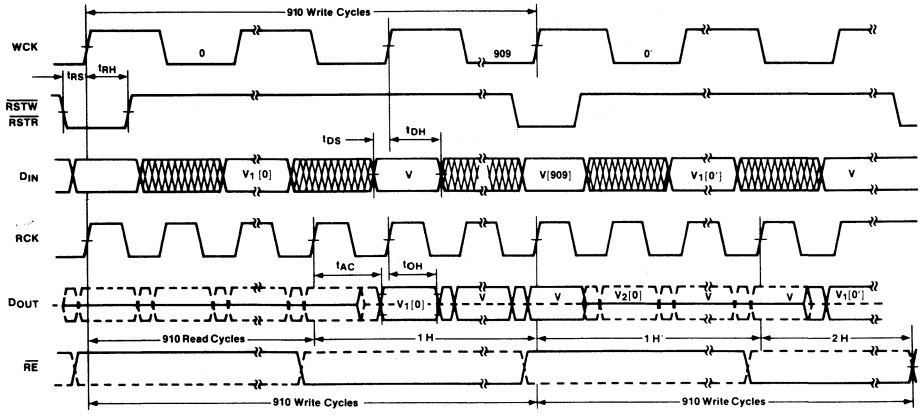
Note:

[1] $\overline{WE}$ = V_{IL}.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

Application Timing for Noninterlace Conversion



Note:

[1] $\overline{WE}$ = V_{IL}.

[2] V = Valid Data.

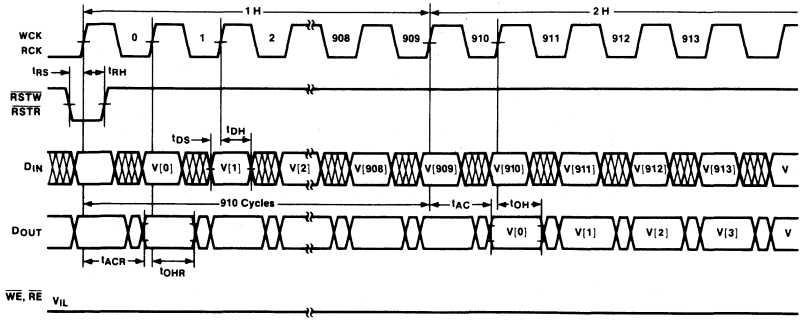
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

[4] 1H = the first "actual line" of 910 words. 1H' = the first (normally) interpolated line of 910 words. See Figure 1.

[5] See Figure 1. D_{IN} above represents the scan line input to one of the two μPD41101s. D_{OUT} and $\overline{RE}$ above represent the combined output and the complementary $\overline{RE}$ inputs for both devices. The signals for one μPD41101 are drawn as solid lines; the signals for the second μPD41101, as dashed lines.

[6] Reset pulses can be applied to $\overline{RSTW}$ and $\overline{RSTR}$ at regular intervals to remove any effects due to jitter in the system clock.

910-Bit Delay Line

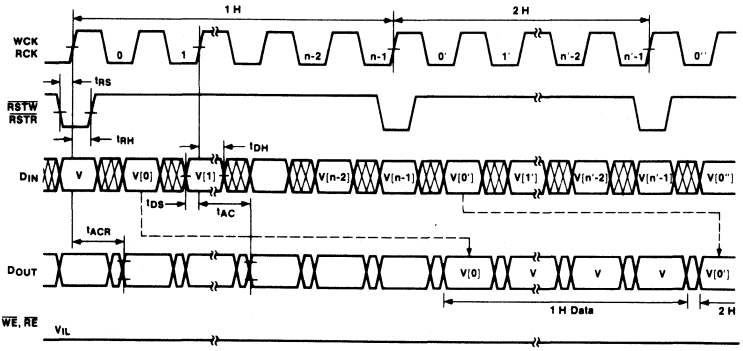


Note:

[1] V = Valid Data.

[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

n-Bit Delay Line

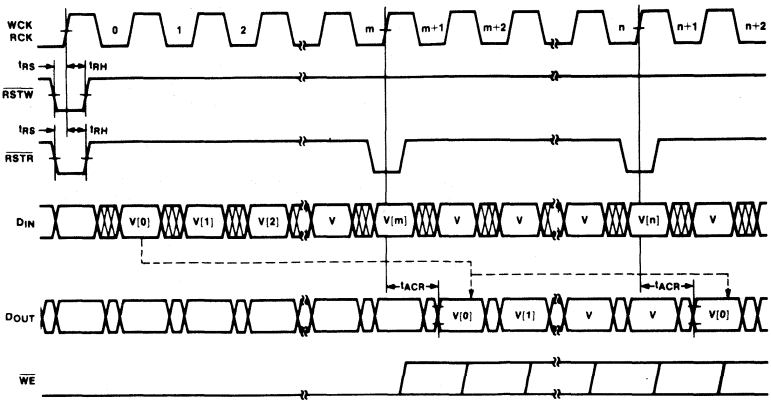


Note:

[1] V = Valid Data.

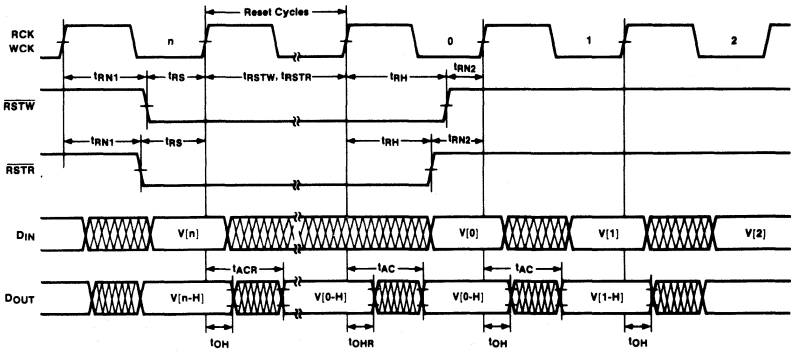
[2] 1H = the first group of n bits. 2H = the second group of n bits.

Re-Read Operation



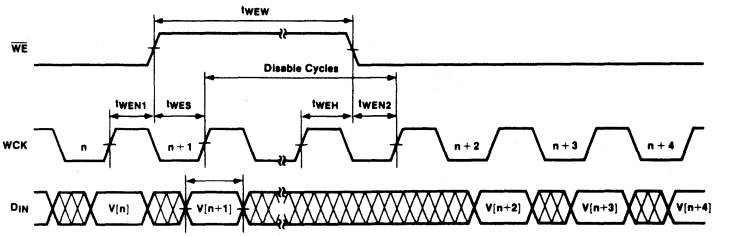
Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

Read or Write Reset



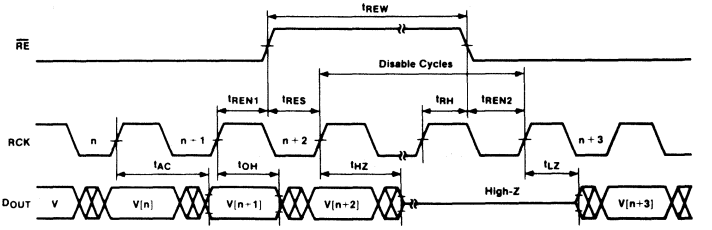
Note:
[1] $\overline{WE}$ = $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.
[4] H = 910 cycles.
[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

Write Disable



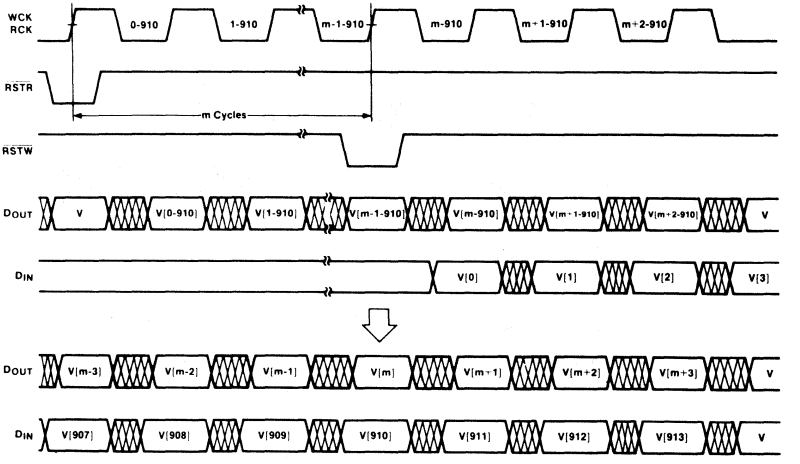
Note:
[1] V = Valid Data.

Read Disable



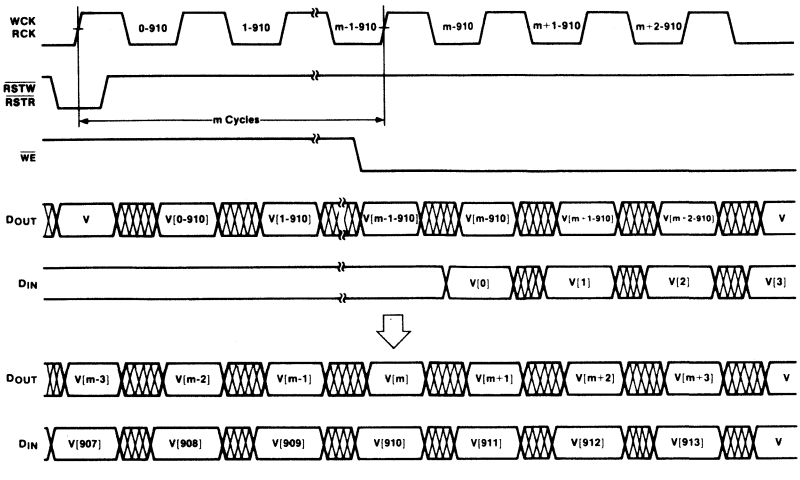
Note:
[1] V = Valid Data.

(910-m)-Bit Delay Line, No. 1



Note:
[1] $\overline{RE}$ V_{IL}.
[2] V Valid Data.

(910-m)-Bit Delav Line, No. 2



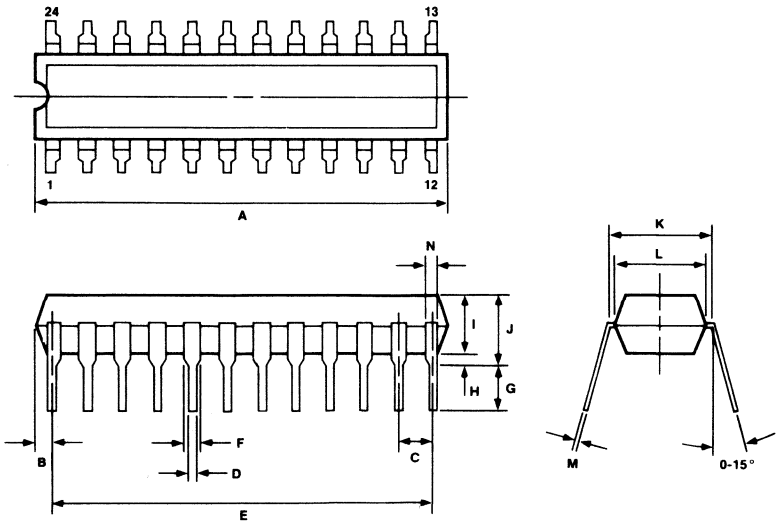
Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

Package Dimensions

24 PIN Plastic DIP

μPD41101C

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.50 ± 0.3
H	0.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



1135 x 8-BIT FIFO MEMORY

Description

This device is a 1135-word by 8-bit first-in first-out biport memory fabricated with the N-channel silicon gate process. The device helps to create a PAL flicker-free television picture (noninterlace conversion) by providing intermediate storage and very high speed read and write operations.

The μPD41102C can also be used as a digital delay line. The delay length is variable from 12 to 1135 bits.

Features

- ☐ 1135-word x 8-bit organization
- ☐ FIFO (first-in first-out) biport memory
- ☐ Suitable for PAL, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operations
- ☐ Can be used as a 1H (1135-bit) delay line
- ☐ TTL compatible
- ☐ Three-state outputs
- ☐ Single 5 V ± 10% power supply
- ☐ 24-pin, 300 mil DIP package

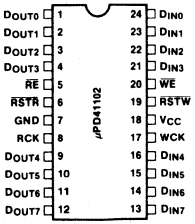
Performance Ranges

Device	Read Cycle Time (Min)	Read Access Time (Max)	Write Cycle Time (Min)
μPD41102-3	28 ns	21 ns	28 ns
μPD41102-2	28 ns	21 ns	56 ns
μPD41102-1	56 ns	40 ns	56 ns

Pin Identification

No.	Symbol	Function
1-4, 9-12	D_{OUT0}-D_{OUT7}	Read data outputs
5	$\overline{RE}$	Read enable input
6	$\overline{RSTR}$	Read address reset input
7	GND	Ground
8	RCK	Read clock input
13-16, 21-24	D_{IN0}-D_{IN7}	Write data inputs
17	WCK	Write clock input
18	V_{CC}	5 V power supply
19	$\overline{RSTW}$	Write address reset input
20	$\overline{WE}$	Write enable input

Pin Configuration



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]
In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]
These tri-state outputs are used to access the stored information. In a simple digital delay line application, a minimum delay of 12 clock cycles is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ [Write Address Reset Input]
Bringing this signal to a low level resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ [Read Address Reset Input]
Strobed by the rising edge of RCK, this signal resets the internal read address to 0.

$\overline{WE}$ [Write Enable Input]
This input controls write operations. If $\overline{WE}$ is at a low level, all write operations proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]
This signal is similar to $\overline{WE}$ but controls read operations. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]
All write operations are performed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 1134 to 0 and begin increasing again.

RCK [Read Clock Input]
All read operations are performed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts the internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 1134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram

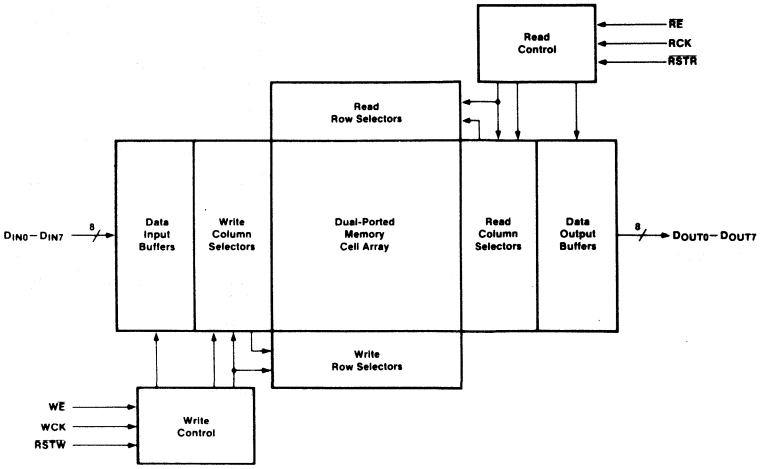
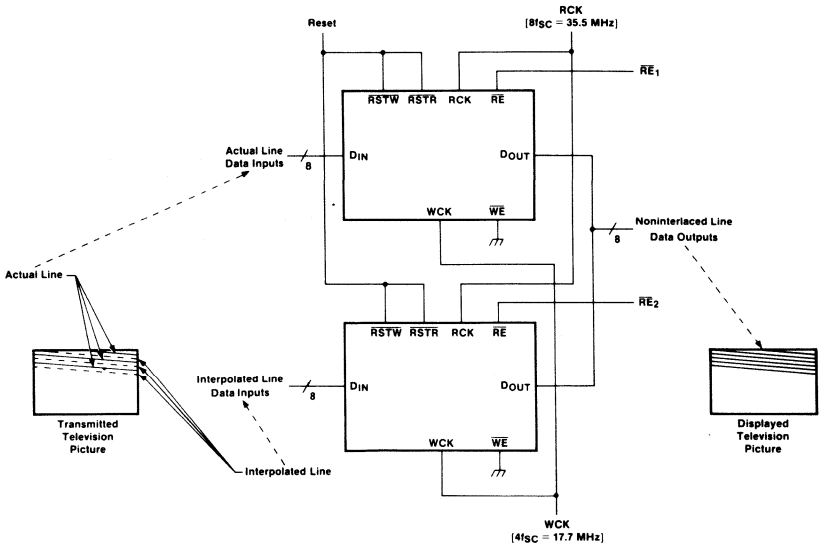


Figure 1. Connection for Noninterlace Conversion



Recommended DC Operating Conditions

T_A = −20 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Ground	GND	0	0	0	V	
Input voltage high	V_{IH}	2.4		5.5	V	
Input voltage low	V_{IL}	−1.5		0.8	V	

Capacitance

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, $\overline{WCK}$, $\overline{RCK}$, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Note:
(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/Read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} is disabled; V_O = 0 to 5.5 V
Output voltage high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 2 mA

Note:
(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Symbol	Parameter	Limits μPD41102-3 Min	Limits μPD41102-3 Max	Limits μPD41102-2 Min	Limits μPD41102-2 Max	Limits μPD41102-1 Min	Limits μPD41102-1 Max	Unit	Test Conditions
t_{WCK}	Write clock cycle time	28	880	56	880	56	880	ns	
t_{WCW}	WCK pulse width	12		20		20		ns	
t_{WCP}	WCK precharge time	12		20		20		ns	
t_{RCK}	Read clock cycle time	28	880	28	880	56	880	ns	
t_{RCW}	RCK pulse width	12		12		20		ns	
t_{RCP}	RCK precharge time	12		12		20		ns	
t_{AC}	Access time		21		21		40	ns	
t_{ACR}	Access time after a reset cycle		40		40		40	ns	
t_{OH}	Output hold time	5		5		5		ns	
t_{OHR}	Output hold time after a reset cycle	5		5		5		ns	(Note 7)
t_{LZ}	Output active time	5	21	5	21	5	40	ns	(Note 4)
t_{HZ}	Output disable time	5	21	5	21	5	40	ns	(Note 4)
t_{DS}	Data-in set-up time	12		15		15		ns	
t_{DH}	Data-in hold time	5		5		5		ns	
t_{RS}	Reset active set-up time	12		12		20		ns	(Note 8)
t_{RH}	Reset active hold time	5		5		5		ns	(Note 8)
t_{RN1}	Reset inactive hold time	5		5		5		ns	(Note 9)
t_{RN2}	Reset inactive set-up time	12		12		20		ns	(Note 9)
t_{WES}	Write enable set-up time	12		20		20		ns	(Note 10)
t_{WEH}	Write enable hold time	5		5		5		ns	(Note 10)
t_{WEN1}	Write enable high delay from WCK	5		5		5		ns	(Note 11)
t_{WEN2}	Write enable low delay to WCK	12		20		20		ns	(Note 11)
t_{RES}	Read enable set-up time	12		12		20		ns	(Note 10)
t_{REH}	Read enable hold time	5		5		5		ns	(Note 10)
t_{REN1}	Read enable high delay from RCK	5		5		5		ns	(Note 11)
t_{REN2}	Read enable low delay to RCK	12		12		20		ns	(Note 11)
t_{WEW}	Write disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ns	
t_{REW}	Read disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ns	
t_{RSTW}	Write reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ns	
t_{RSTR}	Read reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ns	
t_T	Transition time	3	35	3	35	3	35	ns	

Note:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ± 200 mv from the steady state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristic (cont)

Note [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 1135t_{WCK} \leq 1$ ms
$t_{REW} + t_{RSTR} + 1135t_{RCK} \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (1135-Bit) Delay Line

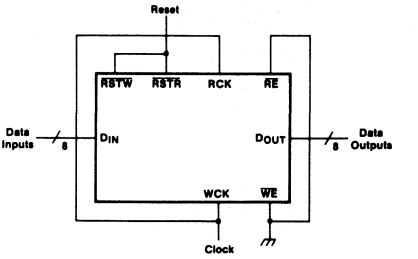


Figure 3. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

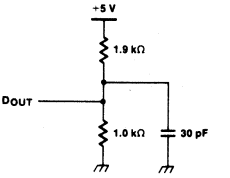
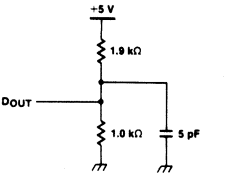
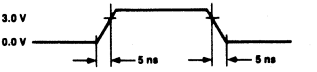


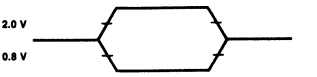
Figure 4. Output Load for t_{LZ} and t_{HZ}



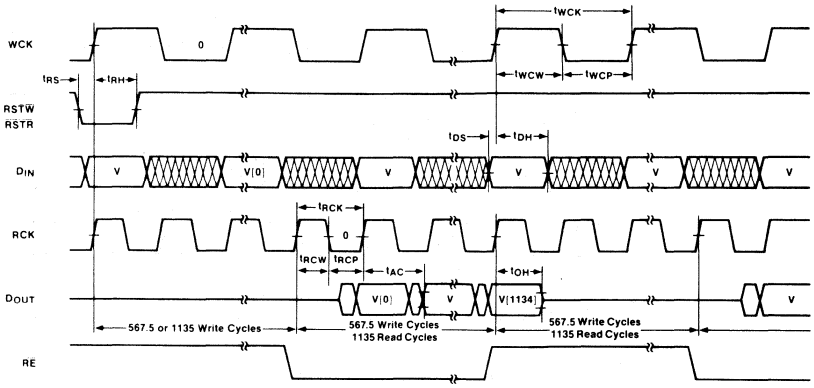
AC Input Timing Reference Waveform



AC Output Timing Reference Waveform



Basic Timing for Noninterlace Conversion



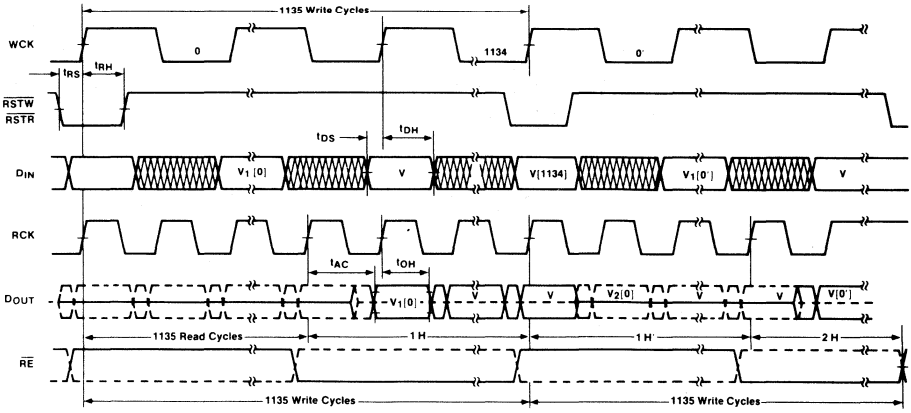
Note:

[1] $\overline{WE}$ V_{IL}.

[2] V Valid Data.

[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

Application Timing for Noninterlace Conversion



Note:

[1] $\overline{WE}$ V_{IL}.

[2] V Valid Data.

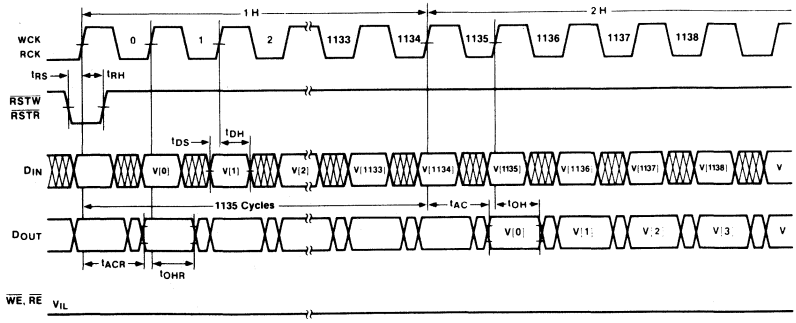
[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

[4] 1H The first "actual line" of 1135 words. 1H' The first (normally) interpolated line of 1135 words. See Figure 1.

[5] See Figure 1. D_{IN} above represents the scan line input to one of the two μPD41102s. D_{OUT} and $\overline{RE}$ above represent the combined output and the complementary $\overline{RE}$ inputs for both devices. The signals for one μPD41102 are drawn as solid lines; the signals for the second μPD41102, as dashed lines.

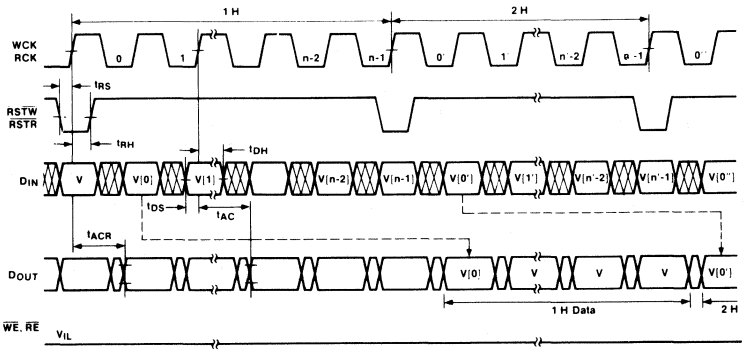
[6] Reset pulses can be applied to $\overline{RSTW}$ and $\overline{RSTR}$ at regular intervals to remove any effects due to jitter in the system clock.

1135-Bit Delay Line



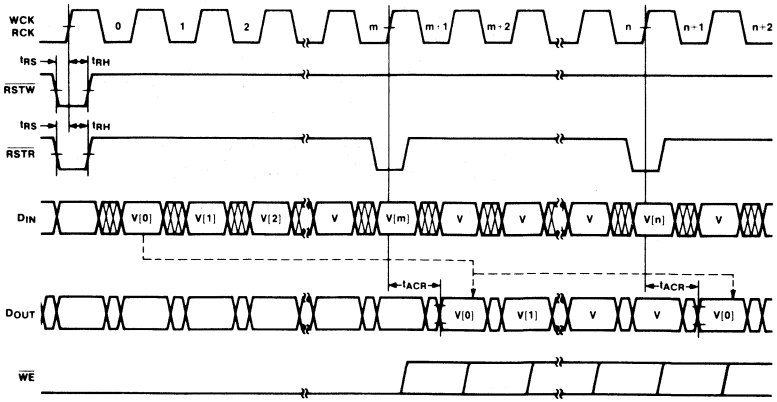
Note:
[1] V = Valid Data.
[2] 1H = the first group of 1135 bits. 2H = the second group of 1135 bits.

n-Bit Delay Line



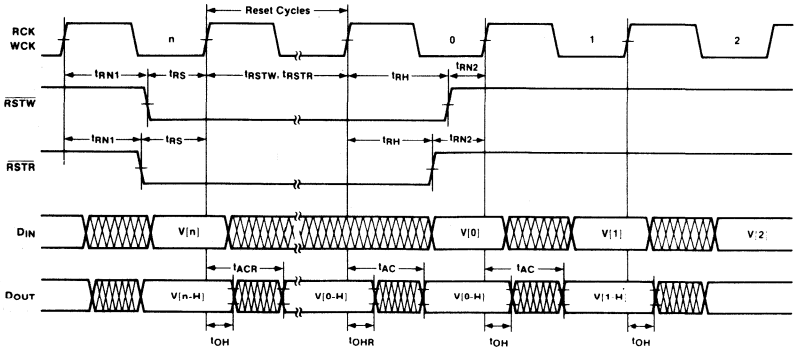
Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n bits.

Re-Read Operation



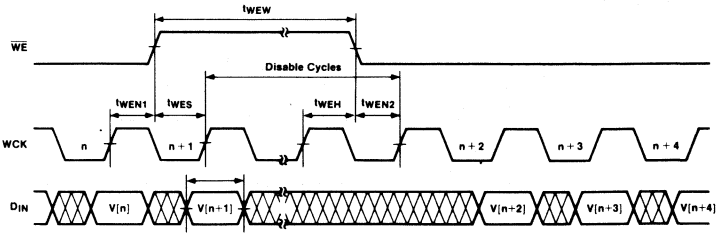
Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

Read or Write Reset



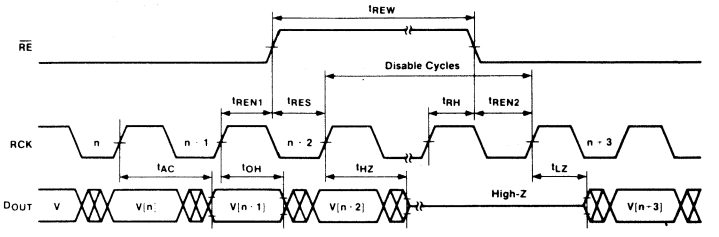
Note:
[1] $\overline{WE}$ · $\overline{RE}$ V_{IL}
[2] V Valid Data.
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.
[4] H 1135 cycles.
[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

Write Disable



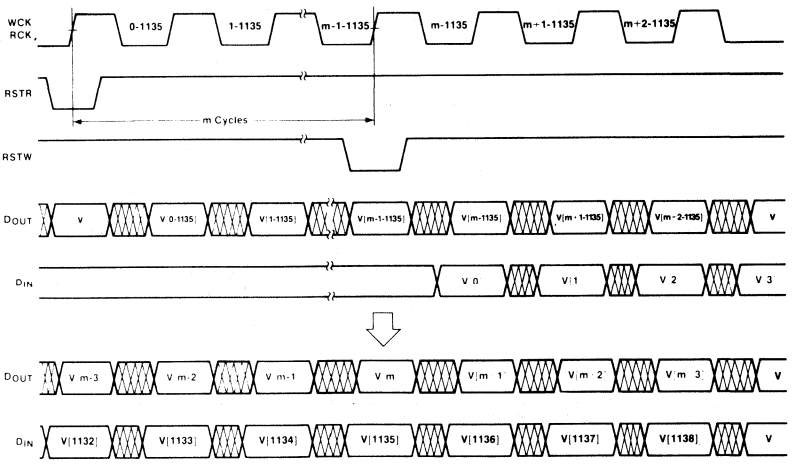
Note:
[1] V = Valid Data.

Read Disable



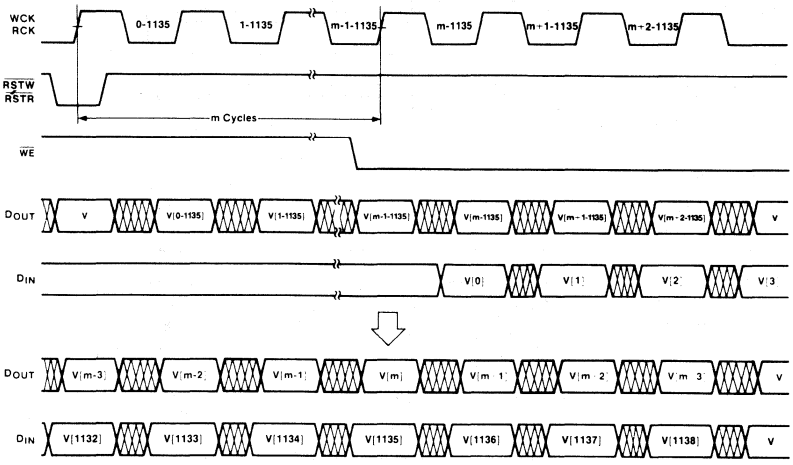
Note:
[1] V Valid Data.

(1135-m)-Bit Delay Line, No. 1



Note:
1 RE V_{IL}
2 V Valid Data.

(1135-m)-Bit Delay Line, No. 2



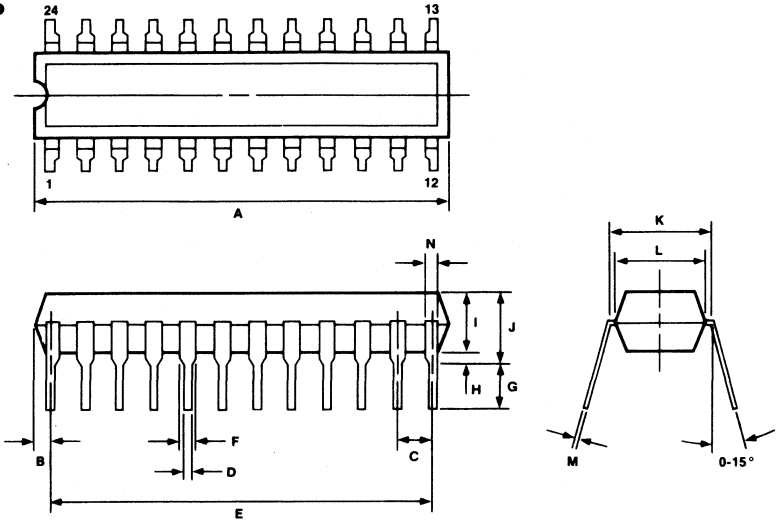
Note:
[1] $\overline{RE}$ V_{IL}.
[2] V Valid Data.

Package Dimensions

24 PIN Plastic DIP

μPD41102C

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.50 ± 0.3
H	0.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



5048 x 8-Bit FIFO Line Memory

Description

The μPD42505C is a high-speed, FIFO, 5,048 x 8-bit format line memory. It is fabricated using a silicon-gate CMOS process. This device allows independent write/read operations. Data can be read in the same order as is put during write operations due to the FIFO algorithm. Therefore, the μPD42505C can be used as a device for frequency (time-axis) conversion. In addition, the μPD42505C can be used as a digital delay line which has delay bits of 5,048 bits long or less.

The interface of the μPD42505C has independent modes for the WRITE CLOCK (WCK) and READ CLOCK (RCK). In order to control these modes,the μPD42505C has WRITE ENABLE ($\overline{WE}$) and READ ENABLE ($\overline{RE}$) control terminal pins. These pins can be used to prohibit write and read operations independently and in real time while a CLOCK is supplied. This is one of user-friendly aspects of the μPD42505C.

Also, using reset functions ($\overline{RSTW}$-$\overline{RSTR}$) which are independently provided for write/read operations, a write/read address can be initialized at any time for performing re-write and re-read operations.

The μPD42505C operates from a 5-Volt single power supply. It is housed in a 24-pin 300-mil dual in-line package (DIP).

Features

- 5048 x 8 bit organization.
- FIFO (First-In First Out) line memory
- Write/read operations in the asynchronous mode using different bit rates (at arbitrary different timings and cycles for operations), featuring a suitable configuration as a time-axis converter.
- Can be used as a delay line up to 5,048 bits; a delay bit-length variable one by one (10 bits for a minimum delay bit length).
- Can be used as an N (N=10 to 5,048) bit delay line using each pulse synchronized to horizontal scanning as a reset signal.
- TTL compatible
- Three-state outputs
- Single 5 V ± 10% power supply
- 24-pin, 300 mil DIP package

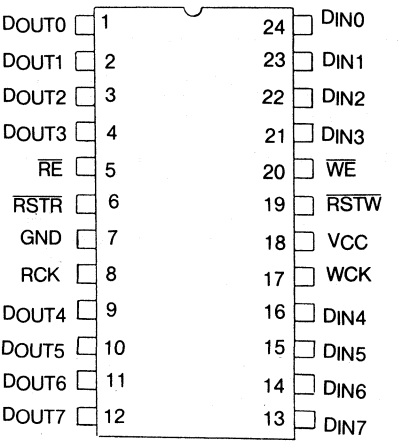
Performance ranges

Device	Read Cycle Time (Min.)	Read Access Time (Max.)	Write Cycle Time (Min.)
μPD42505C-50	50 ns	40 ns	50 ns
μPD42505C-75	75 ns	55 ns	75 ns

Pin Identification

No.	Symbol	Function
1-4, 9-12	D_{OUT0}-D_{OUT7}	Read data outputs
5	$\overline{RE}$	Read enable input
6	$\overline{RSTR}$	Read address reset input
7	GND	Ground
8	RCK	Read clock input
13-16, 21-24	D_{IN0}-D_{IN7}	Write data inputs
17	WCK	Write clock input
18	V_{CC}	5 V power supply
19	$\overline{RSTW}$	Write address reset input
20	$\overline{WE}$	Write enable input

Pin Configuration



Pin Functions

D_{IN0} to D_{IN7} (Data Inputs)
Write data inputs

D_{OUT0} to D_{OUT7} (Data Outputs)
These eight three states terminals are used as read data outputs.

$\overline{RSTW}$ (Write Adress Reset Input)
This input signal is for a reset of the internal write address pointer to 0.

$\overline{RSTR}$ (Read Address Reset Input)
This input signal is for a reset of the internal read address pointer to 0.

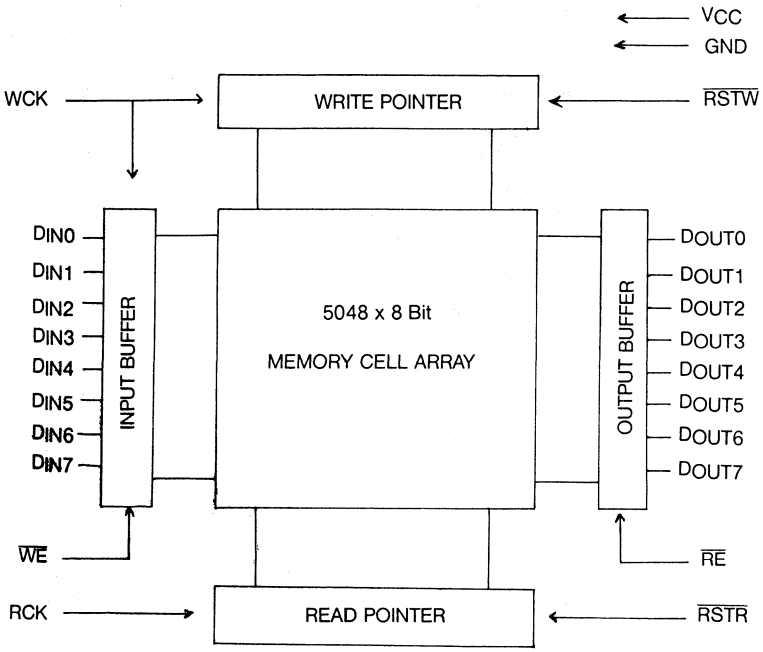
$\overline{WE}$ (Write Enable Input)
This input signal is a control signal to set either the ENABLE (LOW level) or the DISABLE (HIGH level) mode for the write operation. When this input is in the DISABLE mode, the write operation is prohibited within the chip and a write address is maintained at the current position i.e. the write address pointer stops increasing.

$\overline{RE}$ (Read Enable Input)
This input signal is a control signal to set either the ENABLE (LOW level) or the DISABLE (HIGH level) mode to the read operation. When this input is in the DISABLE mode, the read operation is prohibited within the chip and a read address is maintained at the current position. In addition, output goes to a HIGH impedance state.

WCK (Write Clock Input)
This input signal is a WRITE CLOCK signal. The write operation is carried out one at a time with a synchronization to write clock when $\overline{WE}$ is in the LOW level. A write address increases at every clock. Write data is output from the D_{OUT} terminal pins after a 5,048-bit delay when the μPD42505C is used a 1H (line) delay line.

RCK (Read Clock Input)
This input signal is a READ CLOCK signal. The read operation is carried out one at a time with a synchronization to READ CLOCK when $\overline{RE}$ is in the LOW level. A read address increases at every clock.

Block Diagram



Operation

Reset

The μPD42505C requires the initialization of internal circuits using reset signals ($\overline{RSTW}$/$\overline{RSTR}$) before starting operations as a time-axis converter and a digital delay line.
Resetting can be carried out at any time. Note that the reset signal must be supplied in order to satisfy the setup time and the hold time against the rise edge of the CLOCK signal (WCK or RCK). (See timing diagrams for time-axis conversion, 1 horizontal line delay, reread and reset).

Write/Read

Write/read operations are synchronized and carried out one at a time when WCK or RCK is in a HIGH level and while $\overline{WE}$ or $\overline{RE}$ is in a LOW level. Write data must be loaded to satisfy both the data setup time and the hold time against the rise edge of WCK. The access time of the reading operation is measured from the rise edge of RCK. This is defined by t_{ACR} for specifying an access during the first cycle directly after resetting and t_{AC} for specifying an access under other conditions. (See timing diagrams for write/read operation, time-axis conversion and reset).

Time axis conversion

In order to use the μPD42505C as a time-axis converter, write/read operations can be controlled independently. For example, write/read ports are initialized separately using the reset signal. Then, the write operation can be performend by synchronizing to WRITE CLOCK. Write data can be stored sequentially from address O of this device. Afterwards, if the read operation is carred out by synchronizing the READ CLOCK, write data can be read sequentially from address 0.
In this case, write/read operations can be performed independently as well as asynchronously with each other. Therefore, data loaded at an arbitary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD42505C can be used as time-axis converter. (See timing diagram for time-axis conversion).
Also, stored data can be read non-destructively so that data can be repeatedly read within a prescribed time (5 ms). (See timing diagram for 1 horizontal line delay).

Digital delay line

The μPD42505C can be used as a digital delay line, with easy operations, which has a delay length of 5,048 bits or less.
After initalizing the μPD42505C internal circuits using the $\overline{RSTW}$/$\overline{RSTR}$ signal, write/read operations are performed simultaneously by supplying the same pulse to the WRITE CLOCK (WCK) and READ CLOCK (RCK). The write data is always read after the 5,048-bit delay. This is the same function as the delay line.
In this case, if one of either $\overline{WE}$ or$\overline{RE}$ is set at a non-selective level (HIGH level) for a certain amount of cycles while maintaining the other in a selective level (LOW level), the delay bit number can be changed from the 5,048 bits.
For example, if only $\overline{WE}$ is set to a HIGH level (WRITE DISABLE), read operation is performed and the delay bit number goes small. In turn, only $\overline{RE}$ is set to a HIGH level (READ DISABLE), the write operation is performed and the delay bit number becomes large. Note that the minimum delay bit number is 10 bits and the maximum is 5,048 bits.(See timing diagram for write/read operation).
A data delay of 5,048 bits or less can also be obtained in the following way: WRITE RESET signal ($\overline{RSTW}$) and READ RESET signal ($\overline{RSTR}$) can be supplied a different time. For example, data is loaded within m cycles after WRITE RESET and then write data is read by supplying READ RESET.In this case, write data can be read from the beginning after m cycles. Therefore, the device can be used as an m-bit digital delay line.
Other usage of this memory as a delay line is as follows: the reset signals ($\overline{RSTW}$/$\overline{RSTR}$) can be simultaneously loaded at every 1H (horizontal line) period. In this case, write data which is loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay bit length ranging from 10 to 5,048 bits can be obtained according to the supply period of the reset signals. (See timing diagram for 1 horizontal line delay).

Cautions

In order to read out data on a write address, it must take ½ write cycle + 500 ns (at most) after writing the address.

Data on a write address must be read out within 5 ms (maximum) after writing the address.

Electrical Specifications

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short circuit output current, I_{OS}	20 mA
Ambient Temperature, T_A	0 to +70°C
Storage temperature, T_{STG}	−50 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

T_A = 0 to +70°C (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Ground	GND	0	0	0	V	
Input voltage high	V_{IH}	2.4		5.5	V	
Input voltage low	V_{IL}	−1.5		0.8	V	

Capacitance

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Note:
(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/Read cycle operating current	I_{CC}			120	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} is disabled; V_O = 0 to 5.5 V
Output voltage high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 2 mA

Note:
(1) All voltages are referenced to ground.

AC Characteristics

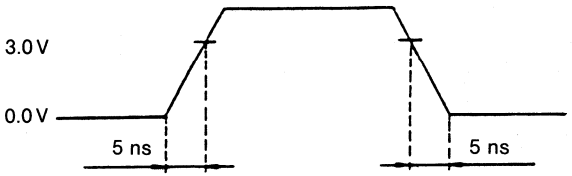
$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\,V \pm 10\%$ (Note 2, 3, 5)

Symbol	Parameter	Limits				Unit	Test Conditions
		μPD42505C-50		μPD42505C-75			
		Min	Max	Min	Max		
tWCK	WRITE CLOCK (WCK) Cycle Time	50	1000	75	1000	ns	Note 12
tWCW	WRITE CLOCK Set-Up Width	20		30		ns	
tWCP	WRITE CLOCK Precharge Width	20		30		ns	
tRCK	READ CLOCK (RCK) Cycle Time	50	1000	75	1000	ns	
tRCW	READ CLOCK Set-Up Width	20		30		ns	
tRCP	READ CLOCK Precharge Width	20		30		ns	
tAC	Access Time		40		55	ns	
tACR	Cycle Access Time after Reset		75		90	ns	
tOH	Output Hold Time	5		5		ns	
tOHR	Cycle Output Hold Time after Reset	5		5		ns	Note 7
tLZ	Output LOW Impedance Time	5	40	5	55	ns	Note 4
tHZ	Output HIGH Impedance Time	5	40	5	55	ns	Note 4
tDS	Input Data Set-Up Time	15		20		ns	
tDH	Input Data Hold Time	5		5		ns	
tRS	WCK or RCK Rise to RST Set-Up time	15		20		ns	Note 8
tRH	WCK or RCK Rise to RST Hold Time	5		5		ns	Note 8
tRN1	WCK or RCK Rise to RST Non-Selective Time 1	5		5		ns	note 9
tRN2	WCK or RCK Rise to RST Non-Selective Time 2	15		20		ns	Note 9
tWES	WCK Rise to WE Set-Up Time	15		20		ns	Note 10
tWEH	WCK Rise to WE Hold Time	5		5		ns	Note 10
tWEN1	WCK rise to WE Non-Selective Time 1	5		5		ns	Note 11
tWEN2	WCK Rise to WE Non-Selective Time 2	15		20		ns	Note 11
tRES	RCK Rise to RE Set-Up Time	15		20		ns	Note 10
tREH	RCK Rise to RE Hold Time	5		5		ns	Note 10
tREN1	RCK Rise to RE Non-Selective Time 1	5		5		ns	Note 11
tREN2	RCK Rise to RE Non-Selective Time 2	15		20		ns	Note 11
tWEW	WE HIGH Level Width	0	Note 6	0	Note 6	ms	
tREW	RE HIGH Level Width	0	Note 6	0	Note 6	ms	
tRSTW	RSTW LOW Level Width (WRITE RESET Width)	0	Note 6	0	Note 6	ms	
tRSTR	RSTR LOW Level Width (READ RESET Width)	0	Note 6	0	Note 6	ms	
tT	Input Transition Time (Rise and Fall)	3	35	3	35	ns	

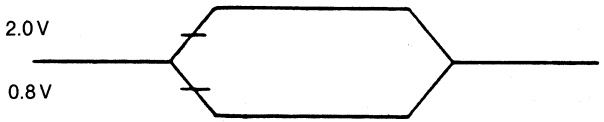
Note 1. All voltages must be referenced to GND.
2. All voltages should be measured at $tT = 5$ ns.
3. Reference levels of input voltages for measuring timing are VIH at 3.0 V and VIL at 0.0 V. Also, the transition time, tT, is measured between VIH and VIL.
4. t_{LZ} and t_{HZ} are measured at a stable state ± 200 mV. Note that $t_{LZ} \geqq t_{HZ}$.
5. The reference level of input signal is 1.5 V.
6. For Max specifications, the following conditions must be satisfied during a one line cycle: $t_{WEW} \leqq 5$ ms − 5000 t_{WCK} − t_{RSTW} and $t_{REW} \leqq 5$ ms − 5000 t_{RCK} − t_{RSTR}.
7. Should be applied only when t_{RCK} is greater than or equal to 70/90 ns.
8. If reset pulse which does not satisfy t_{RS} and t_{RH} is loaded, reset operation is not guaranteed.
9. If reset pulse which does not satisfy t_{RN1} and t_{RN2} is loaded, reset operation may fail to complete within one cycle.
10. If $\overline{WE}$ ($\overline{RE}$) pulse which does not satisfy t_{WES} and t_{WEH} (or t_{RES} and t_{REH}) is loaded, WRITE (READ) DISABLE operation is not guaranteed.
11. If $\overline{WE}$ ($\overline{RE}$) pulse which does not satisfy t_{WEN1} and t_{WEN2} (or t_{REN1} and t_{REN2}) is loaded, WRITE (READ) DISABLE operation may not be fit within one cycle.
12. Two values in the specifications correspond to the DASH 50 and the DASH 75 respectively.

AC Electrical Characteristic Test Condition

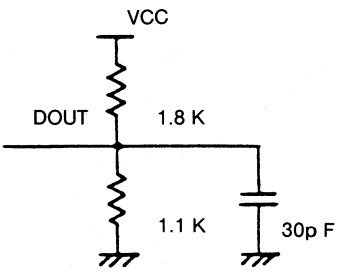
Input Timing



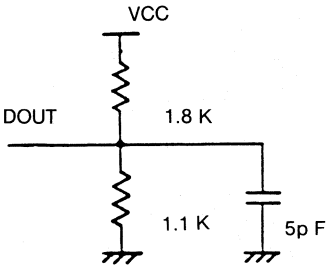
Output Timing



Dout Load

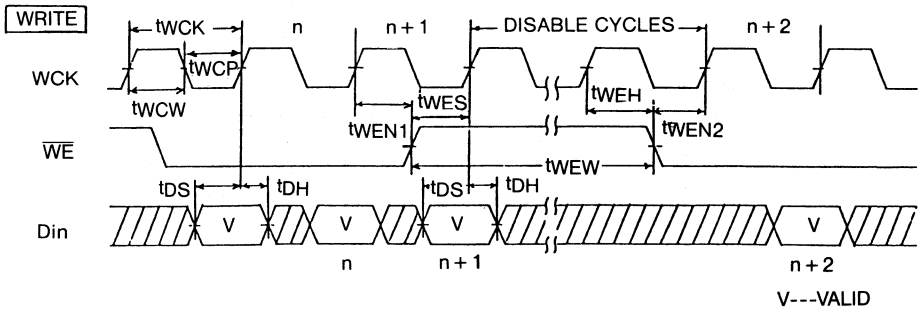


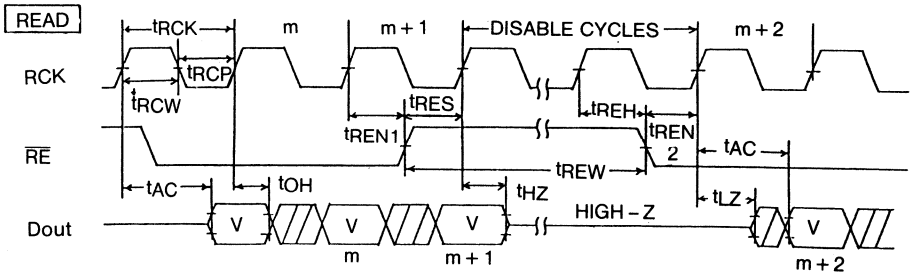
(tAC, tACR, tOH, tOHR)



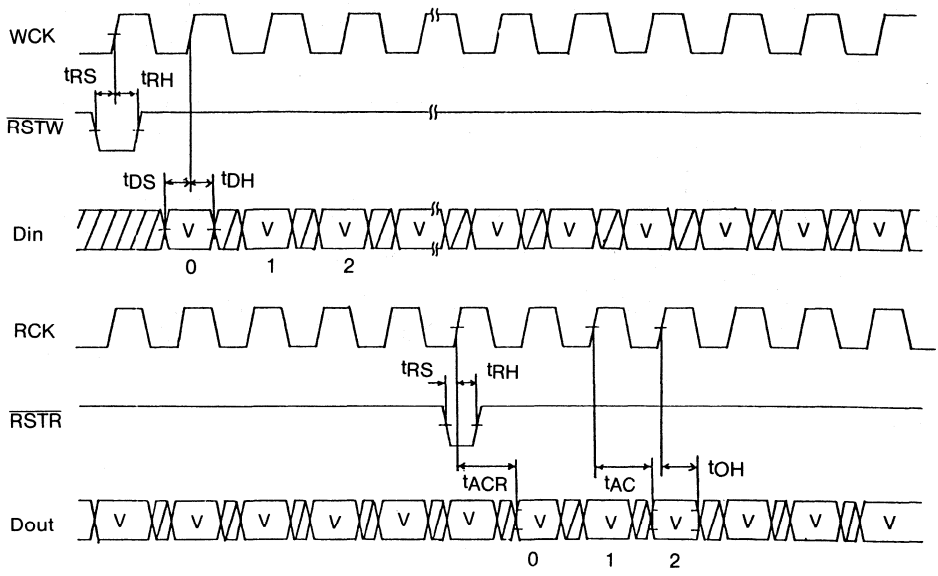
(tLZ, tHZ)

Timing for write/read operation

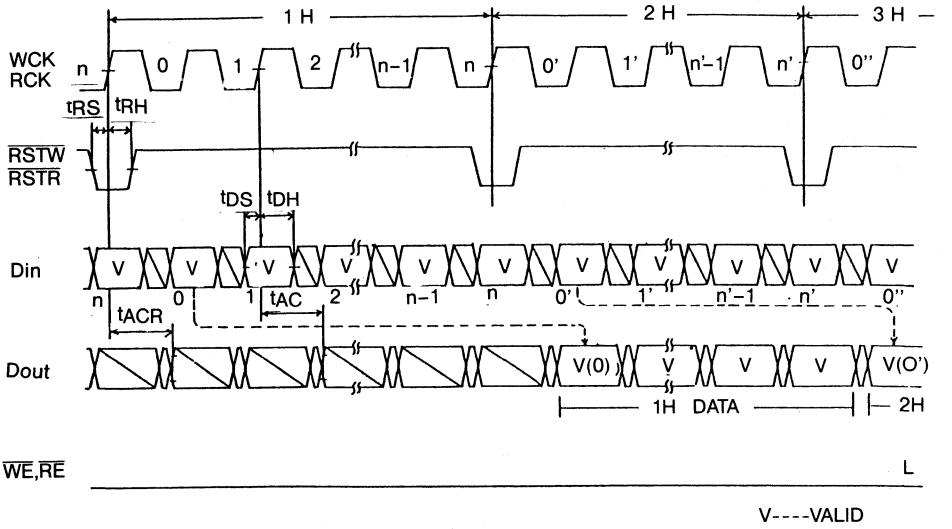




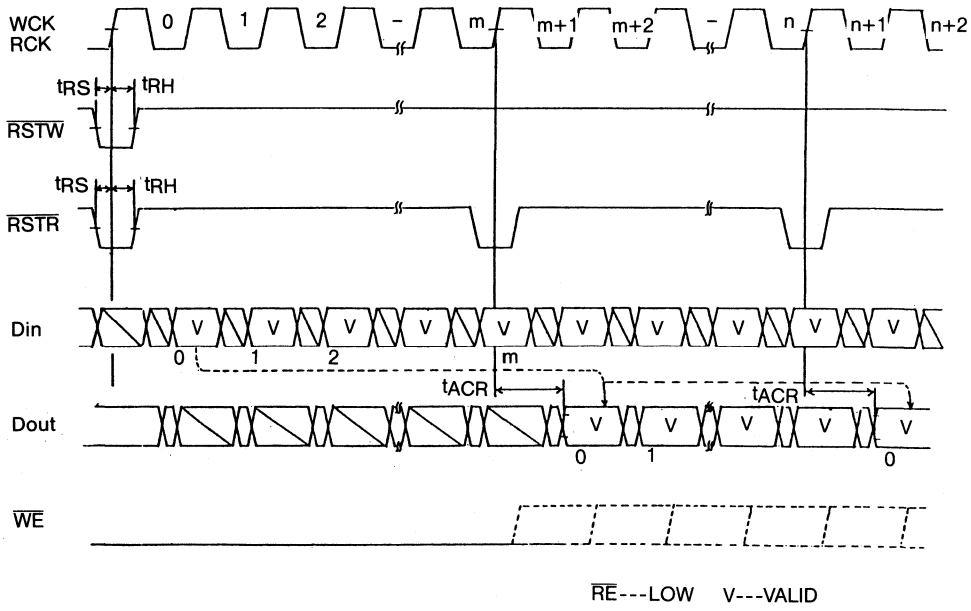
Timing for time – axis conversion



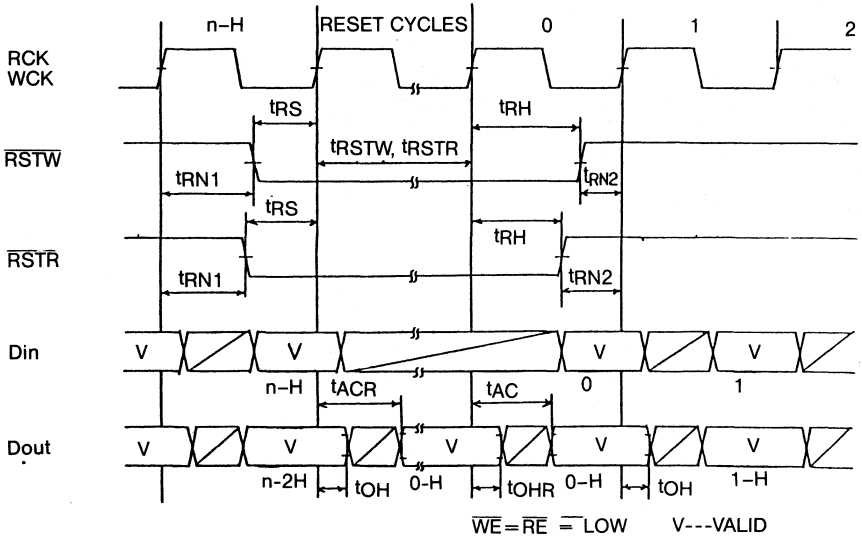
Timing for 1 horizontal line delay



Timing for reread



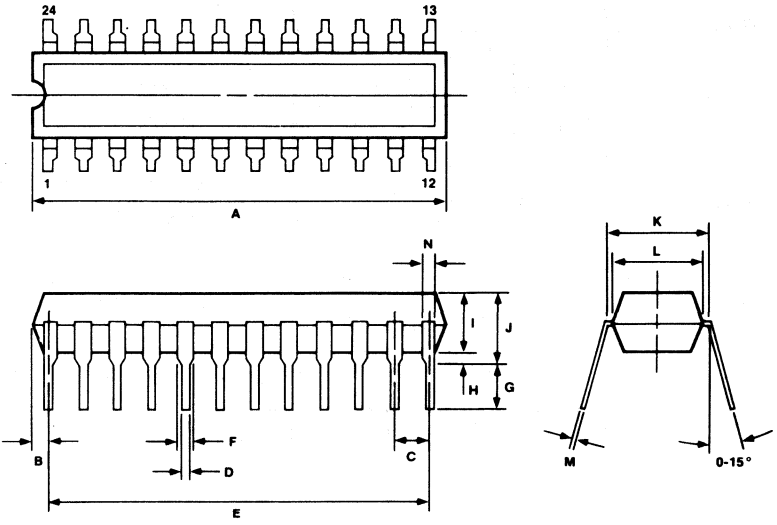
Timing for reset



Package dimensions

24 PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.50 ± 0.3
H	0.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



MOS DIGITAL INTEGRATED CIRCUIT

224,000-BIT SERIAL ACCESS MEMORY

Description

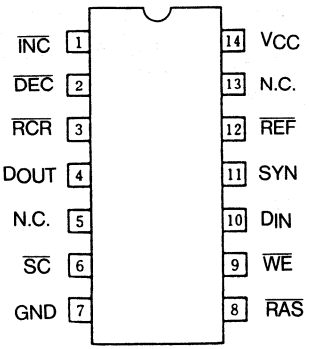
μPD41221C is a 224K-word x 1-bit high-speed serial access memory featuring a 320-row x 700-column memory configuration. A number of features have been specifically incorporated to simplify system configurations in video applications. These include a built-in 700-bit line buffer to enable high-speed input and output of one line (700 bits) of data, 70 and 90 nsec reading and writing capabilities, and refresh cycle asynchronous with data input and output.
And since serial accessing is the main operating mode when used as a field/frame memory, accessing in the row direction is completely serial accessing, thereby eliminating the need for column inputs. And since row-direction accessing involves counting up, down, and resetting of only the three inputs $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$, address inputs are no longer required. The device can thus be mounted in a compact 14-pin 400 mil package. Two types μPD41221C are available depending on the cycle time.

Features

Device	Serial cycle time	Serial access time	Current consumption (serial cycle)	Current consumption (data transfer cycle)
μPD41221C-70	70 ns	55 ns	55 mA	45 mA
μPD41221C-90	90 ns	75 ns	45 mA	45 mA

- Configuration: 224K (320 rows x 700 columns) words x 1 bit
- Built-in 700-bit column-handling line buffer
- Built-in refresh control circuit
- Power supply voltage $V_{CC} = 5\ V \pm 10\%$
- Input voltage level TTL level
- Output voltage level $V_{OH}/V_{OL} = 0.7 \times V_{CC}/0.2 \times V_{CC}$
- Refresh cycle 320 times every 2 msec.

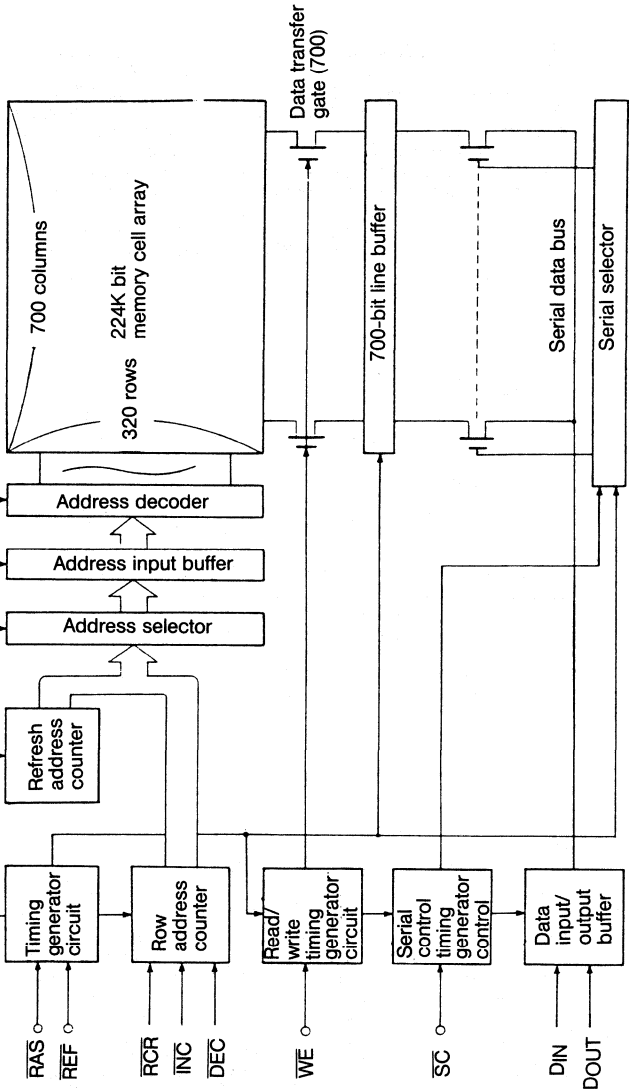
μPD41221C Pin Layout



$\overline{RAS}$: Data transfer/restore control clock input
$\overline{WE}$: Read/write control input
$\overline{SC}$: Serial control clock input
$\overline{REF}$: Refresh control clock input
$\overline{INC}$: Row counter increment clock input
$\overline{DEC}$: Row counter decrement clock input
$\overline{RCR}$: Row counter reset clock input
DIN : Data input
DOUT : Data output
SYN : Synchronization timing output
V_{CC} : Power supply voltage
GND : Ground

Note: Leave N.C. pins open.

BLOCK DIAGRAM



Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Pin voltage	V_T		−1.0 to +7.0	V
Power supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Operating temperature	T_{opt}		−10 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Recommended Operating Temperature

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		5.5	V
Low level input voltage	V_{IL}		−1.0		0.8	V

DC Characteristics (when operating under recommended conditions)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Standby power supply current	I_{CC1}	I_O = 0 mA (DOUT, SYN) $\overline{RAS}$, SC, $\overline{REF}$, $\overline{INC}$, $\overline{DEC}$ $\overline{RCR}$ = V_{IH}		15	mA
Input leak current	I_I	V_I = 0 thru 5.5 V, Other inputs = 0 V	−10	10	μA
Output leak current	I_O	DOUT is inactive V_{OUT} = 0 thru 5.5 V	−10	10	μA
High level output voltage	V_{OH}	I_{OH} = −20 μA	0.7 x V_{CC}	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 20 μA	0	0.2 x V_{CC}	V

Input/Output Capacitance (V_{CC} = 5 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	$\overline{RAS}$, $\overline{SC}$, $\overline{REF}$, $\overline{INC}$ $\overline{DEC}$, $\overline{RCR}$, $\overline{WE}$, D_{IN}		10	pF
Output capacitance	C_O	DOUT, SYN		10	pF

AC Characteristics (when operating under recommended conditions)

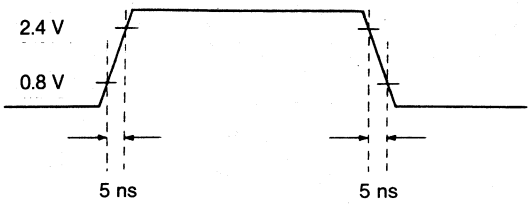
Parameter	Symbol	μPD41221C-70		μPD41221C-90		Unit	Remarks
		MIN.	MAX.	MIN.	MAX.		
Data transfer cycle power supply current	I_{CC2}		45		45	mA	
Data restore cycle power supply current	I_{CC3}		40		40	mA	
Refresh cycle power supply current	I_{CC4}		40		40	mA	
Serial read cycle power supply current	I_{CC5}		55		45	mA	
Serial write cycle power supply current	I_{CC6}		55		45	mA	
Row counter reset cycle power supply current	I_{CC7}		20		20	mA	
Row counter increment cycle power supply current	I_{CC8}		20		20	mA	
Row counter decrement cycle power supply current	I_{CC9}		20		20	mA	
$\overline{RAS}$ cycle time	t_{RC}	710		710		ns	
$\overline{RAS}$ pulse width	t_{RAS}	500	2000	500	2000	ns	
$\overline{RAS}$ precharge time (data restore – data transfer time)	t_{RP}	200		200		ns	
$\overline{RAS}$-$\overline{REF}$ delay time	t_{RFD}	200		200		ns	
$\overline{RAS}$-$\overline{SC}$ delay time	t_{RSD}	300		300		ns	
Read command-set-up time for $\overline{RAS}$ (data transfer cycle)	t_{RRS}	0		0		ns	
Read command hold time for $\overline{RAS}$) (data transfer cycle)	t_{RRH}	20		20		ns	
$\overline{REF}$ precharge time for $\overline{RAS}$	t_{FRP}	200		200		ns	
$\overline{SC}$ precharge time for $\overline{RAS}$	t_{SRP}	200		200		ns	
$\overline{WE}$ set-up time for $\overline{RAS}$ (data restore cycle)	t_{WRS}	0		0		ns	
$\overline{WE}$ hold time for $\overline{RAS}$ (data restore cycle)	t_{WRH}	50		50		ns	
Data output off time for $\overline{RAS}$	t_{RSZ}	0	400	0	400	ns	
$\overline{REF}$ cycle time	t_{FC}	710		710		ns	
$\overline{REF}$ pulse width	t_{REF}	500		500		ns	
$\overline{REF}$ precharge time	t_{FP}	200		200		ns	
$\overline{SC}$ cycle time	t_{SC}	70		90		ns	
$\overline{SC}$ pulse width	t_{SA}	25	2000	35	2000	ns	
$\overline{SC}$ precharge time	t_{SP}	25	2000	35	2000	ns	
$\overline{WE}$ set-up time for $\overline{SC}$ (serial write cycle)	t_{WSS}	0		0		ns	
$\overline{WE}$ hold time for $\overline{SC}$ (serial write cycle)	t_{WSH}	25		25		ns	
Read command set-up time for $\overline{SC}$ (serial read cycle)	t_{RSS}	0		0		ns	
Read command hold time for $\overline{SC}$ (serial read cycle)	t_{RSH}	20		30		ns	
Input data set-up time for $\overline{SC}$	t_{DSS}	0		0		ns	
Input data hold time for $\overline{SC}$	t_{DSH}	25		35		ns	
$\overline{SC}$ access time	t_{SAC}		55		75	ns	

AC Characteristics (when operating under recommended conditions)

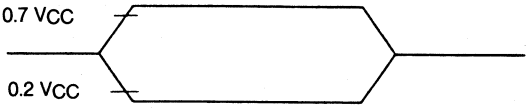
Parameter	Symbol	μPD41221C-70		μPD41221C-90		Unit	Remarks
		MIN.	MAX.	MIN.	MAX.		
Data output off time for $\overline{SC}$	tSCZ	5	40	5	60	ns	
$\overline{RAS}$-$\overline{RCR}$ delay time	tRRD	200		200		ns	
$\overline{RAS}$-$\overline{INC}$ delay time	tRID	200		200		ns	
$\overline{RAS}$-$\overline{DEC}$ delay time	tRDD	200		200		ns	
$\overline{RCR}$ pulse width	tRCR	100		100		ns	
$\overline{INC}$ pulse width	tINC	100		100		ns	
$\overline{DEC}$ pulse width	tDEC	100		100		ns	
$\overline{RCR}$-$\overline{INC}$ interval	tRIP	100		100		ns	
$\overline{INC}$-$\overline{DEC}$ interval	tIDP	100		100		ns	
$\overline{RCR}$-$\overline{DEC}$ interval	tRDP	100		100		ns	
$\overline{RCR}$ precharge time for $\overline{RAS}$	tRRP	100		100		ns	
$\overline{INC}$ precharge time for $\overline{RAS}$	tIRP	100		100		ns	
$\overline{DEC}$ precharge time for $\overline{RAS}$	tDRP	100		100		ns	
SYN output delay time for $\overline{SC}$ (after 605 $\overline{SC}$ cycles)	tSYA		200		200	ns	
SYN recovery time for $\overline{RAS}$	tSYR	0	1400	0	1400	ns	
Refresh interval	tREF		2		2	ms	
$\overline{RAS}$ precharge time (serial operation period)	tRPS		2		2	ms	
Serial data valid output period	tSOV		2		2	ms	
Input leading and trailing edge times	tT	3	35	3	35	ns	

● AC characteristics test conditions

1. Input timing rating (leading and trailing egde timing)



2. Output judgement timing rating and load conditions



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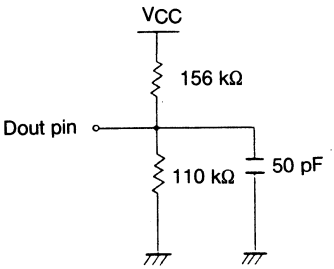

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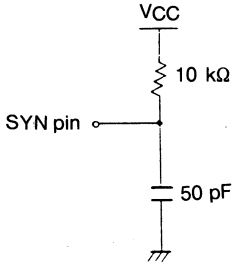


Cautions

1. All voltages are specified in reference to V_{SS} (GND).
2. At least eight dummy cycles each for $\overline{RAS}$, $\overline{REF}$, $\overline{RCR}$,$\overline{INC}$, and $\overline{DEC}$ following a minimum of 2 msec after the power supply is switched on (that is, after $V_{CC} = 4.5$ is attained). (Dummy cycles are not required for $\overline{DEC}$ if this signal is not used in the system.)
3. Execute measurement at $t_T = 5$ ns.
4. The input voltage references level for timimg ratings are V_{IH} (MIN) and V_{IL} (MAX). Transition time t_T is to be define between V_{IH} (MIN) and V_{IL} (MAX).
5. The t_{RSZ} and t_{SCZ} parameters are to be defined as the time taken for the output to attain open status. Since output data is actually left behind due to the large time constants in HCMOS, these parameters serve as reference specification ratings.
6. The memory power supply (V_{CCM}) must be related to the peripheral HCMOS power supply (V_{CCH}) in the following way.
   $V_{CCH} \leqq V_{CCM} \pm 0.1$ V
   This specification is necessary to maintain the speed ratings.

1. Input/Output Pin Functions

The μPD41221C device is equipped with $\overline{RAS}$, $\overline{WE}$, $\overline{SC}$, $\overline{REF}$, $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$ clock input pins plus D_{IN}, D_{OUT}, and SYN input/output pins.

- RAS — μPD41221C has a 320-row x 700-column memory configuration (see block diagram), and a built-in 700-bit line buffer for a single row. The $\overline{RAS}$ clock input controls reading and writing of one row of data between the memory cell array and line buffer according to the $\overline{WE}$ signal level. (Data transfer/data restore cycle)
- $\overline{WE}$ — Read/write control input
  The $\overline{WE}$ input controls data transfer/data restore cycles and serial read/write cycles. The operation controlled is determined by the trailing edge of the $\overline{RAS}$ clock input if in a data transfer/data restore cycle, and by the trailing edge of the $\overline{SC}$ clock if in a serial read/write cycle.
- $\overline{SC}$ — Serial control clock input
  The $\overline{SC}$ clock input controls line buffer serial read/write operations. Serial operations are enabled in 70 nsec (max.) in μPD41221C-70, and 90 nsec (max.) in μPD41221C-90.
- $\overline{REF}$ — Refresh control clock input
  If the $\overline{REF}$ clock is applied while the $\overline{RAS}$ clock input is inactive, an on-chip refresh operations is executed by the built-in refresh control circuit.
- $\overline{INC}$, $\overline{DEC}$, $\overline{RCR}$ — Row address counter clock input. Control of row address by input of the respective $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$ clocks. Row address increment (+1) is executed by $\overline{INC}$ clock input row address decrement (−1) is executed by $\overline{DEC}$ clock input, and row address counter reset (reset to address 0) is executed by $\overline{RCR}$ clock input.
- D_{IN}, D_{OUT} — Data input and output
  Data input is separated from data output in μPD41221C to enable easier control of the high-speed serial cycle.
  And with the D_{OUT} output level at $V_{OH}/V_{OL} = 0.7\ V_{CC}/0.2\ V_{CC}$, low power consumption HCMOS loads have been made possible.
- SYN — Synchronizing signal output
  When more than 605 consecutive cycles of serial read/write are executed by $\overline{SC}$ clock input, the SYN output is changed to low level until the next $\overline{RAS}$ cycle (data transfer, restore cycle).
- N.C. — Open pin

2. μPD41221C Operations

(1) μPD41221C Configuration

See the μPD41221C block diagram

The μPD41221C memory cell array consists of 1-transistor dynamic memory cell with a 320-bit (row) x 700-bit (column) configuration. This configuration is especially useful in video signal digital processing applications. The low cost-performance memory is suitable for both the NTSC system (used in Japan and U.S.A.) and the PAL system (used in European countries).

Furthermore, μPD41221C is equipped with a 700-bit high-speed line buffer capable of handling 700 bits per row, thereby matching the bit-unit speed without additional circuitry. In addition to enabling 70 and 90 nsec cycle times, this also permits data input and output to be executed in parallel with memory cell refresh operations. And since the video signal storage (memory read/write) is adequate for serial access data input/output apart from video signal processing where bit-unit random access occurs, no external address needs to be applied, and accessing in the row direction only requires three signals $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$.

(2) μPD41221C reading and writing

- Serial read/write cycle

  Serial read/write cycles become high-speed cycles only when reading/writing is executed between the line buffer and the data input/output pin. These cycles are determined by the $\overline{WE}$ input level at the trailing edge of the $\overline{SC}$ clock input. A serial read cycle is set if the level is "H" (inactive), and a serial write cycle if "L" (active).

  In both serial read and write cycles, D_{OUT} is switched to low impedance by t_{SAC}. Data transferred to the line buffer during the previous data transfer cycle in a serial read cycle, and data fetched from D_{IN} at the $\overline{SC}$ clock trailing edge in a serial write cycle is passed to the output and held until the next $\overline{SC}$ or $\overline{RAS}$ clock trailing edge. And if more than 700 consecutive serial real read cycles are executed, D_{OUT} is maintained at high level by t_{SAC} since the line buffer data to be output is cleared. Since the μPD41221C line buffer is a data selector type, and because column counter is always reset to 0 by the $\overline{SC}$ clock when the $\overline{RAS}$ clock input is applied, the read and write positions are always matched even if less than 700 serial read/write cycles are executed.

  And since the μPD41221C line buffer consists of dynamic circuitry, the line buffer data following data transfer or a serial write operation is maintained at the maximum of 2 msec irregardless of the $\overline{SC}$ clock input. This point should be kept in mind in applications where low-speed reading or writing is executed.

- Refresh cycle

  Refresh cycles in μPD41221C are execued by input of at least 320 $\overline{REF}$ clocks per 2 msec. This refresh cycle can be executed by $\overline{RAS}$ clock asynchronously from other cycles apart from the data transfer and data restore cycles.

- Data transfer and retore cycles

  The purpose of the 700-bit line buffer in μPD41221C is to enable the device to cope with high-speed operations in video signal display etc. Therefore, all data writing and reading to/from memory cells is executed via this line buffer. The cycle where data is read from memory cell to line buffer is called the data transfer cycle, and the cycle where data is written from line buffer to memory cell is called the data restore cycle.

  The data transfer and restore cycle operations are decided by the level of the $\overline{WE}$ input at the $\overline{RAS}$ clock trailing edge. A data transfer cycle is selected if the level is "H" (inactive), and a data restore cycle is selected if the level is "L" (active).

  Since the μPD41221C memory cell is a 1-transistor type connected to dynamic type peripheral circuits, special attention must be paid in switching the $\overline{REF}$ clock input to "H" level (inactive) and to the timing specifications t_{RAS} and t_{RP} of the $\overline{RAS}$ clock input.

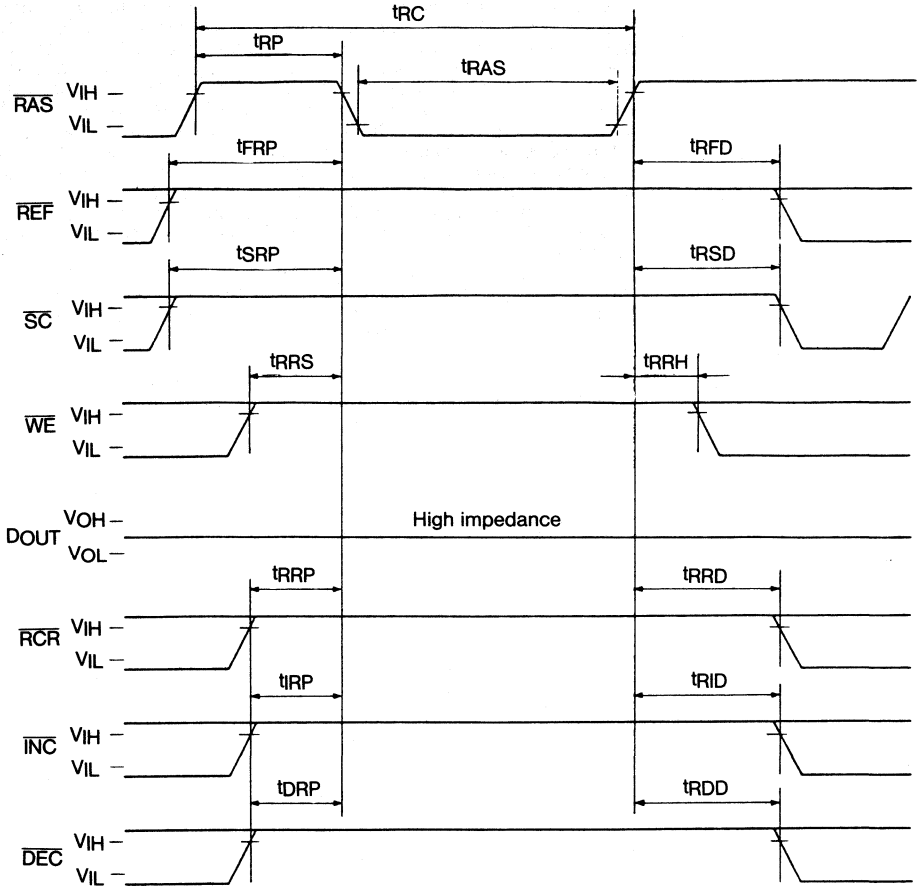
- Row counter control cycle

  Row address control is achieved by resetting (to address 0), incrementing, and decrementing of the respective $\overline{RCR}$, $\overline{INC}$, and $\overline{DEC}$ clock inputs. Note that the row address does not become valid until the next data transfer cycle where it is fetched by the address input buffer. Therefore, data written into the line buffer during a serial write cycle is written by data restore cycle into a memory cell corresponding to the row address specified by the previously executed data transfer cycle. Consequently, to write data into the next row address, the data transfer cycle must be executed again, and the row address has been changed, the serial write and data restore cycles must be repeated.

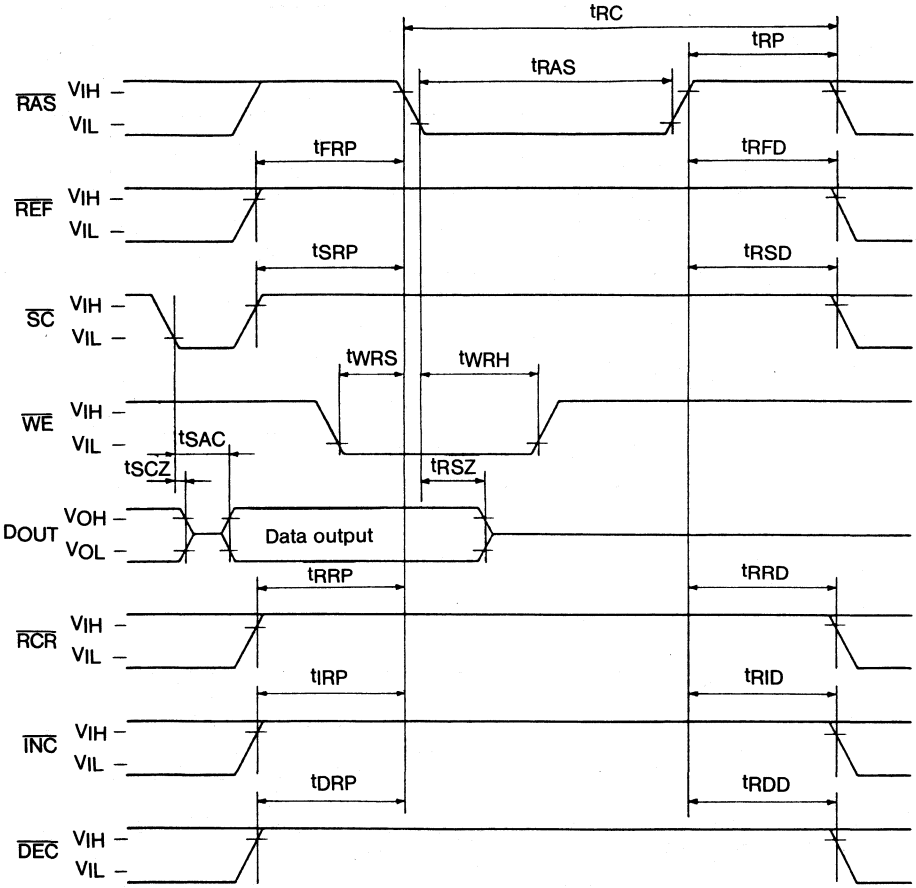
  $\overline{INC}$ and $\overline{DEC}$ addresses are selected by the number of input clocks up to the next data transfer cycle. That is, three consecutive $\overline{INC}$ inputs result in the address being advanced by three lines. And three consecutive $\overline{INC}$ inputs followed by two $\overline{DEC}$ inputs results in the address being advanced by one line. Repeating the $\overline{RCR}$ input any number of times does not interfere with the operation.

  When an $\overline{INC}$ clock input is entered after the row address has reached 319 (from address 0), and when a $\overline{DEC}$ clock input is entered after the address has been returned to 0, and $\overline{RCR}$ clock input must always be applied to reset the address row counter contents.

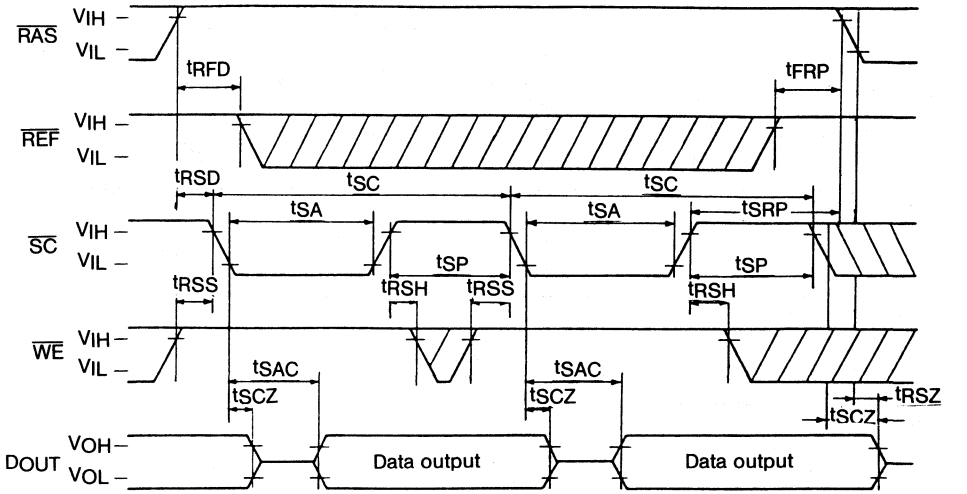
Data Transfer cycle (memory cell to line buffer)



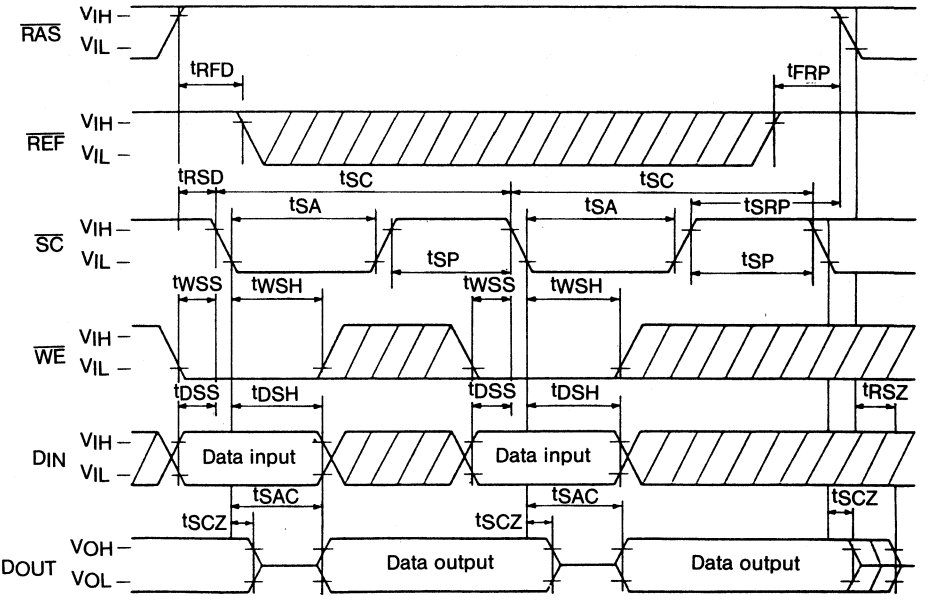
Data Restore Cycle (line buffer to memory cell)



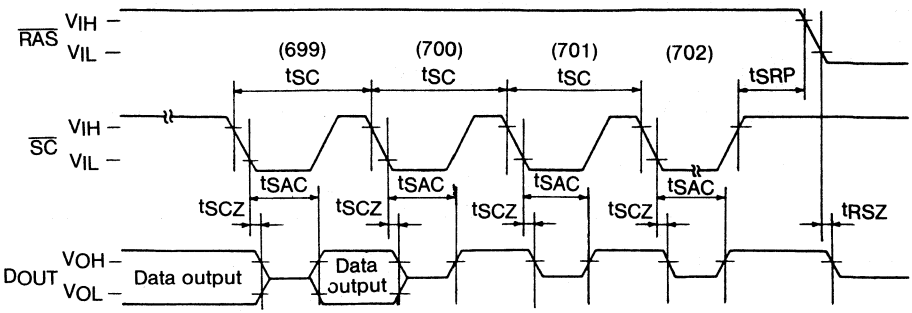
Serial Read Cycle



Serial Write Cycle

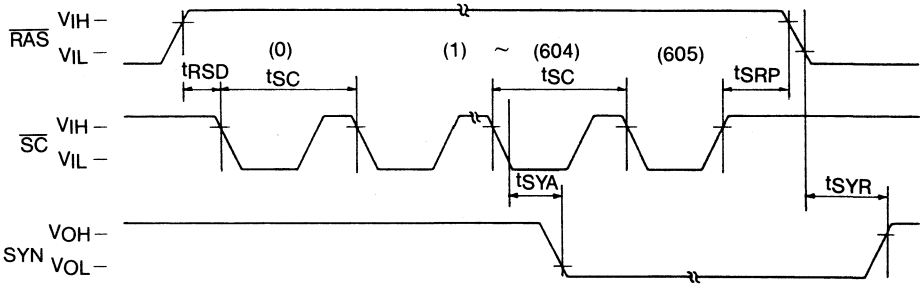


Serial Read Cycle Output Control



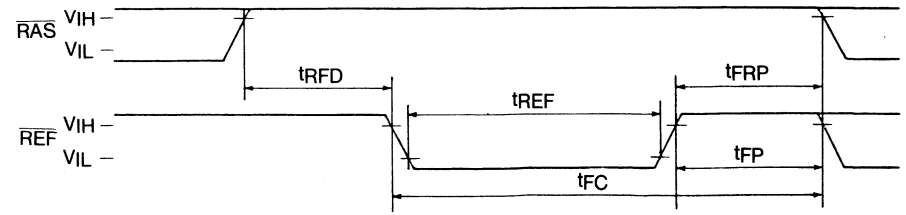
*DOUT is high-level output after 700 $\overline{SC}$ cycles

SYN Output

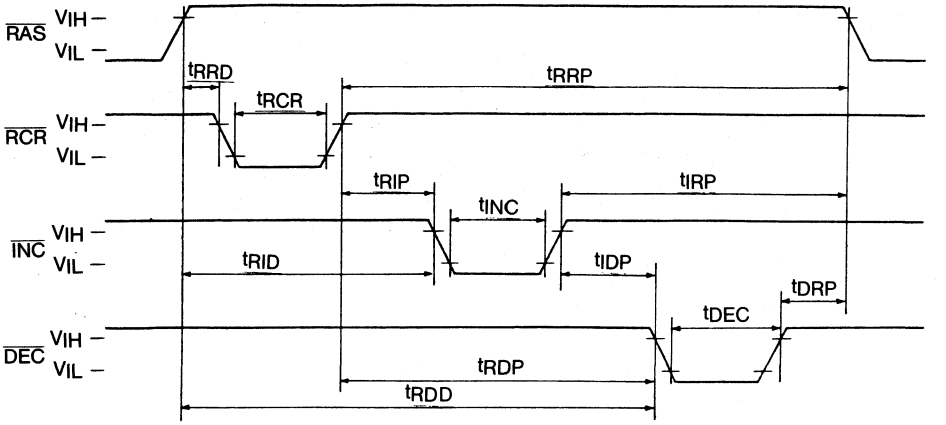


*SYN is low-level output after 605 $\overline{SC}$ cycles. This applies to both serial read and write cycles.

Refresh Cycle



Row Counter Cycle



3. μPD41221C Overall Timing

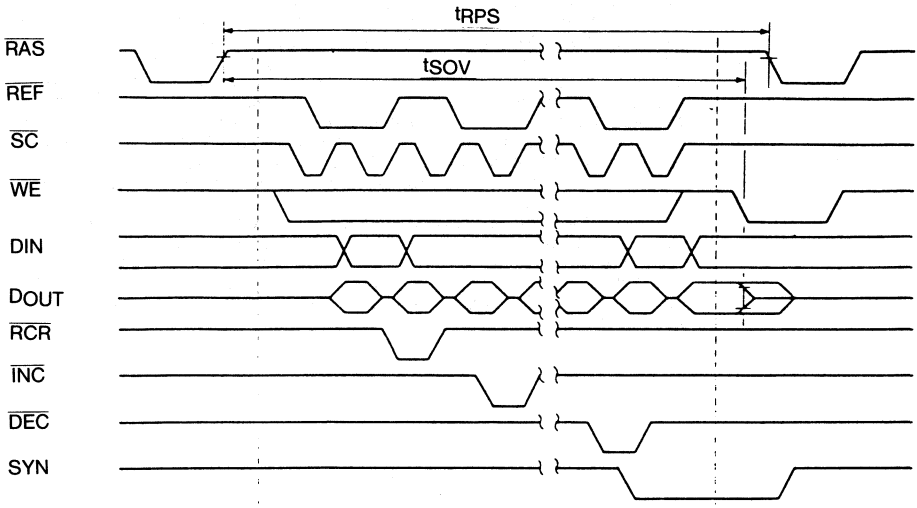
The μPD41221C device has been specifically designed for use as a video applications memory. Best results are obtained where read and write operations are set as next cycle operations.

The basic overall timing covers data transfer, serial read/write, and data restore cycle. A $\overline{WE}$ clock is switched to "L" (active) during a serial cycle only when input video data etc. is applied, resulting in one row of data being stored in a memory cell. The $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$ clock inputs which control the row counter are only entered during serial cycles when required. To ensure that the next data transfer cycle is at the specified position (for example, when storing one screen of video signal from a TV system) it is recommended that the $\overline{RCR}$ clock be formed from the vertical synchronizing signal, and include a control circuit for input of one INC clock in each horizontal scan line.

The correspondence between the display screen and memory cell array in this case consists of horizontal scanning executed in the column direction (700 bits) and vertical scanning in the row direction (320 bits).

Also note that input of at least one $\overline{REF}$ clock every 6.25 μsec (2 msec : 320 times) during serial cycles enables clocks obtained by dividing the $\overline{SC}$ clock to be used.

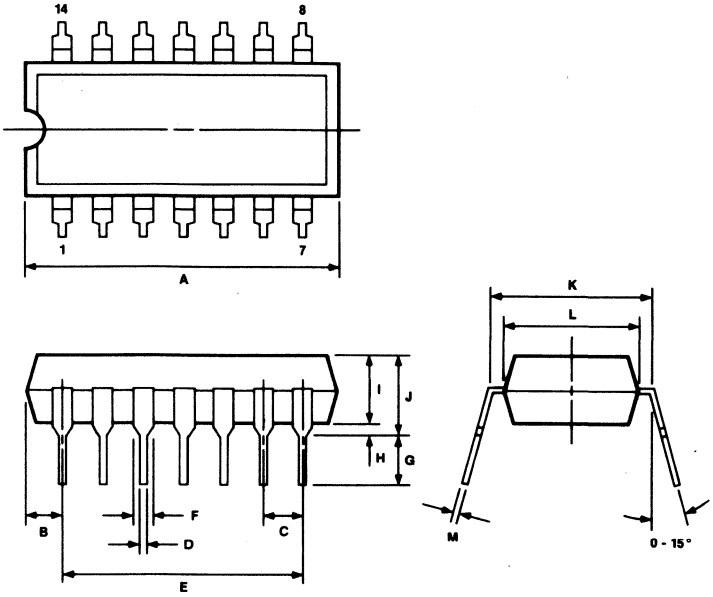
μPD41221C Overall Timing



Data transfer	○		
Data restore			○
Refresh		○	
Serial write		○	
Serial read		○	
Row counter reset		○	○
Row counter increment		○	○
Row counter decrement		○	○

Package Dimensions
14-Pin Plastic DIP

Item	Millimeters
A	20.32 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	15.24
F	1.2 min
G	3.2 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	10.16 [TP]
L	8.6
M	$.25^{+.10}_{-.05}$



262 144 BIT DUALPORT DYNAMIC RAM

Description

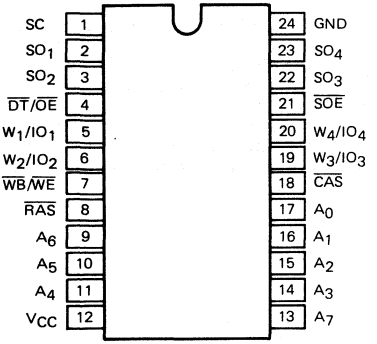
The NEC μPD41264C is a dual port dynamic RAM with a RAM port consisting of a 256 K bit (64 K words x 4 bits) memory cell array and a serial read port that allows clock operation at a maximum of 25 MHz from the 256 words x 4 bits data register. It realizes large capacity and low level of power dissipation by using one transistor dynamic memory cells and dynamic peripheral circuits.
The organization of RAM and serial read port is x 4 bit. It realizes simple structure of image buffer memory design and various applications requiring high speed processing. The 4 bit RAM port allows data to be written bit by bit for easy execution of bit processing at high speed.
It uses a 24 pin, 400 mil plastic DIP.

Features

FAMILY	Access Time t_{RAC}	Cycle Time t_{RC}	SC Cycle Time t_{SCC}	Power Dissipation I_{CC1}	Power Dissipation I_{CC8}
μPD41264C-12	120 ns	220 ns	40 ns	95 mA	60 mA
μPD41264C-15	150 ns	270 ns	60 ns	85 mA	45 mA

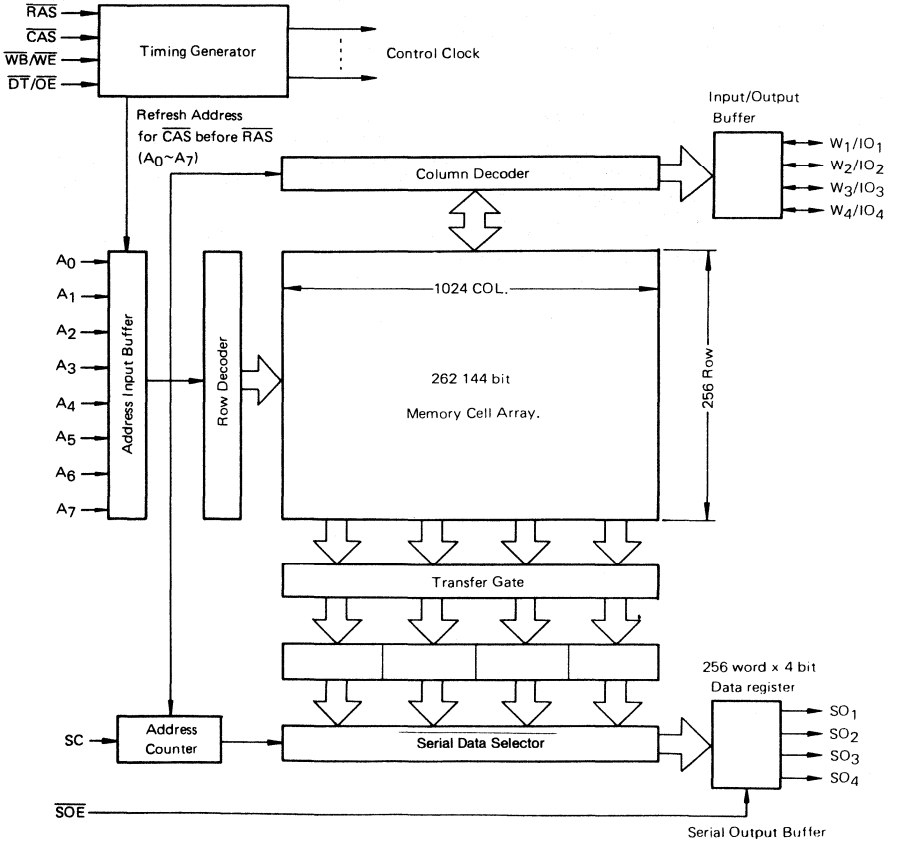
- Dual port organization — 64 K words x 4 bits RAM port; 256 words x 4 bits serial read port
- Data transfer capability from memory cell array to 1024 bits data register.
- Unsynchronous operation capability between RAM and serial read port.
- Pointer control capability.
- Write per bit capability.
- Page mode, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh capability.
- 256 cycle/4 ms refresh interval.
- Input/Output level is TTL compatible.

PIN CONFIGURATION



SC	:	Serial Control clock input
SO_1~SO_4	:	Serial Data Output
$\overline{DT}$	:	Data Transfer control input
$\overline{OE}$	:	Output Enable input
W_1~W_4	:	Write per bit mode selection data input
IO_1~IO_4	:	Data Input/Output
$\overline{WB}$	:	Write per bit control input
$\overline{WE}$	:	Write Enable input
$\overline{RAS}$	:	Row Address Strobe input
A_0~A_7	:	Address input
$\overline{CAS}$	:	Column Address Strobe input
$\overline{SOE}$	:	Serial Output Enable input
V_{CC}	:	Power supply
GND	:	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}		−1.0 to +7.0	V
Terminal Voltage	V_T	All of Input, Output Pins	−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1.5	W
Operation Temperature	T_{opt}		0 to 70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
High Level Input Voltage	V_{IH}	2.4		5.5	V	
Low Level Input Voltage	V_{IL}	−1.0		0.8	V	
Ambient Temperature	T_a	0		70	°C	

DC CHARACTERISTICS 1 (Recommended Operating Conditions unless Otherwise Noted)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Leakage Current	I_{IL}	−10	10	μA	V_{IN}=0~5.5 V, Other Input = 0 V
Output Leakage Current	I_{OL}	−10	10	μA	Output is not active. V_{OUT}=0~5.5 V
RAM Port High Level Output Voltage	$V_{OH(R)}$	2.4		V	$I_{OH(R)}$ = −2.0 mA
RAM Port Low Level Output Voltage	$V_{OL(R)}$		0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial Read Port High Level Output Voltage	$V_{OH(S)}$	2.4		V	$I_{OH(S)}$ = −2.0 mA
Serial Read Port Low Level Output Voltage	$V_{OL(S)}$		0.4	V	$I_{OL(S)}$ = 4.2 mA

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{I1}		8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC
	C_{I2}		5	pF	A_0~A_7
	C_{I3}		6	pF	$\overline{SOE}$, $\overline{DT}/\overline{OE}$
Output Capacitance	C_O		7	pF	SO_1~SO_4
Input/Output Capacitance	C_{IO}		7	pF	W_1/IO_1~W_4/IO_4

DC CHARACTERISTICS 2 (Recommended Operating Conditins unless Otherwise Noted)

RAM PORT	SERIAL PORT		SYMBOL	μPD41264C-12	μPD41264C-15	UNIT	NOTE
	Standby*	Active		(MAX.)	(MAX.)		
Random Read, Write Cycle	○		I_{CC1}	95	85	mA	3
$t_{RC}=t_{RC(MIN.)}$, I_O=0 mA		○	I_{CC7}	155	130	mA	3
Standby	○		I_{CC2}	12	12	mA	
$\overline{RAS}=V_{IH}$, D_{out} disable		○	I_{CC8}	60	45	mA	
$\overline{RAS}$ Only Refresh Cycle	○		I_{CC3}	75	65	mA	
$\overline{RAS}$ Cycle, $\overline{CAS}=V_{IH}$, $t_{RC}=t_{RC(MIN.)}$		○	I_{CC9}	135	110	mA	
Page Mode Cycle	○		I_{CC4}	65	55	mA	3
$\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycle, $t_{PC}=t_{PC(MIN.)}$		○	I_{CC10}	125	100	mA	3
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	○		I_{CC5}	75	65	mA	3
$t_{RC}=t_{RC(MIN.)}$		○	I_{CC11}	135	110	mA	3
Data Transfer Cycle	○		I_{CC6}	120	110	mA	
$t_{RC}=t_{RC(MIN.)}$		○	I_{CC12}	180	145	mA	

* SC = V_{IL}

AC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise Noted)[1,2,4]

PARAMETER	SYMBOL	μPD41264C-12		μPD41264C-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}		120		150	ns	5
Access Time from $\overline{CAS}$	t_{CAC}		60		75	ns	6
Access Time from $\overline{OE}$	t_{OEA}		30		40	ns	
Access Time from SC	t_{SCA}		40		60	ns	
Access Time from $\overline{SOE}$	t_{SOA}		35		50	ns	
Output Buffer Turn Off Delay from $\overline{CAS}$	t_{OFF}	0	30	0	40	ns	7
Output Buffer Turn Off Delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	ns	7
Serial Output Buffer Turn Off Delay from $\overline{SOE}$	t_{SOZ}	0	30	0	40	ns	7
Random Read, Write Cycle Time	t_{RC}	220		270		ns	
Read - Write, Read Modify Write Cycle Time	t_{RWC}	300		355		ns	
Page Mode Cycle Time	t_{PC}	120		145		ns	
Transition Time	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns	
$\overline{CAS}$ Precharge Time (Except Page Mode)	t_{CPN}	25		30		ns	
$\overline{CAS}$ Precharge Time (Page Mode Only)	t_{CP}	50		60		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	30	75	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	
Row Address Set Up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		20		ns	
Column Address Set Up Time	t_{ASC}	0		0		ns	
Column Address Hold Time (from $\overline{CAS}$)	t_{CAH}	20		25		ns	
Column Address Hold Time (from $\overline{RAS}$)	t_{AR}	80		100		ns	
Read Command Set Up Time	t_{RCS}	0		0		ns	
Read Command Hold Time (from $\overline{RAS}$)	t_{RRH}	20		20		ns	11
Read Command Hold Time (from $\overline{CAS}$)	t_{RCH}	0		0		ns	11
Write Command Set Up Time	t_{WCS}	0		0		ns	9
Write Command Hold Time (from $\overline{RAS}$)	t_{WCH}	35		45		ns	
Write Command Hold Time (from $\overline{CAS}$)	t_{WCR}	95		120		ns	
Write Command Pulse Width	t_{WP}	35		45		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{RWL}	40		45		ns	9
Write Command to $\overline{RAS}$ Lead Time	t_{CWL}	40		45		ns	9
Data Input Set Up Time	t_{DS}	0		0		ns	10
Data Input Hold Time	t_{DH}	35		45		ns	10
Data Input Hold Time from $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	100		120		ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	160		195		ns	9

PARAMETER	SYMBOL	μPD41264C-12		μPD41264C-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
$\overline{OE}$ to Data Input Delay Time	t_{OED}	35		40		ns	
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	30		40		ns	
$\overline{CAS}$ Set Up Time for CBR Refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time for CBR Refresh	t_{CHR}	25		30		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		ns	
Refresh Period for Each Cell	t_{REF}		4		4	ms	
$\overline{DT}$ Set Up Time for Data Transfer Cycle	t_{DLS}	0		0		ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$ for Data Transfer Cycle	t_{RDH}	100		130		ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$ for Data Transfer Cycle	t_{CDH}	40		55		ns	
SC to $\overline{DT}$ Delay Time	t_{SDD}	10		20		ns	
SC Hold Time from $\overline{DT}$	t_{SDH}	10		20		ns	
$\overline{OE}$ Pulse Width	t_{OE}	30		40		ns	
Serial Read Cycle Time	t_{SCC}	40	50000	60	50000	ns	
SC Pulse Width (SC = V_{IH})	t_{SC}	10		20		ns	
SC Precharge Time (SC = V_{IL})	t_{SCP}	10		20		ns	
Output Data Set Time from $\overline{SOE}$	t_{SOO}	5		5		ns	
Output Data Hold Time	t_{SOH}	10		10		ns	
$\overline{DT}$ Set Up Time	t_{DHS}	0		0		ns	
$\overline{DT}$ Hold Time	t_{DHH}	20		25		ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10		10		ns	
$\overline{DT}$ to $\overline{CAS}$ Delay Time	t_{DTC}	10		10		ns	
Write Per Bit Mode Set Up Time	t_{WBS}	0		0		ns	
Write Per Bit Mode Hold Time	t_{WBH}	20		25		ns	
Write Per Bit Mask Data Set Up Time	t_{WS}	0		0		ns	
Wirte Per Bit Mask Data Hold Tmie	t_{WH}	20		25		ns	
$\overline{SOE}$ Pulse Width	t_{SOE}	15		20		ns	
$\overline{SOE}$ Precharge Time	t_{SOP}	15		20		ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{DTH}	20		25		ns	
$\overline{OE}$ Set Up Time for $\overline{RAS}$ Reset	t_{OES}	10		10		ns	

NOTE

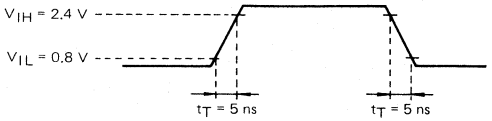
(1) All voltages are referenced to GND (= 0 V).

(2) To initialize internal dynamic circuits, it is necessary to execute dummy cycles inputting eight or more any $\overline{RAS}$ clock cycles after initial pause (Device is not selected) of 100 μs followed Power-ON. (after V_{CC} becomes 4.5 V or more.)

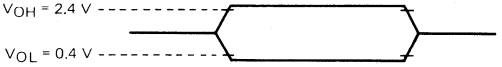
(3) IOi and SOi are measured without load.
Therefore, the values in actual operating conditions depend on the output load and operation cycle time.

(4) AC characteristics test condition

- **Input timing specification**

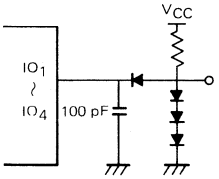


- **Output timing specification**

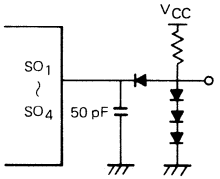


- **Output load**

RAM PORT



SERIAL READ PORT



(5) t_{RAC} is applied when t_{RCD} is smaller than t_{RCD} (MAX). ($t_{RCD} \leqq t_{RCD}$ (MAX)). If t_{RCD} exceeds t_{RCD} (MAX), t_{RAC} increases by the portion in excess of t_{RCD} (MAX), that is, $t_{RCD} - t_{RCD}$ (MAX).

(6) This value is applied when t_{RCD} is greater than t_{RCD} (MAX). ($t_{RCD} > t_{RCD}$ (MAX).)

(7) These specifications are defined as the time until the output is placed in an open circuit state and the output voltage level becomes unmeasurable.

(8) t_{RCD} doesn't define the limit operation but the maximum value that guarantees t_{RAC} (MAX.).

(9) t_{WCS}, t_{CWD} and t_{RWD} specify EARLY WRITE, READ/WRITE, and READ MODIFY WRITE cycles, respectively.
If $t_{WCS} > t_{WCS}$ (MIN.), the EARLY WRITE cycle is performed and data output is placed in a high impedance state during the cycle.
If $t_{CWD} > t_{CWD}$ (MIN.) and $t_{RWD} > t_{RWD}$ (MIN.), the READ MODIFY WRITE cycle is performed and data from the memory cells is output from I/O pins. If none of these conditions is met, the status of I/O Pins is undecided.

(10) In the EARLY WRITE cycle, write timing is defined from the falling edge of $\overline{CAS}$. In the READ-WRITE/READ-MODIFY-WRITE cycle, it is defined from the falling edge of $\overline{WB}/\overline{WE}$.

(11) In the READ cycle, either t_{RRH} or t_{RCH} has to be satisfied.

(12) All DC and AC Characteristics are valid for processcode "X" only. For processcodes "E", "K", and "P" other data are valid.

1. Basic operations of μPD41264C

(1) Structure of μPD41264C

As shown in the block diagram, the μPD41264C is a dual port RAM with a standard 256 K bit (64 K words x 4 bits) dynamic RAM, a 1024 bit (256 words x 4 bits) data register and a serial selector that permits high speed serial read operation. In addition to standard function read, write and refresh as a conventional 64 K words x 4 bits dynamic RAM (μPD41464C), the RAM port features a data transfer cycle that transfers data from the 1024 bit memory cells to the data register on the word line selected by a Tow address. Besides 4 bit input/output organizations, write per bit capability is added to execute the write cycle for selected bit of the 4 bit input data and relizes high efficient bit by bit data rewriting in image processing, etc.
For these two additional functions, the data transfer cycle is assigned to $\overline{OE}$ and the write per bit cycle is assigned to $\overline{WE}$ and $IO_1 \sim IO_4$ so as not to increase the number of pins.

(2) Input/Output terminal functions

The μPD41264C has input terminals $\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, SC, $\overline{SOE}$, and $A_0 \sim A_7$, and input/output terminals $W_1/IO_1 \sim W_4/IO_4$ and output terminals $SO_1 \sim SO_4$.

- $\overline{RAS}$ ..... (Row Address Strobe) $\overline{CAS}$ (Column Address Strobe)

  μPD41264C has two chip activation clocks, $\overline{RAS}$ and $\overline{CAS}$. The $\overline{RAS}$ clock takes ROW addresses (A_0 to A_7), selects a word line corresponding to input address and activates the sense amplifier (Read/Write operation). It refreshes 1024 bit memory cells on one line selected by the Row address (A_0 to A_7). The $\overline{RAS}$ clock also serves as a clock to select the operation of write per bit cycle, real time data transfer cycle, and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{CAS}$ clock takes Column addresses (A_0 to A_7) and output the memory cell data amplified by the sense amplifier from the RAM port ($IO_1 \sim IO_4$).

- $A_0 - A_7$ ..... (Address input)

  A 16 bit address has to be input to select one word (4 bit data) memory cell from the memory cell array of 65536 words x 4 bits. The μPD41264C uses the address multiplex method to divide a 16 bit address into lower 8 bits (Row address) and upper 8 bits (Column address). The Row and Column addresses are placed in the memory on the falling edges of the $\overline{RAS}$ and $\overline{CAS}$ clocks, respectively. For this reason, the address input set up (t_{ASR}, t_{ASC}) and hold (t_{RAH}, t_{CAH}) times are specified for the falling edges of the $\overline{RAS}$ AND $\overline{CAS}$ clocks. In the operation timing, the $\overline{RAS}$ clock is activated after inputting the Row address and then the $\overline{CAS}$ clock is activated after switching to the Column address. This address input to interval SC counter also serves as the specification of the serial read start address after data transfer cycle.

- $\overline{WB}/\overline{WE}$ ..... (Write per bit/Write enable input)

  The write per bit cycle or 4 bit write cycle is executed by controlling the input level of this $\overline{WB}/\overline{WE}$ clock before activation of the $\overline{RAS}$ and $\overline{CAS}$ clocks. These operations are selected by the level of the $\overline{WB}/\overline{WE}$ clock at the falling edge of the $\overline{RAS}$ clock. That is, the write per bit cycle is selected with the low level and the 4 bit write cycle is selected with the high level.

- $\overline{DT}/\overline{OE}$ ..... (Data transfer/Output enable input)
  The data transfer cycle or read cycle is executed by controlling the input level of this $\overline{DT}/\overline{OE}$ clock before activation of the $\overline{RAS}$ and $\overline{CAS}$ clocks. These operations are selected by the level of the $\overline{DT}/\overline{OE}$ clock at the falling edge of the $\overline{RAS}$ clock. That is, the data transfer cycle is selected with the low level and the read cycle is selected with the high level.

- $W_1/IO_1 \sim W_4/IO_4$ ..... (Write per bit selection data input/data input output)
  These terminals are write per bit selection data inputs and data inputs/outputs. The write per bit cycle is enabled when $W_1/IO_1 \sim W_4/IO_4$ are in the high level at the falling edge of the $\overline{RAS}$ clock. In this cycle, the write operation is executed only for the selected bit. In the write cycle, data is placed in memory on the falling edge of the $\overline{CAS}$ or $\overline{WE}$ clock, whichever is input (activated) slower.

- SC ..... (Serial control clock)
  Serial read port control clock. The serial access operation starts from the rising edge by inputting the SC clock. The output data is maintained until the rising edge of next SC clock.

- $SO_1 \sim SO_4$ ..... (Serial read output)
  These are output terminals for data of 256 words x 4 bits accessed by SC clock.

- $\overline{SOE}$ ..... (Serial output enable)
  Serial read port output control clock input. Data output is executed by making the $\overline{SOE}$ input active.

2. Operations of μPD41264C

(1) μPD41264C read/write operations

(a) RAM port operations

- Random read cycle

  The RAM port of the μPD41264C is the 4 bit I/O common type. In the read cycle, an address is specified by the $\overline{RAS}$ and $\overline{CAS}$ clocks and then the read data is output by activating the $\overline{DT}/\overline{OE}$ clock. Since the read and data transfer cycle operations are decided by the level of the $\overline{DT}/\overline{OE}$ clock at the falling edge of the RAS clock, it is necessary for the $\overline{DT}/\overline{OE}$ clock to maintain the high level for more than t_{DDH} (MIN.) from the falling edge of the $\overline{RAS}$ clock and then to be set in the low level.

- Random write cycle . . . . . early write, late write, read modify write.

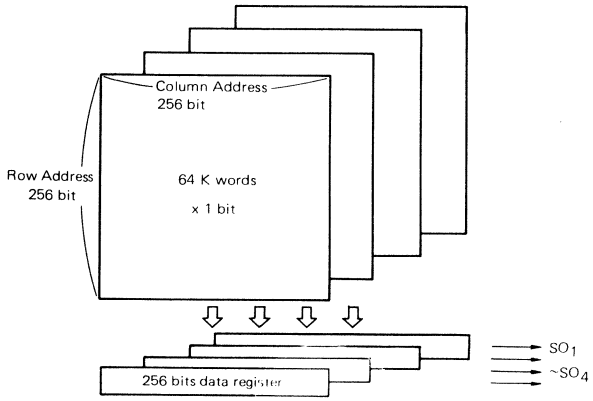
  This cycle is executed by activating the $\overline{RAS}$ and $\overline{CAS}$ clock and by activating the $\overline{WE}$ clock. At this time, since the $\overline{WB}/\overline{WE}$ clock also serves as the bit selection data input, they should be set in the high level at the falling edge of the $\overline{RAS}$ clock when executing ordinary 4 bit write.

  The early write is specified when the $\overline{WE}$ clock is input earlier than the $\overline{CAS}$ clock. The write data is taken into the chip from the falling edge of the $\overline{CAS}$ clock.

  The late write cycle is specified when the $\overline{WE}$ clock is input later than the $\overline{CAS}$ clock. The write data is taken into the chip from the falling edge of the $\overline{WE}$ clock. (At this time, it is necessary to maintain the $\overline{OE}$ clock at a high level until after the input of $\overline{WE}$ clock to ensure the status of read data output.) By delaying the $\overline{WE}$ clock more than t_{RWD}/t_{CWD} from the $\overline{RAS}$, $\overline{CAS}$ clock, it is possible to execute the read modify write cycle in which for one the $\overline{RAS}$ and $\overline{CAS}$ cycle the data read out once can be modified and then written to the same address. During the execution of this cycle, it is necessary to control data output by the $\overline{OE}$ clock to prevent data output and input from clashing on the data bus.

- Write per bit mode

  The μPD41264 has a write per bit capability that permits writing data only in the required I/O of IO_1 through IO_4 to maximize its effect as a video RAM. This write per bit function can be executed in every write cycle and is enabled by setting the $\overline{WB}/\overline{WE}$ clock input in the low level at the falling edge of the $\overline{RAS}$ clock. The bit written in this cycle is decided by the input voltage level of $W_1/IO_1 \sim W_4/IO_4$ at the falling edge of $\overline{RAS}$ clock like the $\overline{WB}/\overline{WE}$ clock.



The Row address selects one Row to be transferred of 256 Rows and the Column address specifies the address of the serial port ($SO_1 - SO_4$) from which serial access is to be performed (pointer control function). For a display system to display 256 bits x 256 bits (x 4 planes), for example, Row addresses correspond to individual horizontal lines and column addresses to the bits (pixels) on each horizontal line. During data transfer cycles, Row addresses are always incremented, and 0 can be input for column addresses. Actually, display screens of various sizes are used and executing a data transfer cycle during display operation (except blanking time) is often necessary.

(b) Serial read port operation

The following explains serial read port operations characteristing the μPD41264C.

As shown in the block diagram, a 256 bit data register is provided for each of the 4 bit blocks (64 K words x 4 bits..... 4 I/O_S). In each data transfer cycle, 256 bit data on the same Row in each 64 K bit memory cell block is transferred to each data register. Since this data register performs only serial read operations through a combination of an 8 bit address counter and a serial data selector, it enables a very high speed (25 MHz MAX.) read cycle.

- Data transfer cycle

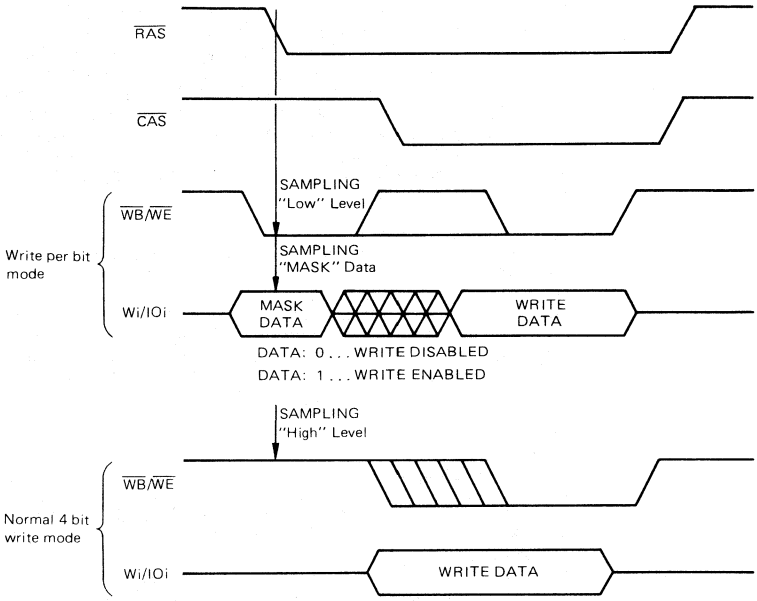
The data transfer cycle is executed by setting the $\overline{DT}/\overline{OE}$ clock in the low level at the falling edge of the $\overline{RAS}$ clock by specifying the address of the required data in the memory cell array by the $\overline{RAS}$ and $\overline{CAS}$ clocks, and by making the rise of the $\overline{DT}/\overline{OE}$ clock and the $\overline{RAS}$ and $\overline{CAS}$ clocks synchronous. At this time, the Row address, Column address, memory cell and data register are related as follows.

When the $\overline{WB}/\overline{WE}$ clock becomes active at the input of the $\overline{RAS}$ clock and write operation is performed for IO_1 to IO_4, it is necessary to set all bit selection data in the high level. The write per bit mode is effective for every write cycle. However, in the page mode write cycle, the bit selection data is decided by the first $\overline{RAS}$ and $\overline{CAS}$ cycle and then becomes active. For this reason, changing the bit selection data during the page mode is impossible without the falling edge of the $\overline{RAS}$ clock. (In page mode, $\overline{RAS}$ clock must be maintained Low level and only changing of the $\overline{CAS}$ clock is repeated in Long $\overline{RAS}$ (active Low) cycle.)

- Page mode cycle

The page mode cycle is the mode that permits accessing memory cells of the same row address at about half of the cycle time required for the random read/write cycle. The page mode cycle is executed by repeating the $\overline{CAS}$ clock cycle twice or more than when the $\overline{RAS}$ clock is activated. Either the read/write or read modify write operation is available in this cycle.

In one long $\overline{RAS}$ cycle, the number of $\overline{CAS}$ clock cycles (page mode cycles) must be set such that access of 256 word (x 4 bits) memory cells of the same Row address does not exceed t_{RAS} (MAX.) = 10 μs.

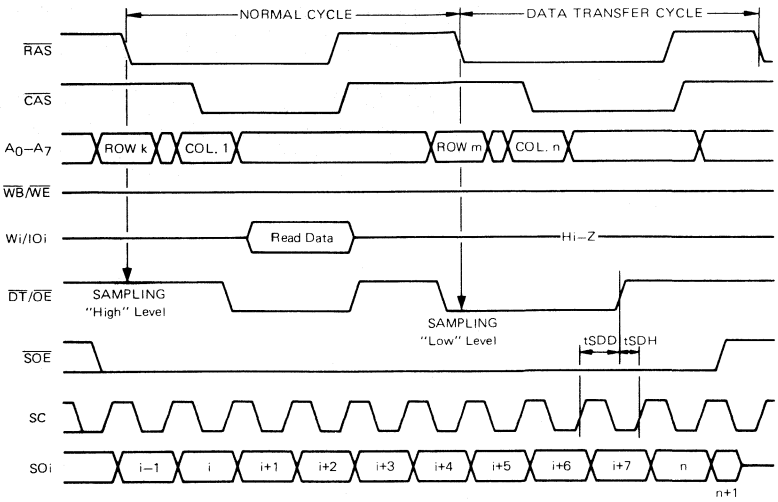


IO	Bit Selection Data		Write Operation
IO_1	1	(High)	Data input
	0	(Low)	Disable (High impedance)
IO_2	1	(High)	Data input
	0	(Low)	Disable (High impedance)
IO_3	1	(High)	Data input
	0	(Low)	Disable (High impedance)
IO_4	1	(High)	Data input
	0	(Low)	Disable (High impedance)

Real Time Data Transfer Capability

The μPD41264C has real time data transfer capability, allowing the data transfer cycle to be executed even when the serial read port is active, that is, during display processing. Real time data transfer can be performed by making the serial read port Standby (SC clock is Low) and by synchronizing the SC clock with the rise of the DT/OE clock. The new data transferred to the data register in the serial read cycle after the rise of the DT/OE clock is accessed.

Timing Chart of Real Time Data Transfer Cycle



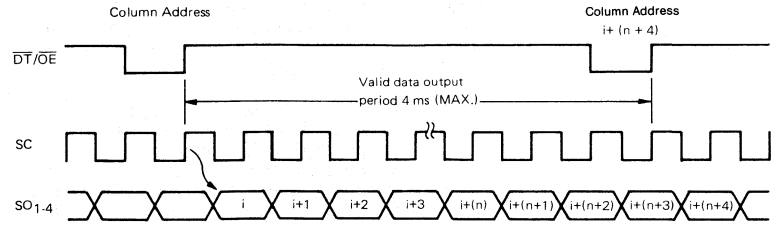
- Serial read cycle

  The 256 word x 4 bits of data stored in the data register in a data transfer cycle can be read out at a very high speed (40 ns with the μPD41264C-12; 60 ns with the μPD41264C-15) cycle by making the SC clock and $\overline{SOE}$ input active. In the case of dual port RAM, the serial read port and the RAM port that accesses a memory cell of 64 K words x 4 bits can be operated asynchronously except the data transfer cycle. This enables a system to be built with a very high CPU access efficiency.

  The access operation (data output) of the serial read port starts from the rise of the SC clock by simply inputting the SC clock when the $\overline{SOE}$ is in the low level, data output is then maintained until the rise of the next SC clock. (The Serial address is counted up with the SC clock only.) This provides a wide allowance for external data latching timing with an expanded timing margin available for system design.

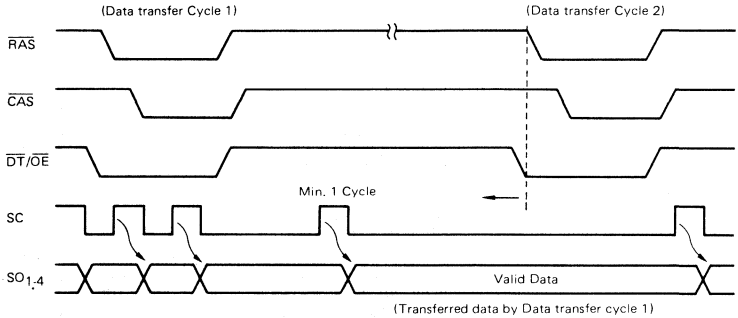
  The address specified by the column address at data transfer explained above becomes the starting address of the serial read cycle. If a 256 cycle SC clock is input, it becomes identical with the starting address by inputting next SC clock and if another SC clock is entered, serial address counting is made sequentially. (Serial address count up by SC clock input is independent of the input of $\overline{SOE}$.)

  The data in the data register of 256 words x 4 bits, as for the memory cell array can be maintained by the dynamic peripheral circuit. When reading out the data loaded in the data register using SC clocks, the output, as effective data, is 4 ms independent of the operation of SC clocks. If the execution of serial read cycles exceeds 4 ms, the execution of the data transfer cycle is necessary again.



To read the data transferred to the data register in data transfer cycles as effective data, it is necessary to input at least one SC clock before starting the next data transfer cycle (before the fall of the $\overline{RAS}$ clock).

If the data transferred in data transfer cycle 1 is not used as effective data, there is no restriction on the input of SC clock. Even if no SC clock is input, the next data transfer cycle is uneffected. (However, for the reduction of power consumption in the system, SC clock must be maintained low level except the interval of SC serial access for pixel data out.)



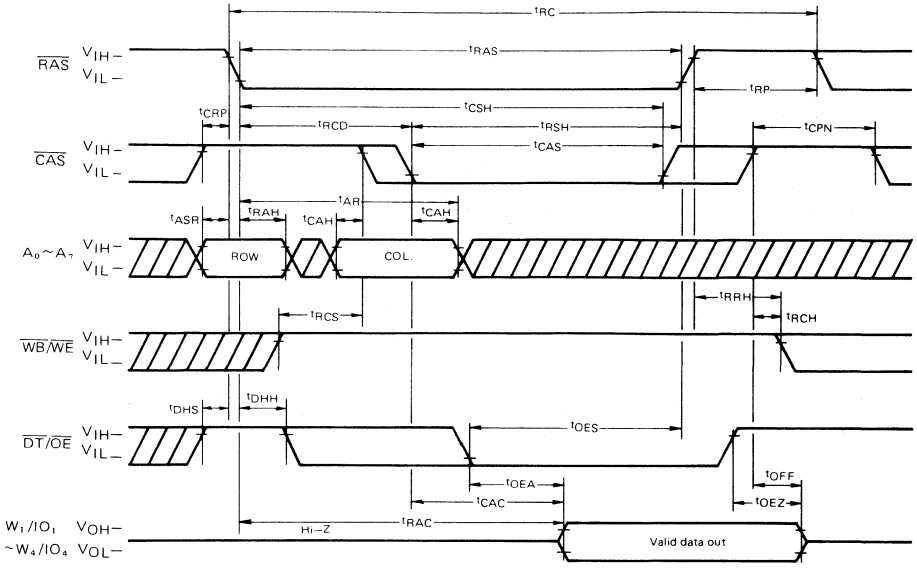
(2) Memory refresh cycle

The μPD41264C refresh processing includes $\overline{CAS}$ before $\overline{RAS}$ refresh and refresh by external address input ($\overline{RAS}$ only refresh, and read/write refresh). The refresh time is 256 cycle within 4 ms and is the standard specification for 256 K DRAM.

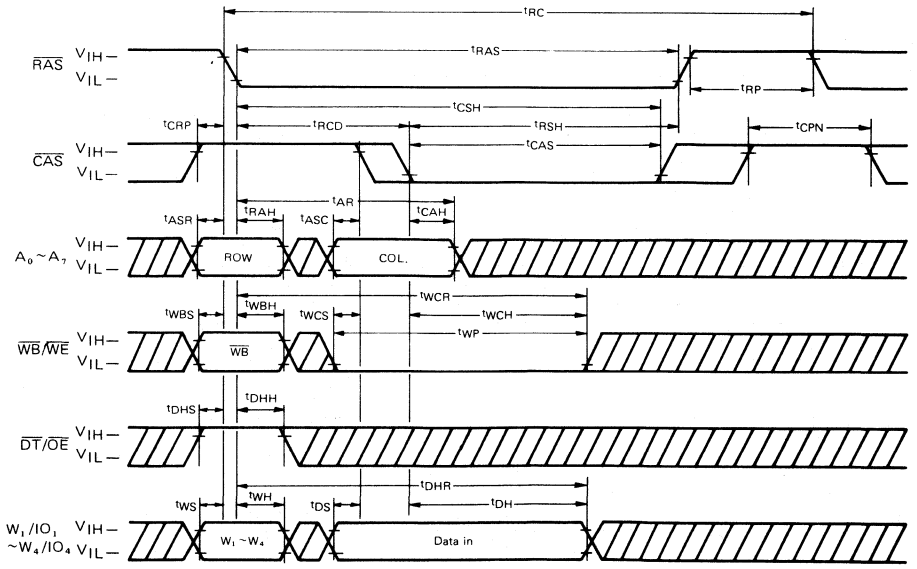
- Refresh by external address ($\overline{RAS}$ only refresh, and read/write refresh)
  This can be executed by specifying a Row address of lower bits A_0 to A_7 and by activating the $\overline{RAS}$ clock. Refresh operation amplifies the 1024 bit memory cell (262144 bits/256 cycles = 1024 bits/cycle) data specified by the Row address of the lower 8 bits by the sence amplifier and rewrites it in the memory cell. This requires that all Rows are accessed by the lower 8 bits within 4 ms. For a system in which memory addresses are always incremented, refreshing may not be required.
  When using $\overline{RAS}$ only refreshing, if there are two or more devices on the same bus (output terminals are connected wired OR), the above read/write operations causes data to clash on the data bus unless a buffer is provided for each device. To prevent this, it is necessary to set the I/O line in a high impedance state for refreshing.

- $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (including hidden refresh)
  Refreshing by the output of the built-in 8 bit refresh address counter is possible by activating the $\overline{CAS}$ clock before $\overline{RAS}$ clock, that is, by executing the $\overline{RAS}$ and $\overline{CAS}$ clock cycle that are reverse to the ordinary clock cycles. It is also possible to execute hidden refreshing, that is, refreshing while outputting data by keeping the $\overline{CAS}$ and $\overline{OE}$ clocks from the previous cycle.

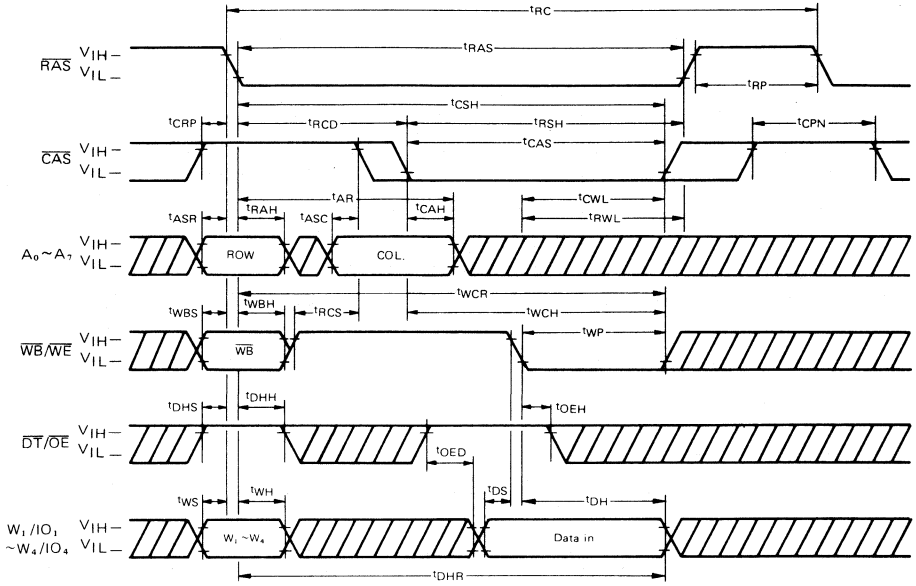
READ CYCLE



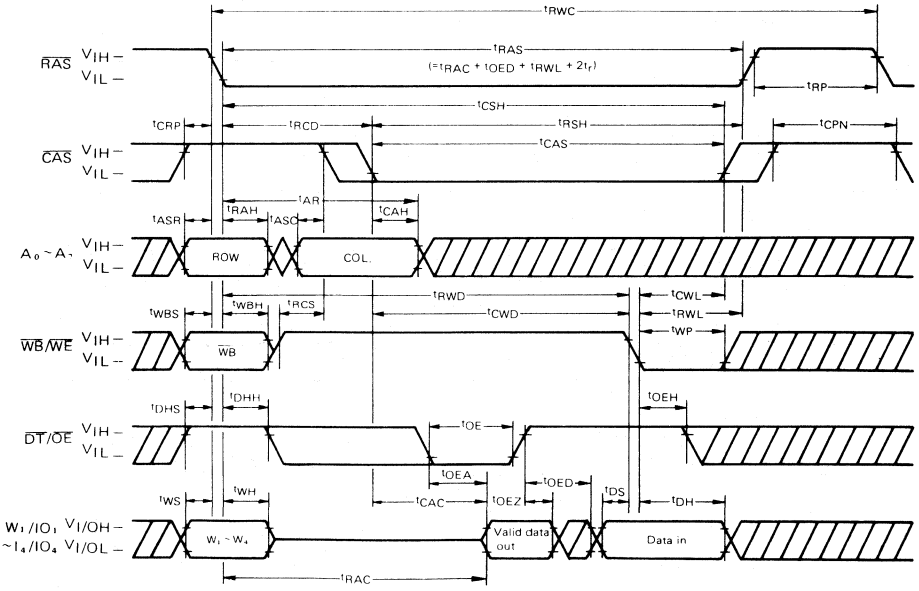
EARLY WRITE CYCLE



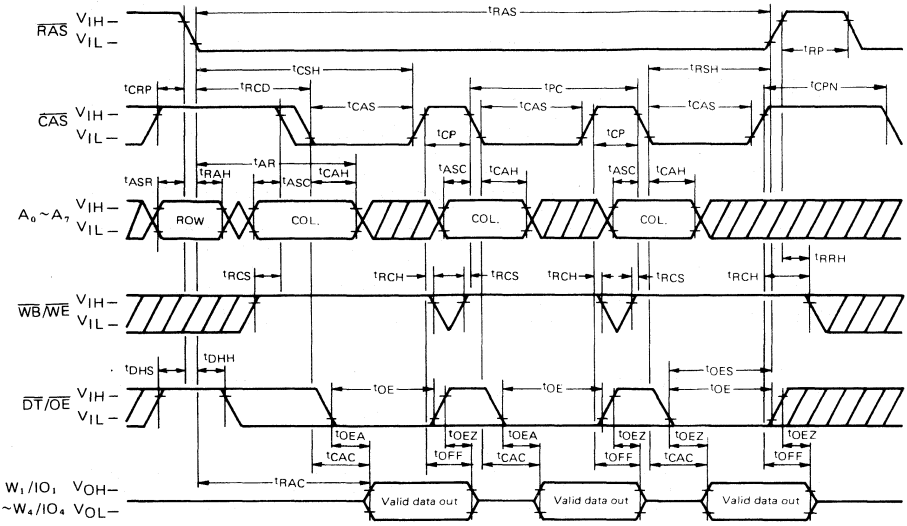
LATE WRITE CYCLE



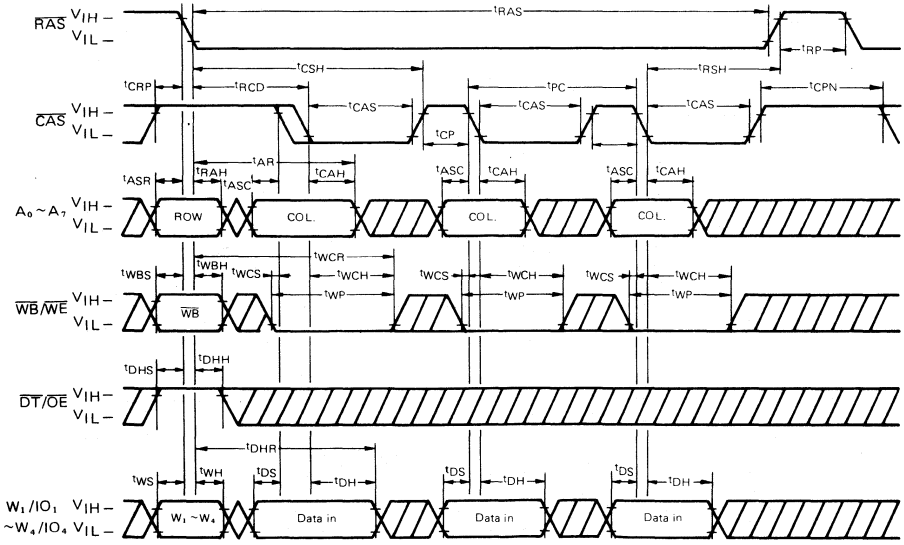
READ MODIFY WRITE CYCLE



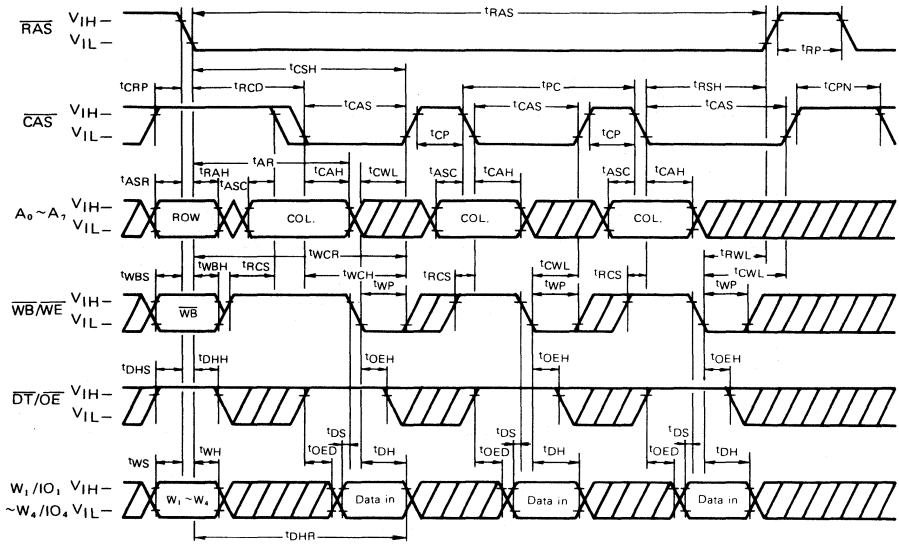
PAGE MODE READ CYCLE



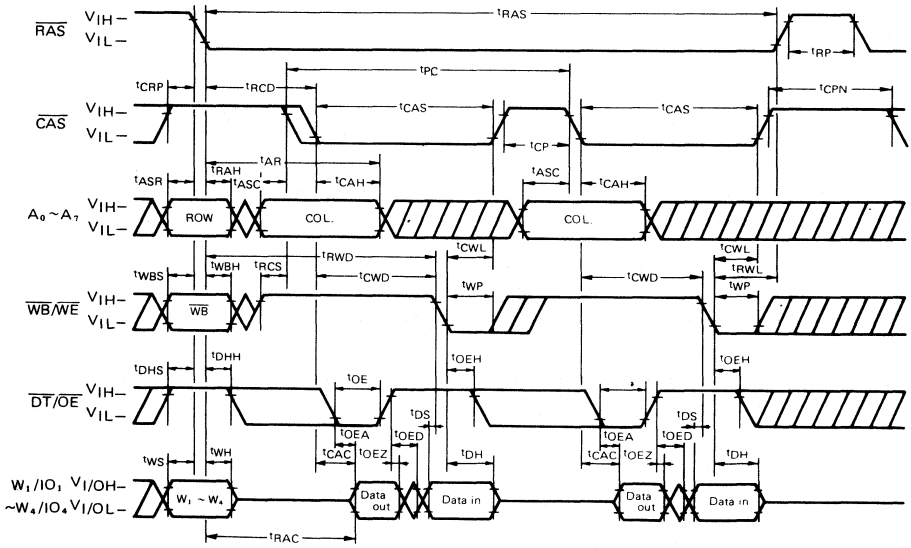
PAGE MODE EARLY WRITE CYCLE



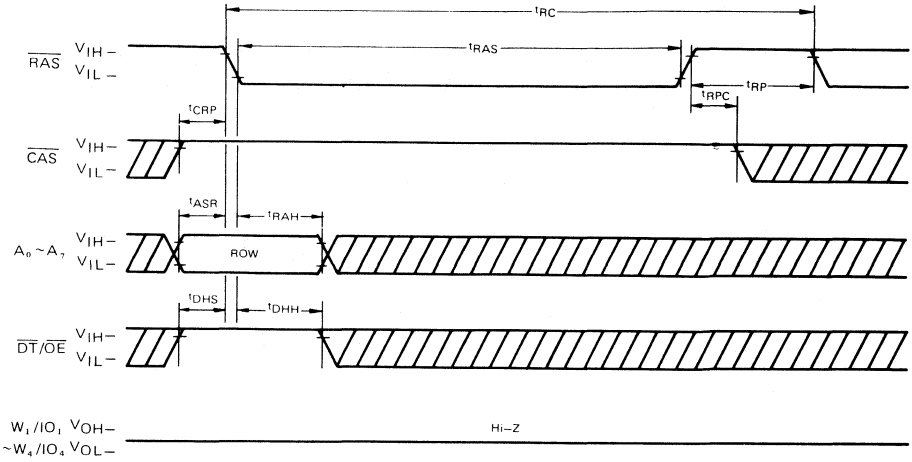
PAGE MODE LATE WRITE CYCLE



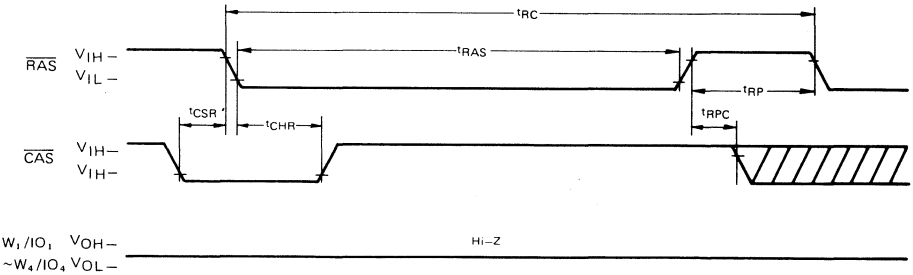
PAGE MODE READ MODIFY WRITE CYCLE



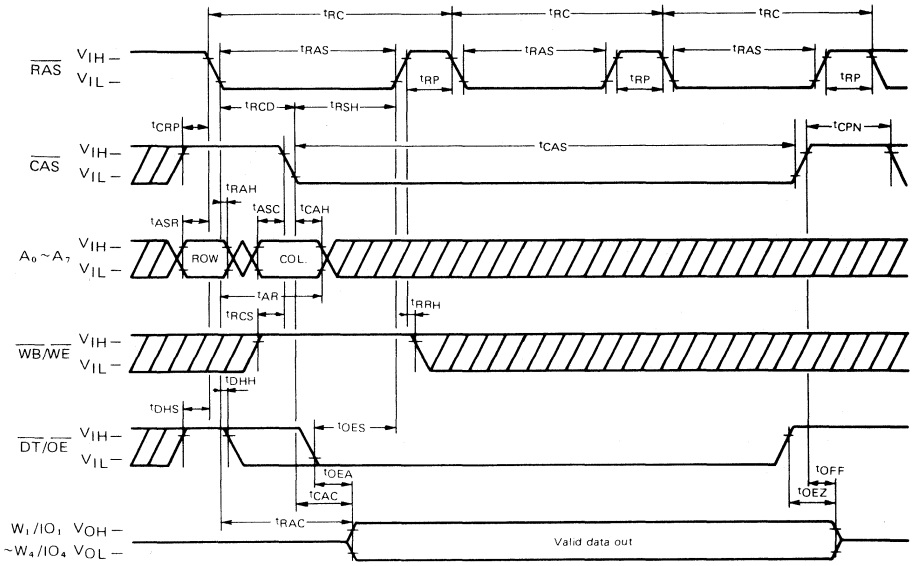
$\overline{RAS}$ ONLY REFRESH CYCLE



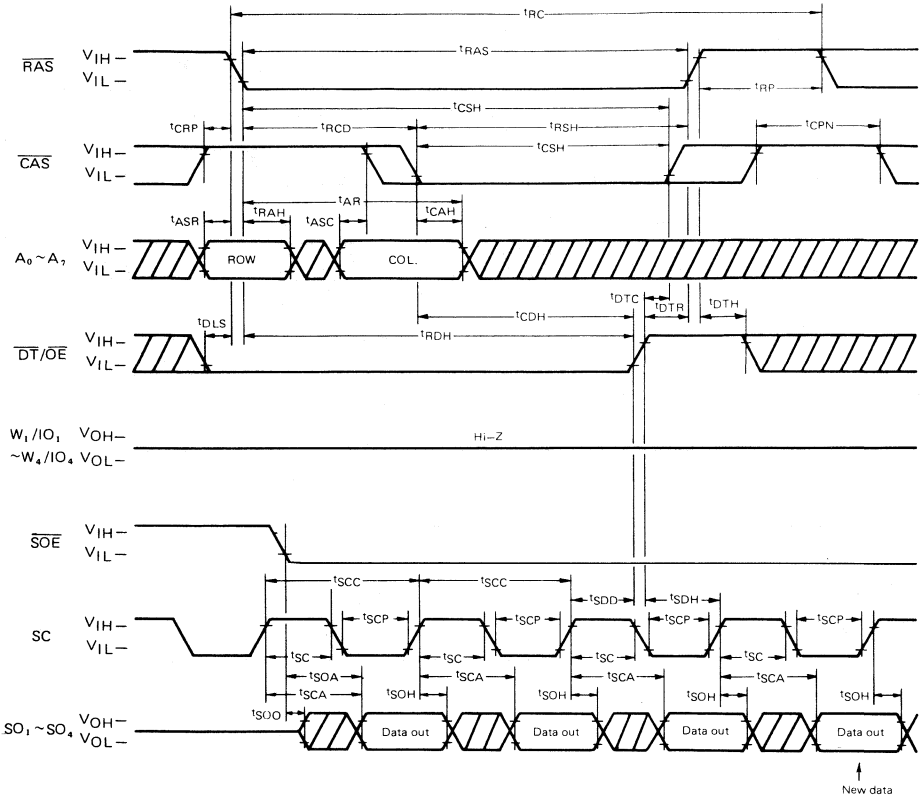
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



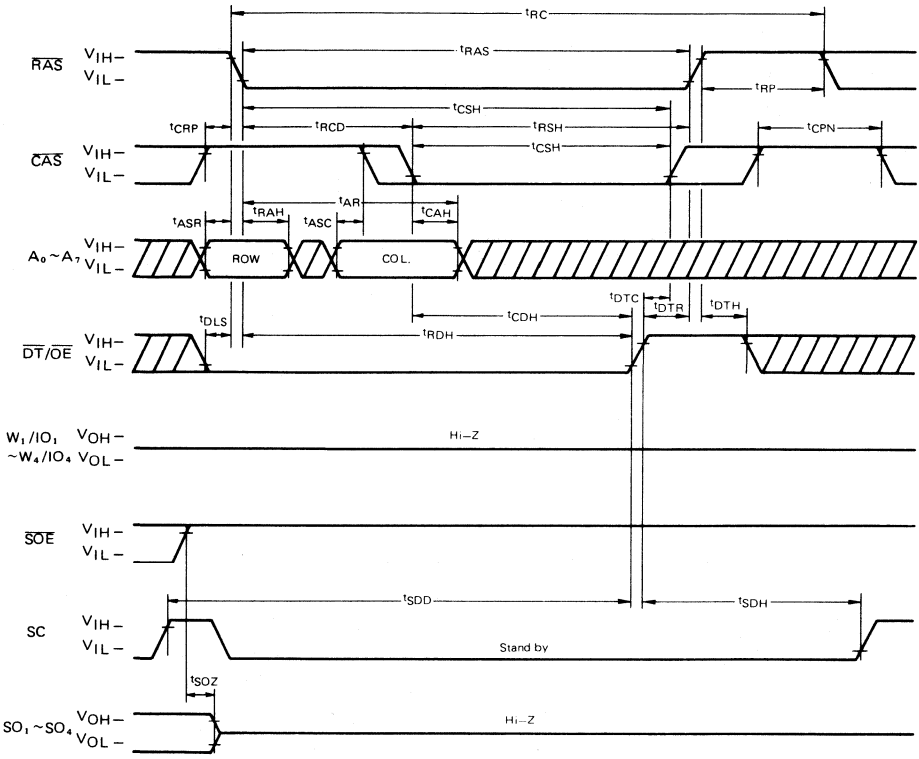
HIDDEN REFRESH BY $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



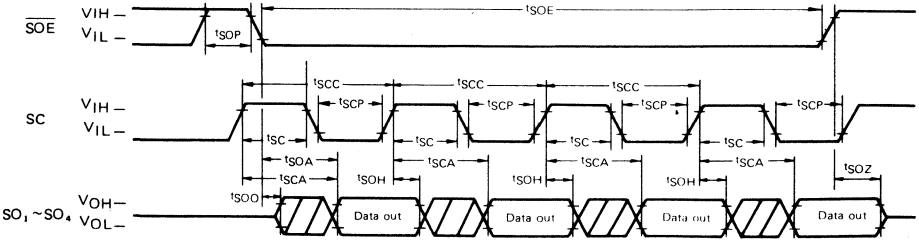
DATA TRANSFER CYCLE (SERIAL READ PORT ACTIVE)



DATA TRANSFER CYCLE (SERIAL READ PORT STANDBY)



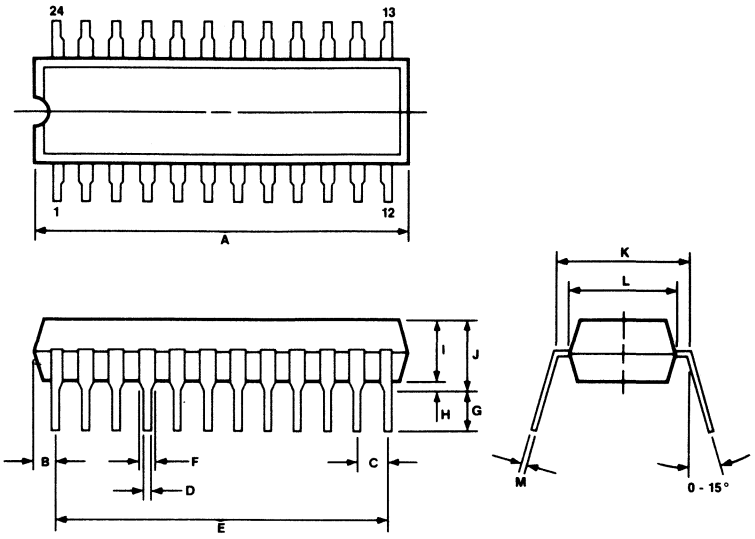
SERIAL READ CYCLE



PACKAGE DIMENSIONS

24-PIN Plastic DIP

Item	Millimeters
A	30.48 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.2 ± 0.3
H	.51 min
I	4.31 max
J	5.08 max
K	10.16 [TP]
L	8.6
M	$.25^{+.10}_{-.05}$



Introduction

This article introduces a new 320-row x 700-bit-field memory device. Originally designed for the television market, this device will find its way into many applications which require storing data in a raster format. NMOS DRAM technology, a 14-pin plastic DIP package and a unique row-pointer addressing scheme offer a low-cost device for smaller system size. The array size can be customized to meet customer applications. See figure 1.

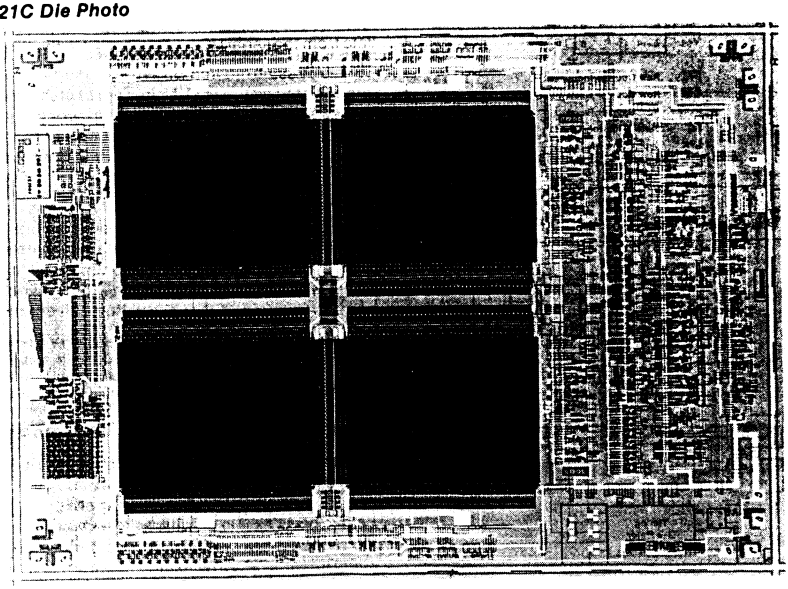
The television business is driven by picture quality, which is an important attribute in the consumer decisionmaking process. High-definition television (HDTV) is usually direct broadcast transmission of 1125 line resolution. Higher picture quality can also be achieved by using the current NTSC/PAL standard and improving the image at the receiver end. It is for this market that the μPD41221 has immediate application. Because VCRs, CATV, video processing and special effects equipment use similar components, the μPD41221 finds many applications in this family of products.

In the associated industry of teletext, system price keeps terminals out of the average consumer's home.

This article shows how the frame buffer memory can reduce component cost and simplify system design. The inevitable success of this product could allow an inexpensive terminal (using tv as the monitor) to be given to the subscriber for only a monthly service charge.

The personal computer business is maturing and stablizing and two or three companies are becoming the de facto standards. With standardization comes opportunities to develop add-on PC products. Playing a dominant role in this market are the image grabber and video digital signal processing option packages. The μPD41221 finds many and varied applications in this business segment. Before studying various applications, let us look at the device architecture and operation.

Figure 1. μPD41221C Die Photo



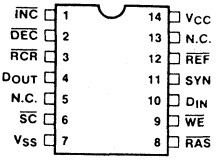
Device Definition

NEC has produced a field memory to fit most tv specifications (see table 1). This device is manufactured at low cost using 256K DRAM NMOS technology. Produced on the same lines as the 256K DRAM, the storage cells are similar, while peripheral circuits differ from those of the standard DRAM.

The device is line-addressable with the three signals $\overline{INC}/\overline{DEC}/\overline{RCR}$, and therefore allows packaging in a 14-pin dual in-line package. See figure 2.

This serial memory operates by sequential readout of each bit (column) in a row. Rows correspond to scan lines on the tv screen. The correspondence between bits in the memory and points on the screen is achieved by analog-to-digital conversion of the composite video signal which has been sampled at three times the frequency of the subcarrier signal. Seven outputs of the A/D converter are then stored in the serial memory. As seen in table 1, the μPD41221 can meet most tv standards and, by minor photomask modifications, can be customized to any size.

Figure 2. 41221 Pinout



$\overline{INC}$	Row Counter Increment
$\overline{DEC}$	Row Counter Decrement
$\overline{RCR}$	Row Counter Reset
$\overline{SC}$	Serial Control
SYN	Sync Acknowledge
$\overline{REF}$	Refresh Control

Table 1. Field Memory Specification for TV Standards

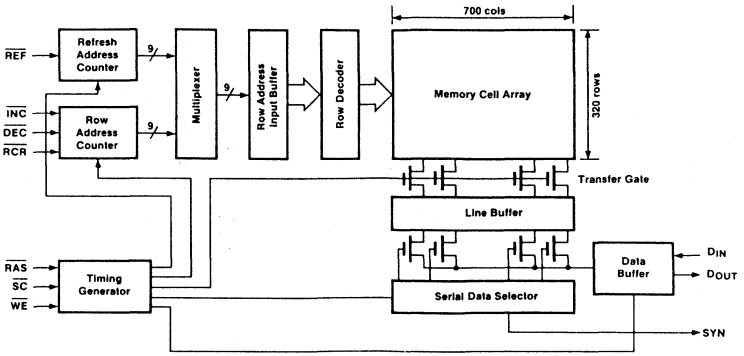
TV Standard	Sampling Rate	Memory Size	Rate
NTSC	$4f_{SC}$	263 x 910	69 ns
	$3f_{SC}$	263 x 682	93 ns
	$2.5f_{SC}$	263 x 569	112 ns
PAL	$4f_{SC}$	313 x 1135	56 ns
	$3f_{SC}$	313 x 851	75 ns
	$2.5f_{SC}$	313 x 709	90 ns

Internal Device Description

Organization

The memory array is similar to a standard DRAM containing a balanced bit line, 1/2C dummy cell and sense amplifier. A single-transistor transfer gate allows the level on the bit-line pairs to flow through and be latched in the line buffer (see figures 3 and 4). A fourphase dynamic shift register provides the appropriately timed column decode to cause a transfer from the line buffer to the serial data bus (read operation). The write operation is simply a reverse of the read, taking the data from the serial I/O and latching it in the line buffer.

Figure 3. Block Diagram



Unique Serial Read and Write Function

An initial pause of 2 ms is required after power up. After this pause it is recommended that 8 cycles of $\overline{REF}$,$\overline{INC}$,$\overline{DEC}$,$\overline{RCR}$, and $\overline{RAS}$ be performed. The total number of dummy cycles required is 40 cycles.

$8 \times (\overline{RAS} + \overline{REF} + \overline{INC} + \overline{DEC} + \overline{RCR}) = 40$ cycles

This requirement is invisible to the CRT user since a few seconds are required for the CRT to heat up.

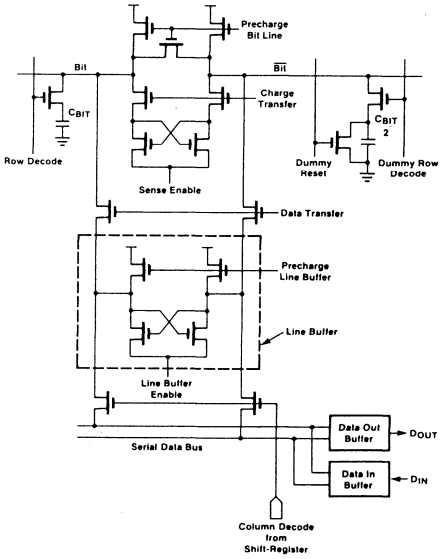
The timing consistent with CRT operation is broken down into two time zones: (1) display time and (2) horizontal retrace time. See figure 6. Row selection can occur at any time but the row-selection pulse must be completed 100 ns before the data-transfer cycle. The negative transition of $\overline{RAS}$ starts a chain of internal clocks which precharge the bit lines, enable the sense amplifiers and turn on the transfer gates allowing the data to flow through and be latched in the line buffer (figure 4). A minimum of 710 ns is required to complete the data transfer operation, which occurs during the horizontal retrace time.

200 ns after $\overline{RAS}$ goes high, the serial clock can become active, beginning the serial-write, serial-read cycle for the display time. Refer to figure 5 for the following discussion of the line buffer and shift register. Data has been latched in the line buffer, which is actually two 176 column buffers (column 0-351) and two 174 column buffers (columns 352-699). Each line buffer pair has a shift register which provides the column decode enable, transferring data to the serial I/O pair. The I/O pairs are connected to four differential input selectors. I/O_0 and I/O_1 are tied to a serial bus which is driven from either the read selector or write selector. I/O_2 and I/O_3 are tied to a second set of read and write selectors.

During a read ($\overline{WE}$ high), one enabled read selector receives and amplifies the differential signal and inputs it to the data-out buffer. $\overline{WE}$ going low initiates a write operation by enabling the appropriate write and read selector driving the serial bus and resetting the decoded flip-flop in the line buffer.

Note: During a write operation the read selector is also active so that data also appears at data out, delayed by one serial access. The alternating reads and writes within the same operation is an unique feature not found in other DRAMs.

Figure 4. Basic Schematics of Sense-Amp. and Line Buffer



Data Restore

After 700 $\overline{SC}$ serial clock cycles, the output does not wrap around but switches unconditionally to a high state following the next $\overline{SC}$ low transition and remains high for any number of additional clocks (read cycle). For a write cycle the output follows the input. At the completion of the serial read or write, an internal clock signal, RAS1, has been active from the beginning of the data-transfer cycle throughout the serial read/write cycle. Due to leakage, the level of this signal begins to decay and may affect stored data. For this reason it is recommended that a data-restore cycle be performed after each period of serial read/write operation. Of course, the data-transfer operation performs a full refresh. It is the relatively long time period of maintaining RAS1 for the full scan line which creates the need for the data-restore cycle.

The data-restore cycle is achieved by bringing $\overline{WE}$ and then $\overline{RAS}$ low 200 ns after the last $\overline{SC}$ and $\overline{REF}$ clock. Data restore precharges the bit line and enables the sense amplifier, thus restoring all 700 cells for the previously selected row.

Refresh

The $\overline{REF}$ operation is executed by an on-chip refresh counter which is incremented by each refresh cycle. Nine address bits from the counter are multiplexed and sent to the row-address buffer and decoder which enables the selected row. The row selection process also generates internal row clock signals, and the full refresh functions occurs.

In an interlaced or non-interlaced CRT application, all 320 scan lines are read and restored every 16.6 or 33.3 milliseconds (one frame time). Obviously, this violates the 320 cycle/2 ms requirements. The $\overline{REF}$ input (pin 12) provides a method of supplying approximately 90 refresh pulses per scan line (refresh cycle = 710 ns) thus easily providing the 320 cycles within 4 scan lines.

Figure 5. Basic Schematics of Shift Register

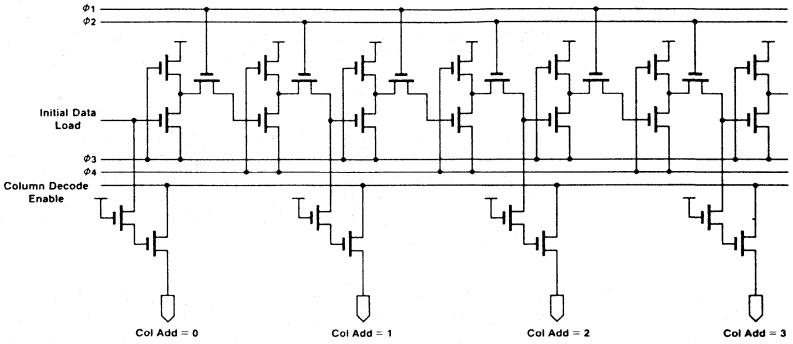
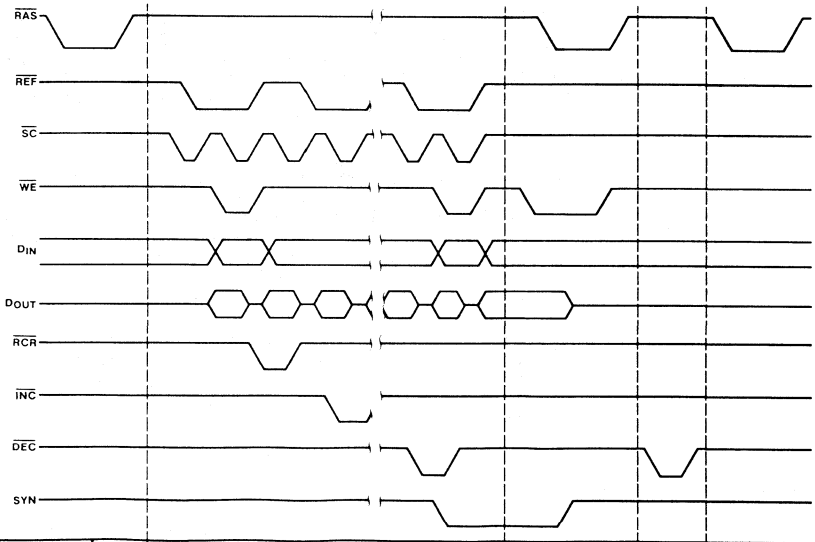


Figure 6. μPD41221 Timing Diagram



Data Transfer	0				0
Data Restore			0		
REF Refresh		0		0	
Serial Write		0			
Serial Read		0			
R.C. Reset		0	0	0	
R.C. Increment		0	0	0	
R.C. Decrement		0	0	0	

Note:

[1] In this table a "0" indicates that the operation is available using the timing shown above.

One refresh scheme is simply to use a convenient clock (200 kHz to 1 MHz) from the system time-base generator. Gating this clock on and off with horizontal synchronous pulse would ensure a $\overline{REF}$ refresh during the serial read/write time. Pin 12 refresh can be performed during, and asynchronously with, the serial read/write operation. Refresh can also be performed during horizontal retrace but not during a data-restore cycle or during a data-transfer operation.

Row Address Selection
The $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$ signals modify the row-address counter. After incrementing, decrementing, or resetting the counter, the multiplexer inputs the 9 bits to the row-address buffer and decoder. This row selection can be initiated during the horizontal retrace or during video time, as shown in figure 6. The previous row address remains valid through any further video time and a data-restore cycle. The new row-decode and sense-amp operation does not begin until the falling edge of $\overline{RAS}$ begins the DT cycle.

Some Application Examples

Improved Picture Quality Through Progressive Scan Technique
The NTSC 1/30-of-a-second 525-line picture frame is broken down into 262 1/2-line fields displayed in 1/60 of a second. This approach uses the current transmitted bandwidth but requires twice the scan rate in the television system. Today large tvs have spacing between lines and the visible line structure degrades picture resolution. The introduction of digital frame stores now makes possible the sequential or progressive scan technique.

With this technique the first or odd field is stored in the μPD41221. After scan conversion to double the line rate, each line of the even field is displayed. The stored odd field is read out of serial memory at double the normal line rate and is time-sequenced after each even line (see figure 7). All 525 lines are scanned in sequence rather than interlaced. Line flicker is thus eliminated and there is a perceived increase in vertical resolution.

Sequential Scan Television
The system in figure 8 is representative of how the sequential scan technique might be implemented for the 25-inch home tv market. A dynamic comb filter separates the luminescence (Y) from the color or chroma signal (I & Q). An A/D conversion is performed on each component at three times the bandwidth of each sampled signal. A field separator discriminates the odd and even fields. The odd lines are stored in two banks of seven μPD41221 chips. The even lines can be displayed in real time, delayed by one horizontal time and scanned at twice the normal rate.

As mentioned before, all 525 lines are displayed in 16.67 ms, which results in 32 μs per line. Displaying 700 samples in 32 μs requires an access time of 45 ns per sample necessitating two banks of memory and a memory interlacing scheme shown in figure 7. The chroma I and Q signals can be multiplexed and only one bank of serial memory is required.

Figure 7. Sequential Scan Technique

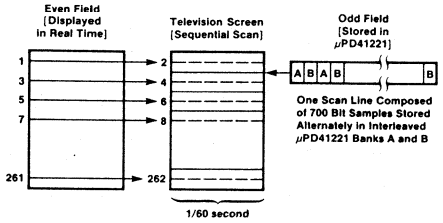


Figure 8. T.V. Employing Sequential Scan Technique with NEC's μPD41221

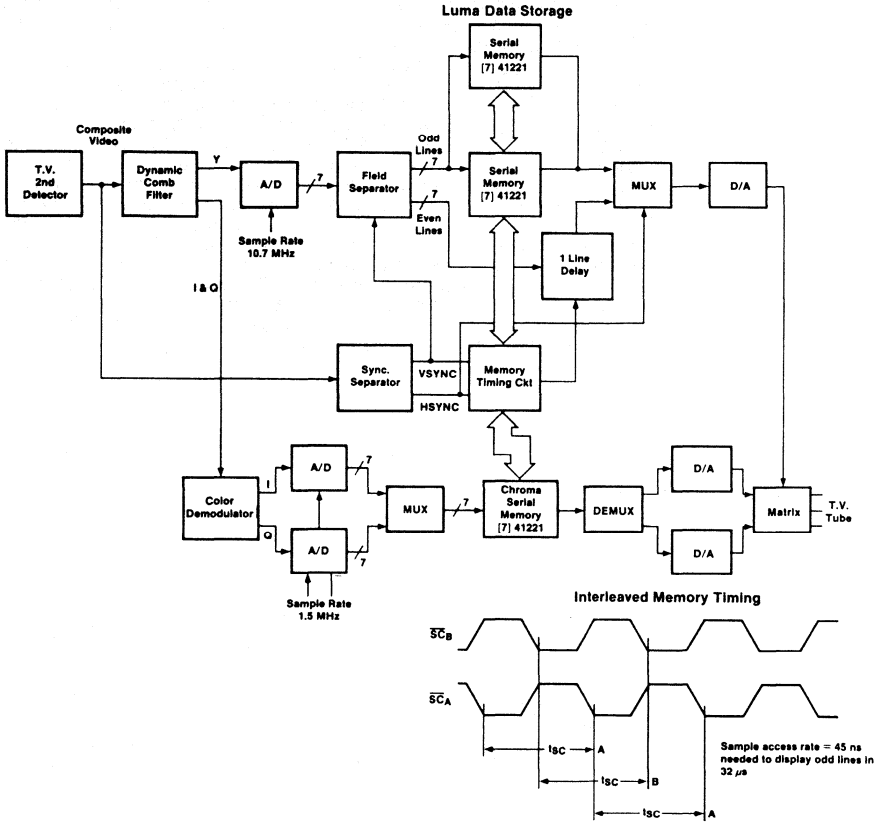


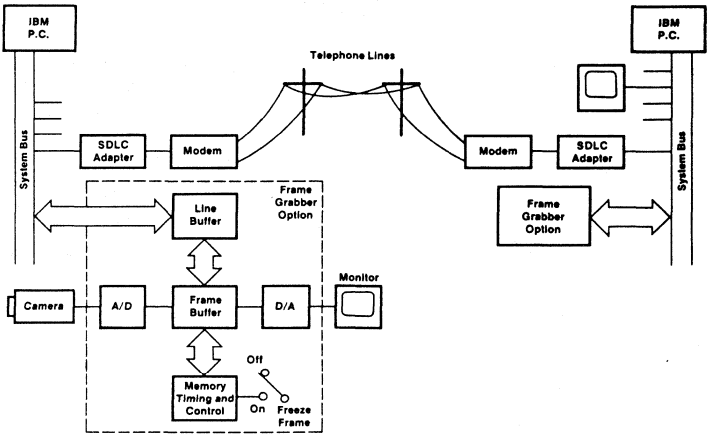
Image Freeze and Transmission

The personal computer in the automated office environment has many purposes, not the least of which is intercompany communications. Electronic mail is a great asset to the office but the ability to transmit images as well as text will open exciting new markets. Providing a means for people to view the same object even though they are thousands of miles apart will have a major impact on productivity while reducing costly travel.

The diagram in figure 9 shows a freeze-frame transmission option for the IBM Personal Computer. Two of the five I/O system bus card slots are utilized. Since the image data is transmitted over telephone lines, a modem and the synchronous data line adapter are required. The frame grabber would occupy a second card slot and would contain the μPD41221 devices, A/D and D/A converters, and the required memory timing and control circuits. The number of serial memories used is dependent on such factors as screen resolution, number of colors, text overlay, etc. A high speed line buffer is used to store one scan line of information.

While the tv camera analog signal is sampled and stored in the frame buffer it is simultaneously displayed on the monitor. (Displaying the frame as it is written in memory is possible because data-in appears at data-out during a write cycle.) A scan line of data is transferred to the line buffer where it awaits a DMA transfer cycle. Now in system memory the data can be compressed prior to being transmitted over the telephone lines. Once received the compressed signal is decompressed and displayed on the monitor.

Figure 9. Image Freeze and Transmission System



μPD41221 vs Standard DRAMs for TV Applications

For tv applications the DRAM is an awkward fit. Achieving the higher access rates requires using three RAMs in parallel combined with a high-speed shift register. The serial-parallel and parallel-serial conversion coupled with the complex logic and control circuits makes this technique a poor alternative. Interleaving page-mode cycles or use of static-column devices also adds circuit complexity and increases system cost. The use of DRAMs is also likely to require the addition of a CRT controller and/or DRAM controller.

Memory-timing circuitry for the system shown in figure 9 is relatively simple compared to that required using DRAMs. The logic diagram in figure 10 is an example of how the memory timing might be designed for the frame grabber section of the image freeze and transmission system. The momentary on/off switch S1 (write/read control) in the on position initiates the data transfer, serial write and data-restore cycle storing one frame of information. When S1 in the off position the frame buffer operates in the read and refresh mode, continuing to update the display.

After the horizontal and vertical sync pulses are stripped from the composite video, these signals are used by flip-flops U3 and U5 to generate the timing for the μPD41221. These signals control the field memory so that data restore and data transfer are performed during the horizontal retrace period. Serial data is read from or written to the field memory starting in the blanking period and continuing through the display period. The timing diagram for this system is shown in figure 11.

The counter U4 is used to generate the basic horizontal scan timing. The leading edge of the HSYNC releases the counter U4. Counter U4 counts the 2 MHz clock and decoder U6 generates $\overline{RAS}$ and $\overline{WE}$ for the data transfer and data restore functions. Outputs of the 74LS42 (1through4) are used for this purpose. $\overline{INC}$ and $\overline{RCR}$, which control the row addresses, are generated by decoder output 6. Decoder output 7 resets the counter, and data reading or writing begins. The $\overline{SC}$ signal is generated from the 3fSC clock. During the read and write time, the $\overline{REF}$ signal (generated by halving the 2 MHz clock) is available to perform memory-cell refresh.

With the momentary swich S1 in the normally off position, the $\overline{WE}$ signal is held high to allow the complete read out of the field memory. To store one field, $\overline{WE}$ is held low during the serial write time. This operation is controlled by counter U5. When switch S1 is pushed on, the memory is placed in the input mode. With all outputs high the counter loads on the next edge of the vertical sync setting QA low. QA controls the $\overline{WE}$ signal to set the one field write mode.

There are no addresses to be generated, no multiplexing, no latches and refresh ($\overline{REF}$) is provided by the 2 MHz output of U1. Using the 41221C, the control circuitry is reduced to about ten standard TTL logic ICs. This logic could be implemented in a gate array of about 250 gates.

A Peek at the Future

The new automated office and consumer applications will require the recording and transmissions of printed documents and photographic images. This facsimile-type transmission will demand low cost systems. Application-specific memories will play a major role in reducing the cost of these systems.

The cost advantages of NMOS DRAM mass production technology can now be applied to consumer products. In defining new devices, NEC is evaluating all operating parameters: speed, power, configuration and special on-chip circuits to best fit these new and emerging products. For example, field memory devices with capacities of 1 megabits could be used with high performance systems requiring four times the sampling rate.

Figure 10. Memory Timing and Control Chart

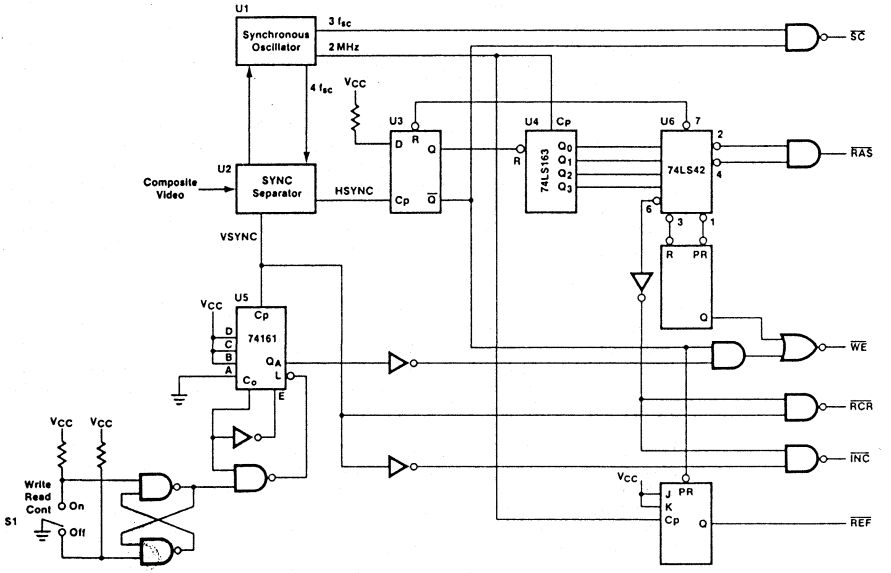
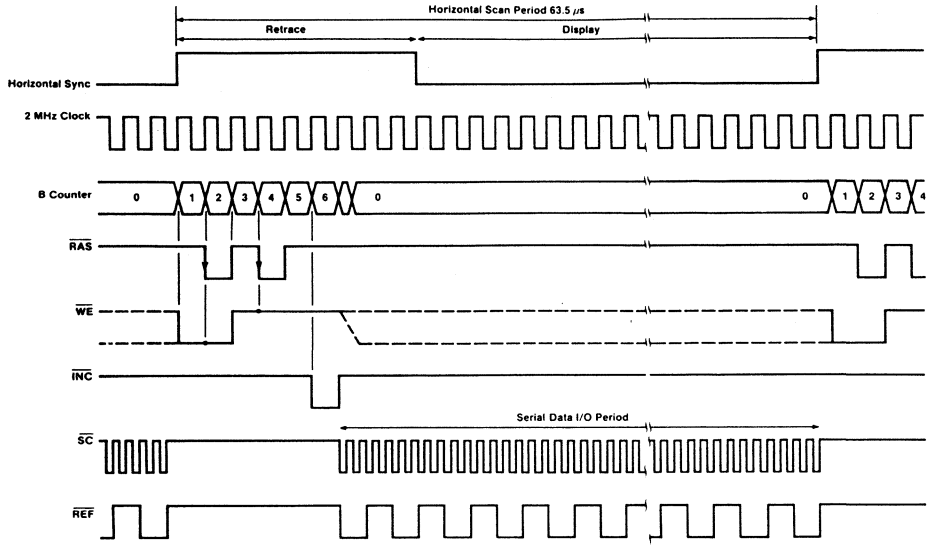


Figure 11. System Timing



Introduction

This application note describes the function of NEC's μPD41264 dual-ported memory and illustrates a graphics system that uses the μPD7220A Graphics Display Controller (GDC) and the μPD41264, operating in flash drawing mode. The first part describes the memory and the second part describes the system, with information on interfacing the video memory to the GDC and generating system timing.

μPD41264 Video RAM

Two real ports in a single piece of silicon is an exciting alternative to the use of standard memories and large quantities of TTL interface logic. NEC introduced the μPD41264 video memory at the 1985 International Solid State Circuit Conference (ISSCC). It combines a standard 64K x 4 DRAM with a high-speed 256 x 4 serial port. In this application, the serial port is referred to as port B and the random access port is referred to as port A.

The μPD41264 uses a double-poly-layer N-channel silicon gate process to provide high density, high performance, and high reliability. The 24-pin 400 mil DIP package is made possible by multiplexing two functions on a single terminal (DT/$\overline{OE}$).

Data Transfer Operation

The data transfer (DT) operation (figure 1) is initiated when $\overline{DT}/\overline{OE}$ is low before $\overline{RAS}$ goes low. The operation begins as in a standard DRAM; $\overline{RAS}$ strobes row-address information into the row-address buffer and the information is sent to the row decoder to select a word line. Cell data is then transferred to the bit line and amplified. The transfer from the memory cell to the data register occurs on the positive edge of $\overline{DT}/\overline{OE}$. 1024 bits of data are sent through the enabled data transfer gates and into the data registers. The data registers then contain the new data, which is immediately ready for the serial port. The DRAM (port A) remains in tri-state during this data transfer cycle.

In non-$\overline{DT}$ cycles, $\overline{DT}/\overline{OE}$ is held high, disconnecting the data registers from the memory array. The data transfer gates are disabled or turned off, allowing both ports to operate asynchronously. During this time, the CPU can access port A while port B updates the display. In this mode, port A operates as a standard RAM device, making an $\overline{OE}$-controlled write possible.

Port B Operation

While the DT cycle proceeds, the SC clock provides video clock rate timing to a serial selector which shifts data out each pin (SO_0 to SO_3). This activity is independent of the RAM port except during a data-transfer cycle.

This is the only time interval when the RAM port and serial port do not work independently. The serial port reads out data serially from the registers starting at a specified location. Data appears at SOi after an access time of t_{SCA}, referenced from the high transition of SC. With the speed of the SC clock, the data-valid time is short, making it difficult to latch the data into an external shift register. To solve this problem, the μPD41264 holds or latches the data until the next SC cycle.

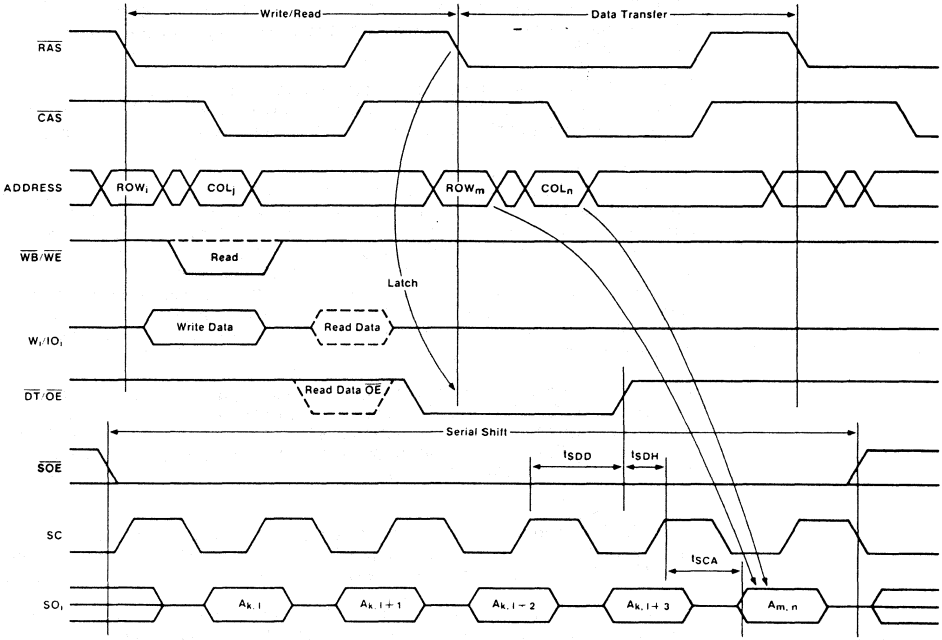
The $\overline{SOE}$ signal must be low during a serial-shift cycle. When this pin is high, port B is in a high-impedance state. The $\overline{SOE}$ pin allows you to combine multiple chips in parallel.

Once the DT cycle occurs, 1024 bits of data are transferred from the cell array to the data register, which is now ready to send new data to the serial port. In this cycle, eight bits of column address are latched in the address buffer and sent to an 8-bit counter. This counter specifies the starting location of the serial selector in the data register. After setting this pointer, the 8-bit counter increments once for each SC clock cycle and wraps around like a ring counter after 256 SC clock cycles. This technique allows you to exchange new data for old "on the fly" in real time withhout interruption.

This real time operation requires that DT and SC be synchronized to ensure a continuous stream of valid data. The rising edge of $\overline{DT}/\overline{OE}$ must maintain a t_{SDD} (setup time) and t_{SDH} (hold time) with respect to the SC clock. This data register update timing is significant because it removes the restriction of waiting for the horizontal-blanking time before passing new pixel updates to the shift register.

Write -Per-Bit Operation
Graphics applications often require changing only selected pixels while surrounding pixels remain unchanged. In a single-memory plane, when you change pixel data for vector generation, the only bits that change are the vector bits. Multiple-plane write-per-bit applications include changing text over a constant image or, in a

Figure 1. Timing Chart in a Data Transfer Cycle



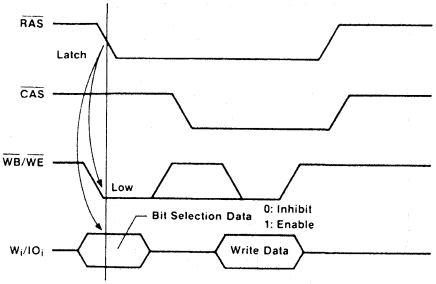
CAD system, changing only one layer of a VLSI chip. Standard DRAMs require two cycles or a read/modify/write cycle for this process. First, all four bits are read out; then the CPU modifies the data and rewrites it.

The μPD41264 can selectively access any one or combination of four bits. Latch the write-per-bit (WB) mode by bringing $\overline{WB}/\overline{WE}$ low before $\overline{RAS}$ goes low (figure 2). The bit selection or mask information is multiplexed on the common I/O terminal W_0/IO_0-W_3/IO_3. If the bit selection data is a logical 1, the common I/O terminal is enabled and new write data updates the frame buffer. A logical 0 inhibits the write and leaves the pixel unchanged.

If you perform a read/modify/write cycle, old mask data remains latched as long as $\overline{RAS}$ is held low. In a non-WB mode, this pin acts as a standard write enable, simultaneously writing all four bits.

Discussions with video systems houses reveal that competitive pressures are driving performance improvement. The independent clocking of the DRAM and serial port allows random access to occur simultaneously with shifting out video data. Asynchronous operation provides the CPU with almost 100% access to the frame buffer. Video RAMs allow the system designer to use his creativity to make the best use of the DRAM update time.

Figure 2. Write-Per-Bit Function Timing



The μPD7220A/ μPD41264 Graphics System

Figure 3 shows a block diagram of a μPD7220A-based graphics system. The display memory is made up of four μPD41264s to form a 16-bit-wide memory plane. The multiplexed input and output lines are directly connected to the μPD7220A address/data bus. The data bits in the μPD41264 data register are loaded into the 8-bit shift register through the four serial output lines. The timing-controller logic generates the signals required to synchronize all the blocks within this system.

Use of the μPD7220A

The μPD7220A interacts with the display memory in display cycles and drawing cycles. (Refer to the Data Sheet and the Design Manual for the μPD7220A for detailed discussion on the use of these features and others mentioned later in this application note.) Display cycles are made up of two 2 x WCLK cycles (2 x WCLK is the input clock to the μPD7220A). A display address is output during the first cycle and the data is available at the end of the second cycle. Drawing cycles are made up of four 2 x WCLK cycles. A drawing address is output during the first cycle and the μPD7220A reads the data from the display memory in the third cycle. It modifies and outputs the data at the end of the fourth cycle.

Drawing and display cycles are output in flashless and flash modes. In flashless mode, the drawing cycles are generated only during the horizontal and vertical blanking periods, and display cycles are performed during the active video time. This means that there are no display disturbances, but the update time is brief (15-20% of the total video time).

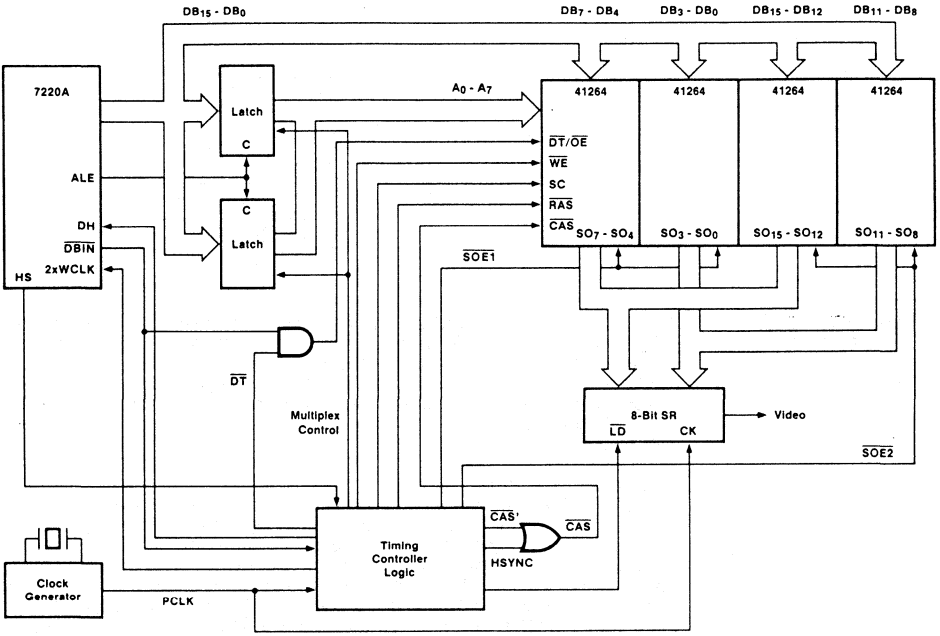
Flash mode allows drawing cycles to be generated at all times. Display cycles are output only when no drawing operation is in progress, or when the drawing hold (DH) pin of the μPD7220A is held high for four 2 x WCLK cycles. This mode increases the update rate by four or five times, but makes display interruptions more likely.

The drawing hold function allows the μPD7220A to interface to the μPD41264 VRAMs. The μPD7220A can then operate in flash mode.

System Interface to the VRAMs

As shown in figure 3, The 8-bit shift register input data lines are connected to the serial data outputs of the four μPD41264s. The serial output enable signals ($\overline{SOE1}$ and $\overline{SOE2}$) input to the μPD41264s become active one at a time. This loads the shift register twice in one SC cycle. The SO_7-SO_0 data bits are loaded into the shift register after the rising edge of the SC clock. The shift register is emptied before the first half of the cycle ends. Then, the SO_{15}-SO_8 data bits are loaded at the middle of the cycle after the falling edge of SC occurs. This method of memory bank switching eliminates the need for an extra 8-bit shift register. Because 16 bits overall are shifted out during an SC cycle, the value of the serial clock frequency is one-sixteenth of the pixel clock (SC = 1/16 x PCLK).

Figure 3. System Block Diagram



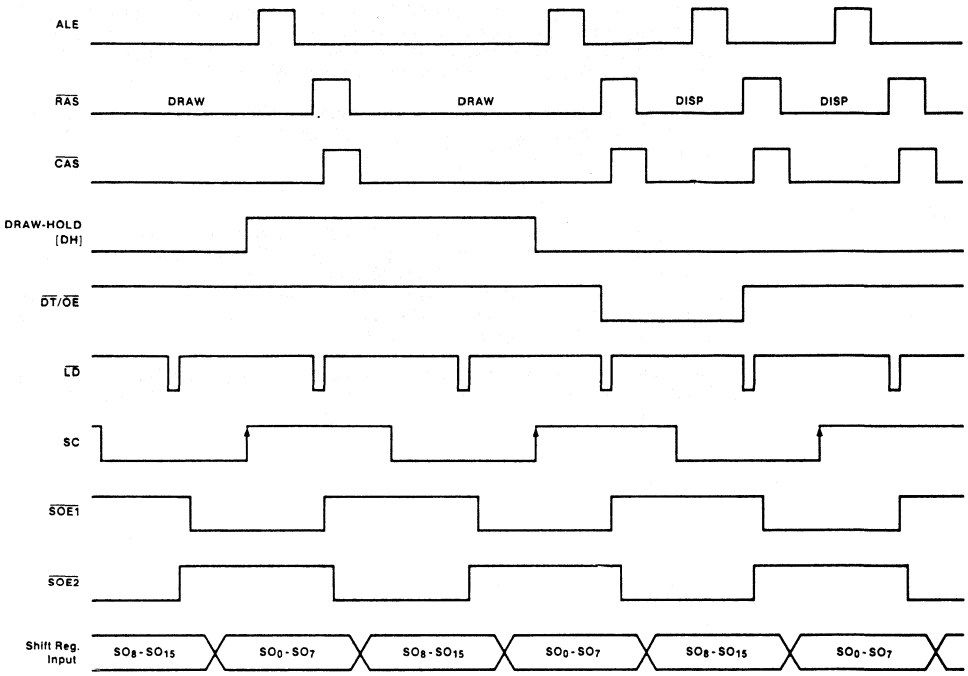
The serial output enable ($\overline{SOE}$) input signal enables the serial output buffers of the μPD41264. There is a delay between the time that $\overline{SOE}$ goes active and when the serial data bits become valid. The signal transitions of $\overline{SOE1}$ and $\overline{SOE2}$ should not coincide with the SC clock to prevent data contention while switching memory banks. If the SC clock period is too short, this time delay may not be tolerated, preventing memory bank switching. In this case, you should use an extra 8-bit shift register.

The falling edge of the ALE signal latches the 16-bit address from the μPD7220A into the tri-state latches. The timing diagram in figure 4 shows how the ALE signal is delayed to construct the $\overline{RAS}$ signal. Delaying the $\overline{RAS}$ signal by a few PCLK cycles generates the $\overline{CAS}$ signal.

System Operation This system uses three memory cycles: $\overline{RAS}$-only refresh cycle, read/modify/write cycle, and data-transfer cycle. The μPD7220A can perform the dynamic memory refresh if this is programmed in its RESET command. The lower 8-bit address lines (AD_7-AD_0) of the μPD7220A are connected to its internal 8-bit refresh address counter. This counter is enabled during horizontal sync and its output is available on the falling edge of the ALE signal. Therefore, $\overline{CAS}$ and horizontal sync should be gated so that the $\overline{CAS}$ cycle does not occur during this period. A refresh cycle is accomplished with the row address coming from the AD_7-AD_0 lines during the $\overline{RAS}$ cycle. The number of refresh cycles depends on the width of the horizontal sync (programmable in the μPD7220A)

A drawing cycle in the μPD7220A is basically an RMW cycle. The external logic uses the $\overline{DBIN}$ signal to control the data bus output direction. This signal is used to control the $\overline{DT/OE}$ inputs of the μPD41264s. When low, data is output from the memories so that the μPD7220A can read it. The $\overline{DBIN}$ signal also generates the $\overline{WE}$ (write enable) signal. This is accomplished by delaying $\overline{DBIN}$ by one and one-half 2 x WCLK cycles and ORing the result with the 2 x WCLK signal (see figure 5).

Figure 4. Timing for Memory Cycles



Setting the image bit and GD bit to one increments the display address every other display cycle. This mode allows you to double the μPD7220 clock rate while maintaining the occurrence of display addresses as in normal mode, thus doubling the drawing speed. This is shown in figure 6. DAD represents the display address.

A data-transfer cycle is the same as a read cycle except that the $\overline{DT}/\overline{OE}$ input signals of the μPD41264s must be low before $\overline{RAS}$ occurs. The external logic should generate a draw hold (DH) signal to the μPD7220A before generating this cycle. The DH signal must be high for four 2 x WCLK cycles so that the μPD7220A can complete the current drawing cycle. After the DH signal goes from high to low, the μPD7220A generates two consecutive display cycle. The external logic can then use these display cycles to perform a data-transfer cycle. Figure 4 also shows the timing for this event.

The rate at which data-transfer cycles occur depends on the mapping of the display memory. If the mapping is such that the screen width is equal to the actual width of the display memory (in μPD7220A terms, this is referred to as the pitch parameter), a data-transfer cycle is generated every 256 SCLK cycles. Depending on the horizontal pixel resolution, the data-transfer cycle could take place during a raster-scan period. If so, you should perform a real-time data transfer.

If the screen width is less than the display memory width, generate a data transfer cycle during every horizontal retrace period to put data for the next horizontal line into the data registers of the μPD41264s.

Conclusion

So far, graphics systems based on the μPD7220A and regular dynamic memories have not been able to take full advantage of the μPD7220A's drawing speed; mainly because most systems use the μPD7220A in flashless drawing mode to avoid display disturbances. However, the advent of the μPD41264 makes it possible to use the flash drawing mode, increasing the drawing rate to four or five times the rate of systems using regular dynamic memories.

The key to this increased drawing rate is the dual data ports integrated into the μPD41264. The μPD7220A can communicate with port A to update the display memory at the same time that port B is being used to update the video display.

Figure 5. Timing for Drawing Cycles

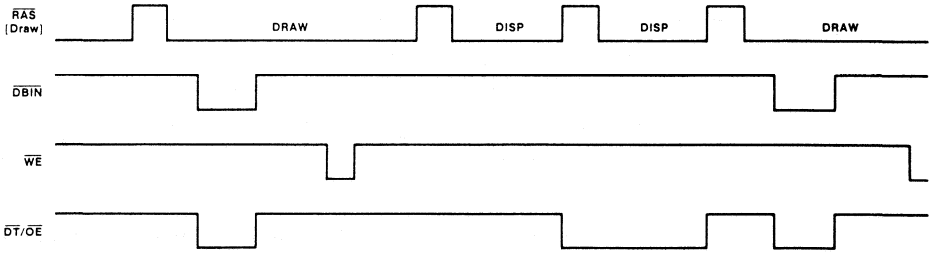
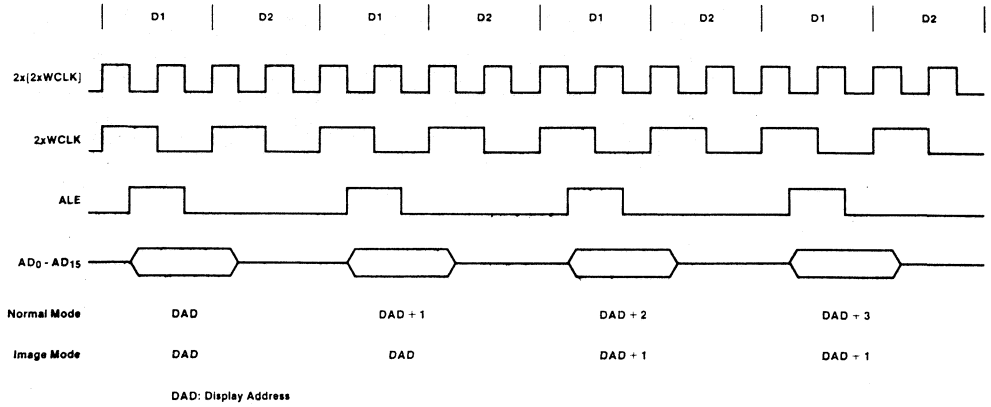


Figure 6. Image Mode and Normal Mode



Development of a 256K-Bit Dual-Port Memory for Frame Buffering with Capability of Uninterrupted Serial Output

262, 144-BIT DUAL-PORT DYNAMIC NMOS RAM

by Satoru Kobayashi, NEC Inc., Memory Technology Headquarters

NEC Inc. has developed a 64K x 4-bit dual-port dynamic memory chip with a key design emphasis on its ease of use in frame buffering for bit-mapped displays. The commercial part number is μPD41264. While it is accessed randomly, the memory is capable of displaying data output in a serial mode at the maximum rate of 25 MHz. In addition to this, as basic features, it has three new functions. They include the function to internally transfer data into the data registers designated for serial output while performing the output function of the display data. To accomplish the intended functions and performance level, the manufacturing technology has been kept the same as the existing one, while the circuit designs were modified. When this memory is used, updating the displayed data becomes several times faster than conventional methods.

The advancement in semiconductor technology has been significant since the beginning of the 1970s. In the field of integrated circuitry, various types of technological innovations were made with the goal of higher density in integration, lower power dissipation, and lower costs.

Among such innovations, most notable changes occurred in the MOS dynamic memory. First, with the advent of the 1K-bit dynamic memory, the traditional magnetic core was replaced by semiconductor memory. Since then its capacity has been increasing by a factor of four every 2 to 3 years. At present the 256K-bit products are prevalent in the marketplace, and it appears as if sometime in 1985 specimens of 1M-bit memory might appear.

Product Diversification Started with 64K-Bit Products

The transition has been characterized by the increase in chip memory capacity; about the time the 64K-bit products appeared, product diversification started. Not only did we see improvements in the basic functions aimed at a decrease in access time and a reduction in power dissipation, but we also started seeing products with functions making them easy to use by increasing the tolerances in their critical timings, new refreshing methods, etc. At the same time, specialized memories dedicted to specific applications started appearing along with the 64K-bit products.[7,11-13]

For instance, in addition to the conventional page mode, new high-speed access modes such as the nibble mode, static column mode, and ripple mode were introduced.[3,4,9] Then there were peripheral CMOS-type dynamic RAMs that combined the CMOS technology in peripheral circuits for the specific purpose of lowering power consumption. Moreover, to improve the ease of use, CAS-before-RAS refresh and self-refresh were introduced as additional functions plus functions to moderate the timing criticality in the areas of RAS time-out in static column mode and timeout during write.

Owing to these improvements in functionality and performance, the burden on users designing their systems was reduced. It should be noted, however, that these improvements were made with the anticipation of primary use as the main memory of large-scale mainframe computers. They were not developed for use in small systems, which have seen a dramatic rise in popularity in recent years. For this reason, they were not the kinds of functions that were necessarily easy to use from the viewpoint of small system designers.

Demands Are Increasing for Display Memories To Be Used in Small Systems

During the latter half of the 1970s, microprocessors began to be used in various types of electronic equipment. At the same time, a demand for memories was created for small systems such as personal computers, word processors, computer terminals, work stations, and CAD/CAM systems. Along with the rise in popularity of microprocessors, the unit price per bit of dynamic RAMs came down dramatically. The falling prices spurred a drastic increase in the volume of dynamic RAMs used in small systems. As a result, the ratio of their use is now reversed between small and large systems.

The application of RAMs in small systems can largely be divided into main memory and display memory. The main difference between small and large systems is that in small systems the ratio of RAMs used as display memories for storing character and graphic data is extremely large. The size of display memories per system ranges from several tens of kilobytes to as many as several megabytes, whereby the trend shows that the size has become equivalent to or larger than that of the main memory itself. It is expected that the demands for RAMs for display memories will continue to grow. There are speculations based on actual usage that within 2 to 3 years as much as 30 to 40 percent of dynamic memories will be used for display purposes. Among display memories, frame buffers for bit-mapped displays will see a dramatic market expansion.

As Memory Capacity Increases, Conventional Chips Become More Difficult To Use.

Some aspects of the traditional standard chips render them difficult to use as frame buffers. Worse yet, as memory capacity increases from 256 kilobits to 1 megabit, problems stemming from difficulties associated with their use will become much more serious.

First, in the area of x 1-bit patterns, which have traditionally made up the main type of RAMs, if the capacity increases, there will be situations in which the length of a word is too deep. At present, the capability for display resolution is generally in the range between 256 x 192 and 1280 x 1024 pixels. For instance, when a 256K-bit memory is used in a small-scale 256 x 192 pixel display, five planes can fit into one chip. It is difficult not to waste memory cells; the peripheral circuits tend to get large. Although there are specimens of x4-bit and x8-bit pattern memories, their main applications are for main memories in small systems. When they are used for frame buffers, and if the memory capacity requirement per chip is increased by a factor of four, then there is a tendency that this setup would spur demands for the word length also to be expanded by a factor of four. But if this is to be done, the number of pins needed would increase and the package size would become large, hence diminishing the advantage of a large capacity memory.

The memory cycle time is also a problem. For instance, in a display of 1280 x 1024 pixels, the display data are sent to the CRT at a speed of about 9.3 nanoseconds per pixel.[5] This is significantly shorter than the cycle time of conventional dynamic RAMs. For the purpose of mitigating the speed difference, the user must resort to a technique taking out the data in parallel from a number of dynamic RAMs and converting the data into a serialized stream. For this, either parallel-to-serial conversion registers are used or a technique is used to enable the dynamic RAMs in a time-sliced synchronization schedule. Either way would result in bloated peripheral circuitry while the number of connection lines would increase on the printed circuit board. This, in turn, would become a burden during the PC board designing phase. As a result, even though it makes a large capacity memory possible, actual use in a system is difficult.

The basic function of a frame buffer is to send display to the CRT at a designated speed. The performance level of a system is determined by the efficiency with which the processor can refresh the display data while continuing this basic function. A frame buffer requires two access ports.[10] But a conventional standard dynamic RAM has been characterized as being a single-port memory, namely, containing only one set each of data input/output terminals and address input terminals. While the display data are being output to the CRT, this type cannot concurrently allow the processor to perform the memory access. There is only one remedy to this: introduce the time-slicing scheme so as to use it as a pseudo-dual-port memory.

There are primarily two methods of time-sliced access to a frame buffer. One is to permit CPU access to it only during the blanking phase of the display, while CPU access during the data display phase is restricted to sending display data to the CRT. This would invariably reduce the access efficiency of the processor to 20-30 percent. Another method is the cycle-steal method wherein the timing intervals are so minutely divided as to allow the processor access to the memory even during the display phase. As compared to the first method, the operational efficiency is improved; however, it requires complex high-speed peripheral circuits.

As pointed out in the foregoing, conventional standard dynamic RAMs are difficult to use for frame buffers. In principle, it is possible to assemble a large capacity memory into a frame buffer so long as it can function at a high rate of speed. Moreover, it is possible that, as replacements to the traditional page memory, techniques will be developed to use this type of memory in such high-speed access modes as the nibble mode, static column mode, and ripple mode.[5,9] But for this type of memory to be used in such modes, additional externally attached circuits are needed between it and the microprocessor. If it is a single-port memory, building a frame buffer out of it becomes more difficult as its memory capacity becomes larger.

A Dual-Port Memory Solves Frame Buffering

Of various memories used for displays, we judged that the most adequate solution for a memory chip to be used for frame buffering was a genuine dual-port memory. Hence, we started our development efforts accordingly. The results were the dual-port dynamic memory (μPD41264), about which we published details in February 1985.[1,6,8]

As illustrated in figure 1, it is equipped with a 64K x 4-bit random access port, and a 256 x 4-bit serial access port. The serial port consists of four 256-bit data registers, each allowing serial output at the maximum rate of 25 megabits/second. This serial port can be used as a dedicated port for sending display data to the CRT. When a 4-bit parallel-serial converter is externally attached to it, it can send display data to the CRT at 100 megabits/second.

The random access port does not have to get involved in display data output to the CRT except for timing the internal transfer of 1024-bit data blocks from the memory cell arrays. Using this memory chip, there is no need to resort to a cycle stealing technique to increase the access efficiency of the processor; in fact it can obtain nearly 100 percent efficiency.

In addition to the foregoing,we also devised measures to keep the memory cell usage efficiency rate near 100 percent regardless of what type of pixel configuration the display may consist of. The design intent was to allow it to accommodate a wide range of uses as a frame buffering memory, from low-resolution to high-resolution displays.

Dedicated Memories Deployed As the Market Determines

As for dynamic memories, we have entered a period when dedicated memories should be developd for a specific application, focusing on the functions and performance level it calls for so long as the market size is large enough. As we mentioned before, the area in which the memory demands will see a dramatic increase in the near future is display memories. We have classified the display memory field in figure 2. We divided the field into computer, television, telecommunications, and hybrid application groups, and established a basic goal of developing dedicated memories best suited to each application group. We have already commercialized a dedicated product (μPD41221C)[2] for television and telecommunication applications. This product was designed as a field memory for television and VTR applications by allowing high-speed serial input/output cycles. Since it is specialized for applications that do not require direct data manipulation by the processor, no random access function was provided. This allowed the chip to be packaged as a 14-pin DIP. The dual-port memory chip that we are introducing as a product this time is aimed at the computer applications group.

Figure 1. Basic Configuration of a Dual-Port Dynamic Memory

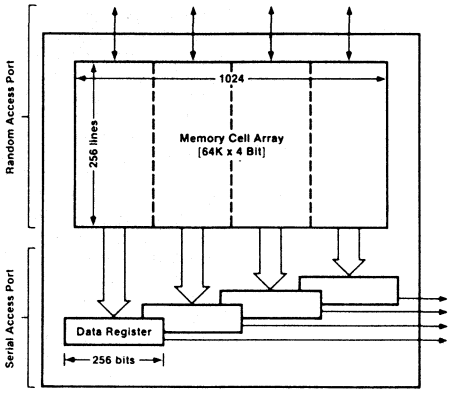
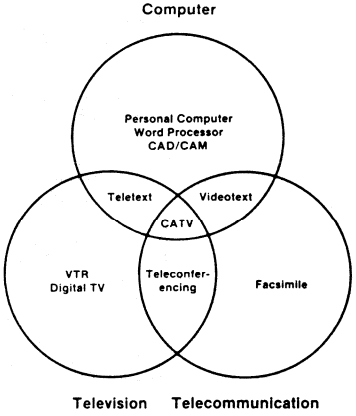


Figure 2. Application Fields of Display Memories



Functions Added for Frame Buffer Applications

The functional block diagram of the dual-port memory that we developed as a product this time is illustrated in figure 3. In addition to the 64K x 4-bit dynamic RAMs, we added a circuit that creates a serial port. The latter can internally transfer in one cycle a line of 1024 data bits from the memory cell array to a 256 x 4-bit register. Interfacing with the internal data transfer are the data transfer gates, which consist of 1024 transistor arrays. This setup makes it possible to serially output the data stored in the data registers by means of a selector and an output buffer. Its maximum output speed is 25 megabits/second.

Instead of shift registers, the serial-port registers were made of circuits that allow selective output of data from the data registers via a selector. Because of this design, it was possible to realize the pointer-control function to start serial output from any array address immediately following an internal data transfer.

The package is a 24-pin plastic DIP (figure 4). Because of the serial-port circuit, the width of the chip grew. For this reason, a 10.2-mm (400-mil) wide package was required. The terminals that are provided in the package but missing from the conventional standard-type RAMs are the serial clock (SC) terminal that controls the

serial port, the serial output enable (SOE) terminal, and the serial data output terminals (SO_0-SO_3), a total of six terminals. In addition, a data transfer control clock ($\overline{DT}$) for internal data transfer to the serial ports, a write per bit control signal ($\overline{WB}$), which became a necessity for the newly created functions, and the mask data input signals (W_0-W_3) were added as new features. However, to keep the increase in pins to a minimum, these were piggy-backed onto the conventional signal terminals.

Table 1 summarizes the primary timing charactreristics of the μPD41264-12 product. With regard to refresh function, it requires 256 refresh cycles in 4 ms, the same as conventional dynamic RAMs. Since a refresh address counter has been provided internally, it is possible to allow the CAS-before RAS refresh function. The input-output signals are handled entirely at the TTL level. In addition to the μPD41264-12, we also provided another product (μPD41264-15) with a maximum RAS access speed of 150 ns.

Figure 5 shows the source current wavefrom. When two ports are active simultaneously, current is 155 mA maximum. When ports are idle, current is 12 mA maximum.

Table 1. μPD41264-12 Timing Characteristics

RAS access time	120 ns max
CAS access time	60 ns max
OE access time	35 ns max
RAS cycle time	230 ns max
Serial access time Serial cycle time	40 ns max 40 ns min
SOE access time	35 ns max
Refresh	256 cycle/4 ms

Note:

(1) The cycle time in page mode is 120 ns minimum.

(2) In addition to RAS-only refresh, it is also furnished with the CAS-before-RAS refresh function.

Three Functions added for Ease of Use

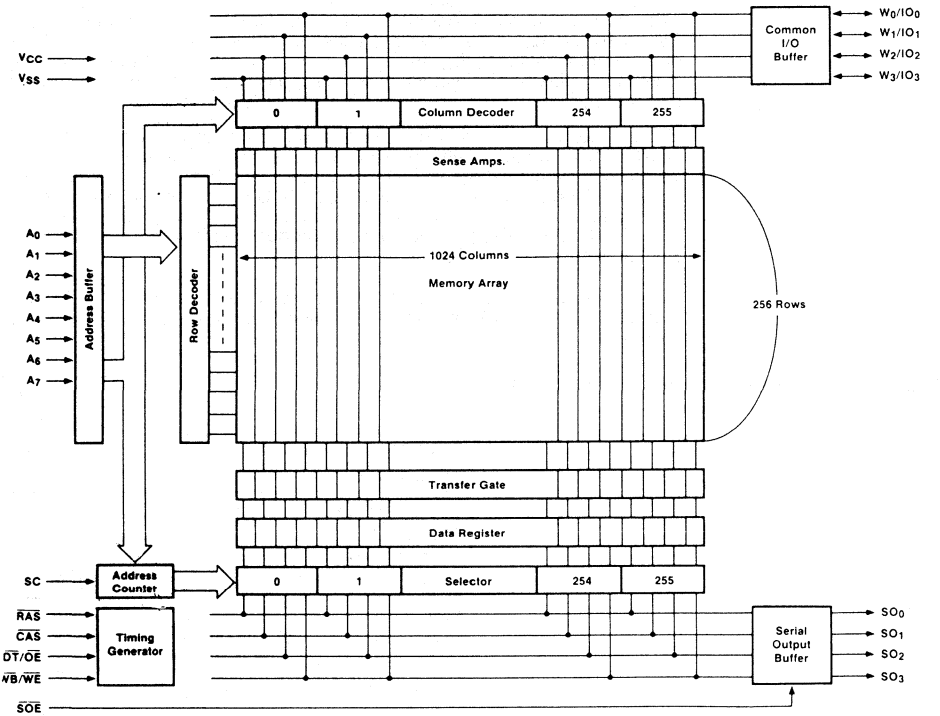
We added three new functions to make the dual-port memory easy to use. One is the write-per-bit function, a new write mode for the random port. When this mode is used, of the 4-bit cells that can be selected during a random access mode by means of the row and column address specifications, it is possible to update the contents of any given cell in one RAS cycle. Although the cell is of 4-bit pattern, write access is possible on a bit basis. In the areas of graphic pattern processing, there are times when the processor accesses the frame buffer(s) on bit-based units. This is a new function to address such demands.

By addition of two functions we call the pointer control function and the real-time data transfer function, we made it easy to use the serial port. When the pointer control function is used, horizontal scrolling of dots is made simpler. When the real-time data transfer function is used, it becomes possible to stop the waste of memory cells by flexibly adjusting to the display pixel patterns.

Serial Output Continues During Internal Data Transfers

Figure 6 shows timing control during internal data transfer. Just like the ordinary random access cycle, the internal data transfer cycle also begins with a timing of the falling $\overline{RAS}$ signal. Which cycle the timing belongs to is determined by the level of the data transfer control clock ($\overline{DT}$). Hence, when $\overline{DT}$ is kept at a high level during timing of the falling $\overline{RAS}$ signal, it means an ordinary random access cycle. Conversely, when the $\overline{DT}$ level is low, it means a data transfer cycle.

Figure 3. Block Diagram of the Functional Interior



In the example of figure 6, a row address M is specified during the data transfer cycle. By means of this, the contents of row M are newly transferred into a data register and then output serially from the serial port. The actual operation of how the data in row M is read from the serial port is illustrated in figure 6. First, the $\overline{DT}$ signal is restored to a high level during the data transfer cycle; then data readout begins with the very first start-up timing of the SC clock.

Similary, in order to update the contents of the data register(s), it is necessary to set up data transfer cycles using the random port control signals. During this period, only the random port is disabled from performing the ordinary random access function. However, as shown in figure 6, the functioning of the serial port can be continued without interruption. As described above, we provided a function to perform the internal data transfer while continuing the serial output. This we named the real-time data transfer function.

To accomplish the foregoing objectives, we provided only one timing rule between the SC signal, which is used by the serial port during data tranfer cycles and the data transfer clock, which is the signal from the random port side. They are shown in figure 6 as t_{SDD} and t_{SDH}. To accomplish the real-time data transfer, we introduced the restriction that both t_{SDD} and t_{SDH} be kept above 10 ns. As a method of meeting this requirement, we recommend a technique of synchronizing the timings between the start-up of $\overline{DT}$ during the data transfer cycle and the falling of SC. Since one phase period of SC is a minimum of 40 ns, even when the serial port is utilized at its maximum speed, this woud allow a margin of about 10 ns for the start-up timing of $\overline{DT}$.

Figure 5. Source Current Waveform

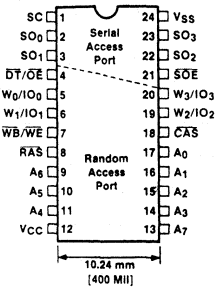
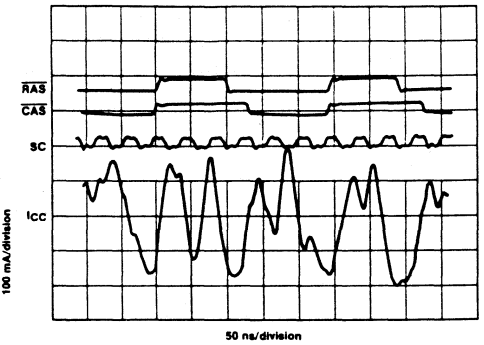


Figure 4. Pin Configuration, 24-Pin Plastic DIP



Owing to this real-time data transfer function, it is possible during the display to perform the internal data transfers needed to update the data within the data register(s). For this reason, it is possible to relate the data equal to one horizontal line to a plural number of lines within the memory. As a result, regardless of the pixel configuration of the display, it became possible to make the usage efficiency of the memories making up the frame buffer(s) very close to 100 percent. It should be noted that during a data transfer cycle, the data output pin of the random port turns into a high-impedance state.

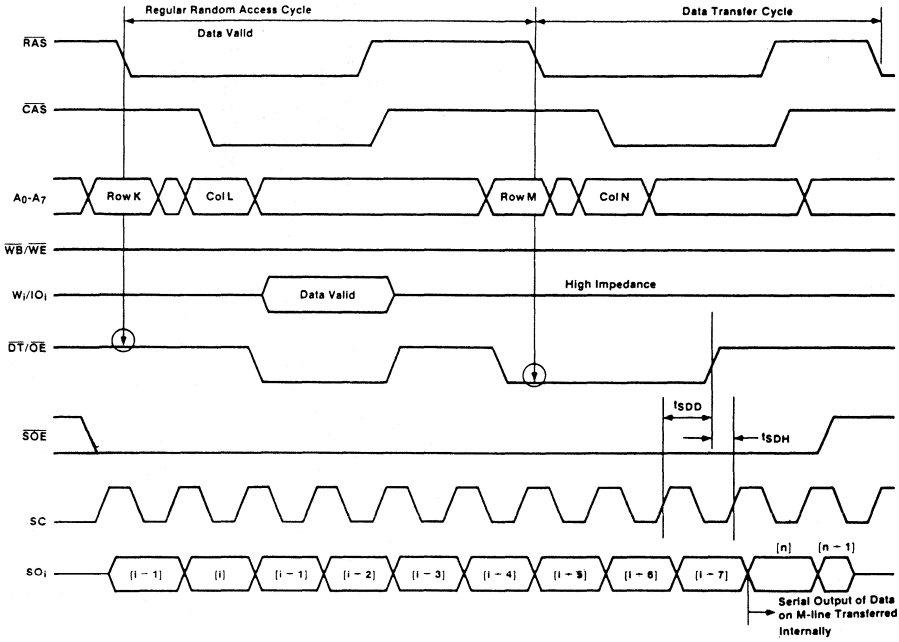
Although it is true that by virtue of the real-time data transfer function, the memory assignment can be accomplished freely regardless of the pixel configuration of a given display image, it is necessary to be careful of the refresh of the internal data register(s).

Because the serial port also consists of dynamic circuits, it is necessary to repeat the internal data transfers within a cycle period of 4 ms. During a vertical interlacing period of the display, it is always necessary to perform the internal data transfer prior to the beginning of display.

Pointer Control Function

As shown in figure 3, the serial readout port consists of the 256 x 4-bit data registers and the selector that serially selects and outputs their contents. Using such a design configuration, we made it possible to freely select the address of the data register from which to start the readout after the completion of internal data transfer(s). We call this the pointer control function.

Figure 6. Internal Data Transfer Timing



In the timing example of figure 6, the column address N is specified by means of the $\overline{CAS}$ signal at the time of the internal data transfer. Its value determines the staring address of the data register. As shown in figure 6, it is after the $\overline{DT}$ signal is restored to the higher level during the data transfer cycle that the data in row M column N is read out by the first SC clock. Using this function, it is relatively easy to accomplish the horizontal dot scrolls.

A serial counter governs the pointer control function as shown in figure 3. This 8-bit counter counts the SC signals, and its output becomes the address of the selector, thereby serially selecting the contents of the data registers. By furnishing this counter with a control preset function and by assigning a predetermined value to it as the column address at the time of internal data transfer, we enabled it to perform the aforementioned function of determining the starting address of the selected data register. Note that the serial address counter directly counts the SC signals and that its action is not designed to be stopped by means of a serial output enable $\overline{SOE}$ signal.

Write-per-Bit Function Timing

The write-per-bit function is a new random access function by which any specific memory cell can be rewritten on a bit basis in one $\overline{RAS}$ cycle, even though its design is 4-bit based.

Figure 7 shows the timing aspects of the write-per-bit function. During the falling phase of the $\overline{RAS}$ signal, if the $\overline{WB}/\overline{WE}$ signal is high level, it is the ordinary access mode the same as conventional memories. If the $\overline{WB}/\overline{WE}$ signal level is kept low during the $\overline{RAS}$ signal falling phase, the access mode becomes the write-per-bit mode. In write-per-bit mode, to determine which of the 4-bit data terminals is to be write-enabled, mask data are input to the W_i/IO_i terminal during the $\overline{RAS}$ signal falling phase. When the level of the mask data is high, the terminal is write-enabled wheras when it is low the terminal is write-inhibited.

The foregoing function was accomplished by furnishing one internal circuit to determine the level of the $\overline{WB}/\overline{WE}$ signals during the $\overline{RAS}$ signal falling phase, and another to latch the determination as the mask data. This mask-data latch circuit is reset each time by means of the RAS clock. For this reason, it is necessary that the mask data be reset each time the RAS cycle takes place. In page mode, the mask data is set up in the very first RAS/CAS cycle when the mode shifts to page mode and the same value is retained so long as page mode continues. In page mode, it is not possible to update the mask data in each and every CAS cycle.

New Functions and Performance at Low Cost

When we set about developing the new memory chip, one important prerequisite was to keep the production cost as low as possible. Our market research revealed that no matter how outstanding the functions and performance, unless we keep the price at 1.2 to 1.5 times that of the conventional standard 256K-bit RAM chips, the new chip would not be accepted by large number of users.

To achieve high access speed, there were efforts to bring in CMOS technology, which was already adopted in RAMs with static column mode.[3] At present, however, we judged that the way to realize a low-cost memory chip is undisputedly that of NMOS circuits. Consequently, we opted to adopt directly the process technology of NEC's traditional standard 256K-bit dynamic RAMs (see table 2). Since we can use the existing production line without modification, productivity can be kept at the same level as standard dynamic RAMs. If process conditions were altered, they could bring about factors that would raise costs, such as an increase in the number of masks or degradation in the flow of production lines. Against the background of such constraints, we realized the functions and performance of the new memory chip only by revising the design technology of the peripheral circuits while retaining the existing dynamic RAM as a core structure.

Chip Layout

The layout of the new memory chip is shown in figure 8. The rectangular circuit block at the left side was added for this chip. The remaining section is basically identical to the existing 64K x 4-bit dynamic RAM chip. It is characterized by a folding bit-line structure and its sense amplifier block was placed in the periphery. The row decoder, which selects bit lines, was placed in the center. The data registers, selector, and the serial I/O bus, which together compose the serial port, had to be placed close to the memory cell array.

The I/O bus and he row decoder of the random access port must be connected to the pair of bit lines connecting to the sense amplifier. Moreover, the data registers and the selector of the serial port must also be connected. While giving design priority to the serial port, which operates at a high rate of speed, we placed the row decoder in the central part of the gate arrays, a little bit separated from the sense amplifier. The serial port's circuits were placed in the outer rim of the gate arrays adjacent to the sense amplifier. Since the highspeed operating serial port becomes a major source of noise, by placing it at an outer rim we can expect to reduce the probability of transients.

Since we cannot avoid an increase in the surface displacement to the chip, the restriction in packaging was particularly severe in the shorter sides of the chip package. To prevent an increase there, dimensions of the memory cells in terms of the width and length ratio were slightly altered from that of conventional 64K x 4-bit RAMs (6 x 10μm). The cell capacity remained the same.

Figure 7. Write-per-Bit Function Timing

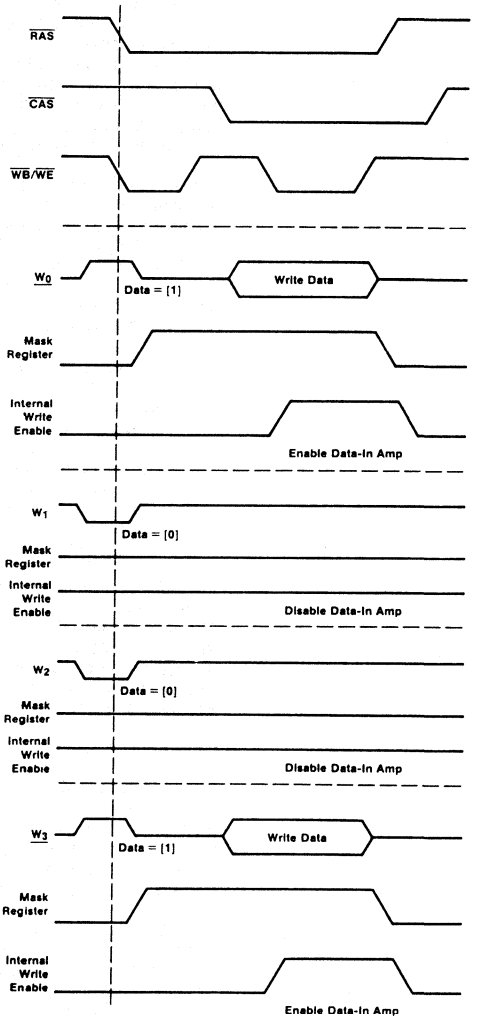
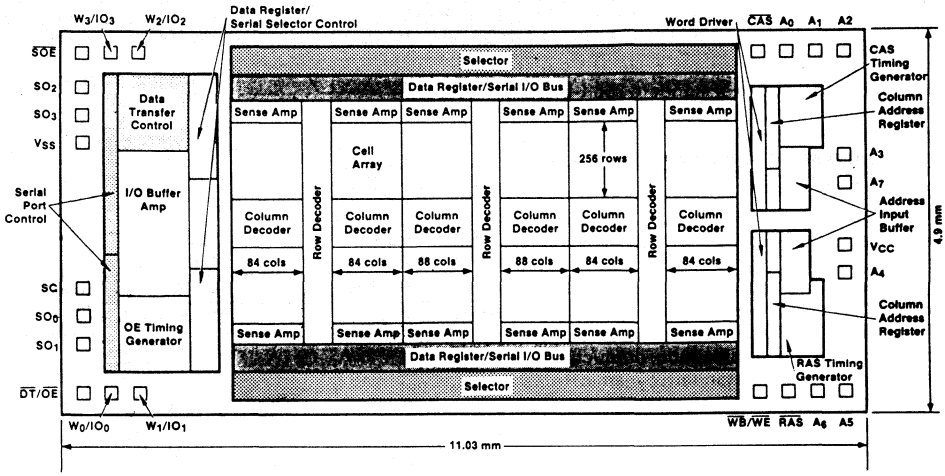


Figure 8. Layout of the Dual-Port Memory Chip



Data Registers

Figure 9 illustrates the architecture of circuits from the data I/O terminal of the random port I/O_i and the output terminal of the serial port SO_i to the sense amplifiers.

The two boxed-in sections indicate the data registers, which are connected to individual sense amplifiers. A set of 256 such circuits make up a serial output terminal.

The bit-line signals, which were amplified by the sense amplifiers, are sent to the serial port and the random access port. The real-time data transfer was accomplished by bypassing the data registers and providing the relay channel to send the signals amplified by the sense amplifiers directly to the serial output terminals.

The functioning of the random port is similar to that of conventional dynamic RAMs. For the serial port, the data registers read in data from the memory cells during the internal data transfer cycle and they retain the data until the next data transfer cycle. Next, the output from the data registers becomes the input to the differential amplifiers attached individually to each register. The differential amplifiers are given the enable state by means of output signals from their selector, which then sends signals to the differential amplifiers connected to the serial output terminal. A set of 256 data registers and differential amplifiers is connected individually to each serial I/O bus depicted in figure 9. The output signals from the selector serially cause them to become enabled, hence causing the data to appear serially from the serial output terminal.

As shown in figure 9, for the data registers we adopted differential amplifiers consisting of MOS transistor pairs. Because we minimized the burden capacity of each bit-line, which would increase when the data registers were connected, the operational tolerances of the sense amplifiers did not diminish.

For the purpose of amplifying the contents of the data registers selected by the selector and to send them to the serial output terminal, static-type differential amplifiers were connected vertically. Since they operate at such a high speed as the maximum 25 MHz, no dynamic circuit can be used in this area. Hence the circuits used in the n-MOS static RAMs were adopted without modification.

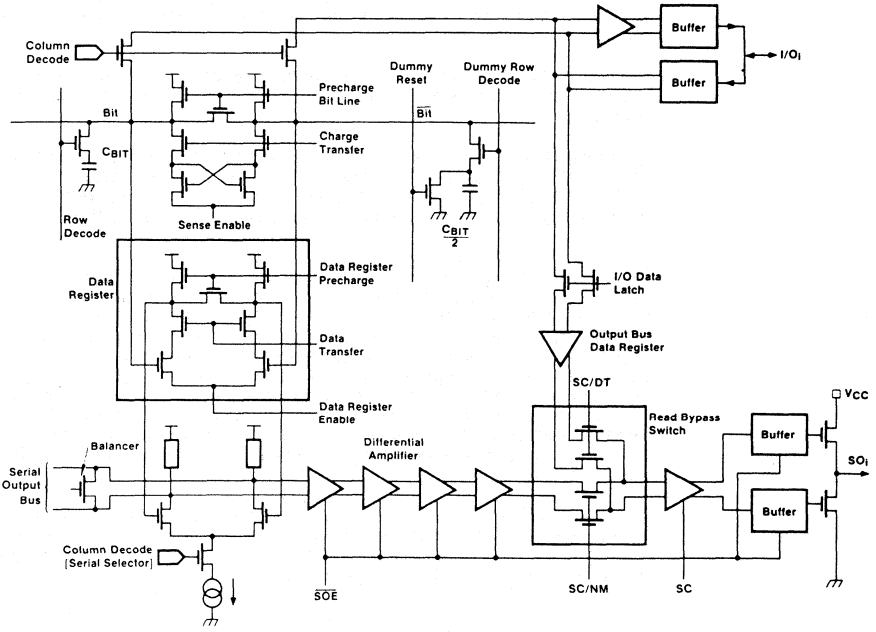
The serial port, which operates at high speed, was placed in the periphery.

Table 2. Processing Technology of the Dual-Port Memory

Polycrystalline Si gate	n-MOS process
n-MOS channel length	1.7 μm
Thickness of gate oxide Memory cell area Peripheral area	 16 nm* 40 nm
Memory cell structure	n-MOS transistor capacitor
Memory cell area	60 μm^2 [6 x 10 μm]
Chip dimensions	4.94 x 11.03 mm
Pre-charge level of bit-line	V_{CC}
Word-line level	Boosted level (higher than V_{CC}
Substrate bias generator	Internally provided

*Converted in terms of SiC_2.

Figure 9. Data Register Circuits



Internal Data Transfer Cycle

The area in figure 9 that required a significant amount of our efforts was the signal relay channel we built for the purpose of sending directly to the serial output ports the data ordinarily directed to the random port (see the right-hand side of the same figure). By bypassing the data registers, and thus taking the output from the sense amplifiers directly to the serial port, it became possible to accomplish the real-time data transfer. The internal data transfer begins with the start-up of the $\overline{DT}$ signal timing. To accomplish the real-time data transfer, the first data must be output within 10 ns of this $\overline{DT}$ start-up timing (figure 6). This operation cannot be done by ordinary procedures using the data registers. For this reason, as illustrated in figure 9, we furnished bypass channels, which were designed to output only the start-up data after the completion of the internal data transfer. In the bus architecture, as compared to ordinary access cycles, the contents of the memory cells are amplified, and they can be determined by specifying the row and column addresses. Although the data output terminal on the random port side is set to high-impedance mode during internal data transfer, its operation is identical to the ordinary readout cycles until it reaches the output buffer phase.

Figure 10 is a block diagram of the circuit to generate the timing signals for controlling the random port. The three asterisked blocks have been newly added. The DT/$\overline{OE}$ level comparator checks levels of the $\overline{DT}$/$\overline{OE}$ signals at the time of the $\overline{RAS}$ ascent to determine whether data transfer or ordinary cycle is being invoked. The DT timing generator creates the internal timing signals to be used for data transfer cycles. The mask register retains mask data for write-per-bit operation.

Figure 10. Block Diagram of the Timing Generator Circuit Controlling the Random Port

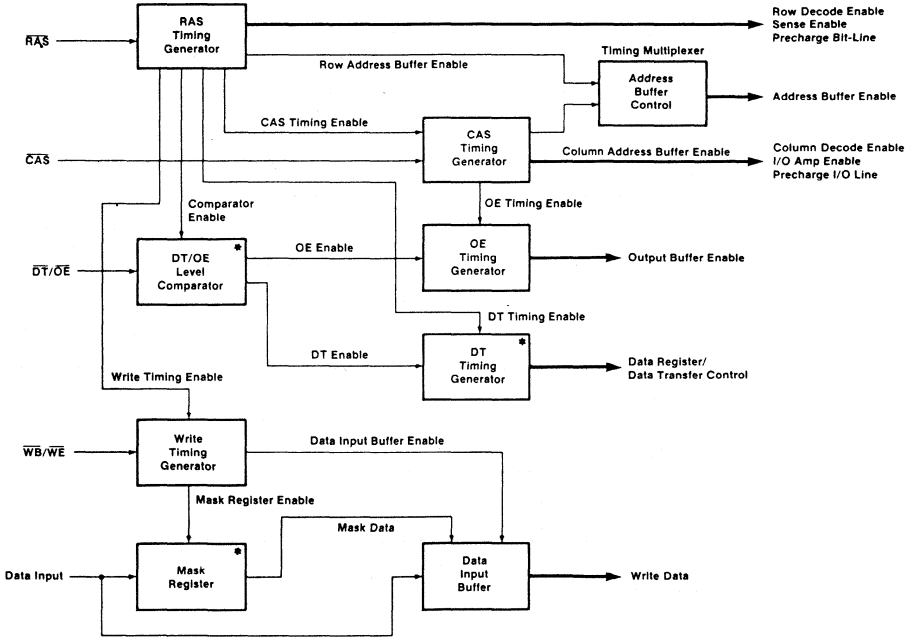
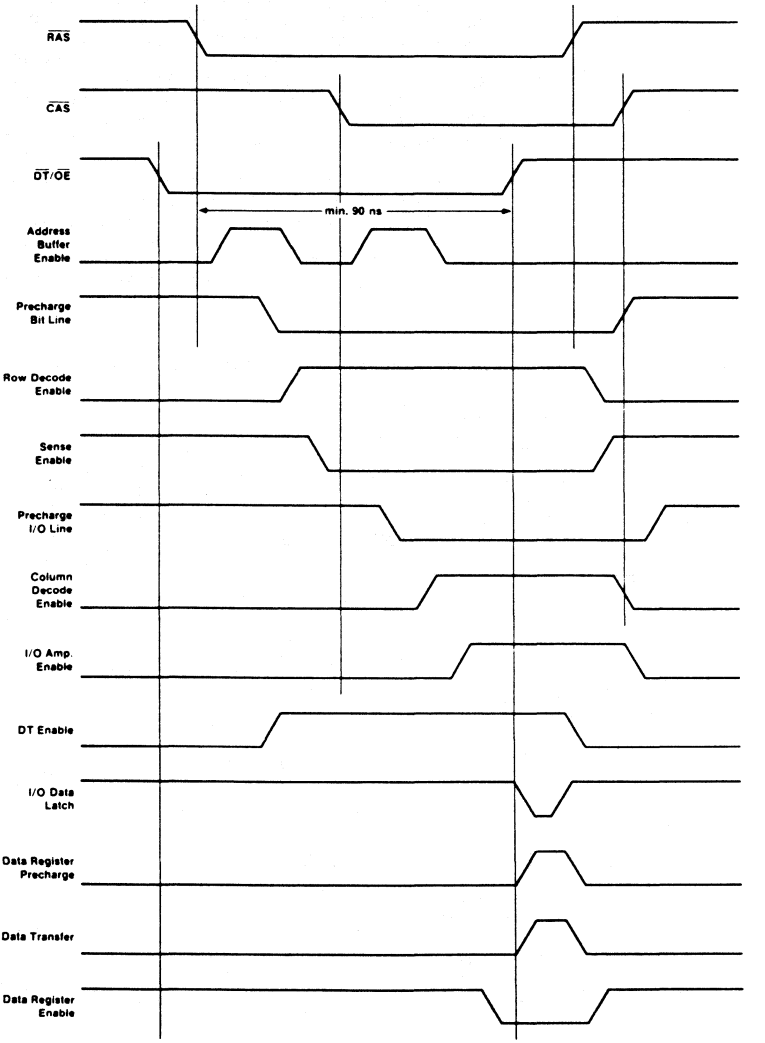


Figure 11 shows timing of the main internal signals of the internal data transfer cycle. In order to invoke the data transfer cycle, first the $\overline{DT}/\overline{OE}$ signals are kept at a low level prior to the falling $\overline{RAS}$. Also it is necessary to keep the $\overline{DT}/\overline{OE}$ signals at a low level for at least 90 ns after the falling $\overline{RAS}$.

Figure 11. Timing of the Main Signals Involved in the Internal Data Transfer Cycle



The DT/OE level comparator circuit shown in figure 10 detects that the $\overline{DT}/\overline{OE}$ signal level is low during the falling $\overline{RAS}$, and when the address buffer latches on the column address and settles its cycle action, the circuit emits the DT enable signal. Receiving this, the DT timing generator is enabled. In addition, the DT/OE level comparator controls the $\overline{OE}$ enable signals and hence turns the data output terminal of the random port into a high-impedance state. During this internal data transfer cycle, write-access to the random port becomes inhibited.

To actually transfer the data internally, the three types of internal signals that operate on the data registers are put under control (figure 9). The timing mechanism pertaining to these signals is illustrated in figure 11.

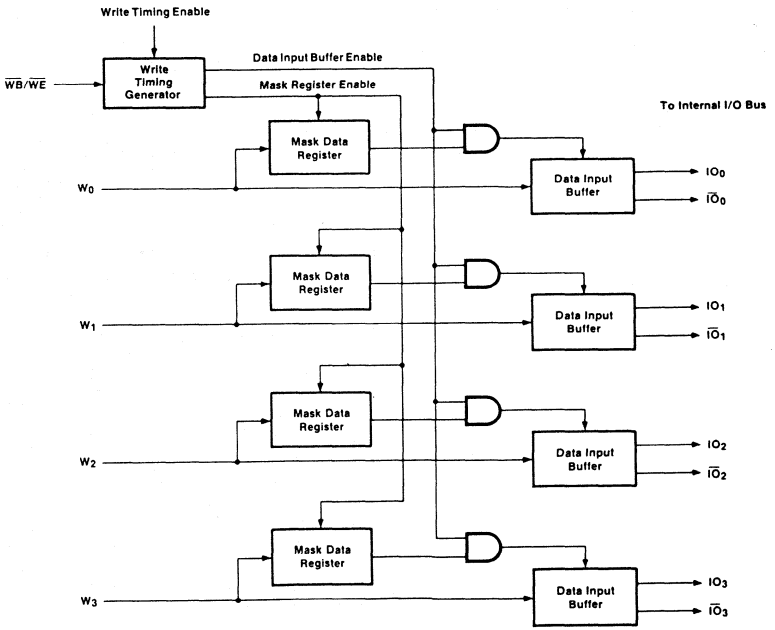
First, a little before the signal to enable the I/O bus amplifier, which amplifies the signal level of the random port's I/O bus, signals are sent to enable the data registers, leaving the data registers activated beforehand. After this, when the $\overline{DT}/\overline{OE}$ signals are started up, the data register precharge signals and the data transfer signals are generated internally. This leads to intake of data by the data registers from the bit-lines. In this manner, the internal data transfer is carried out by means of the start-up timing of the $\overline{DT}/\overline{OE}$ signals.

In the meantime, to accomplish the real-time data transfer function, it is necessary to guide the start-up data after data transfer through the bypass circuit as shown in figure 9. This is controlled by the output data latch signal, timing of which is shown in figure 11. This signal is also generated by means of the start-up timing of $\overline{DT}/\overline{OE}$. Using this signal, the start-up data are supplemented when they are sent to the I/O bus data registers shown in figure 9.

Write-per-Bit Circuit

Figure 12 shows a block diagram of the internal circuit that accomplishes the write-per-bit function. Its operational principle is a simple one. If the $\overline{WB}/\overline{WE}$ signal is at a

Figure 12. Internal Circuit of the Write-per-Bit Function



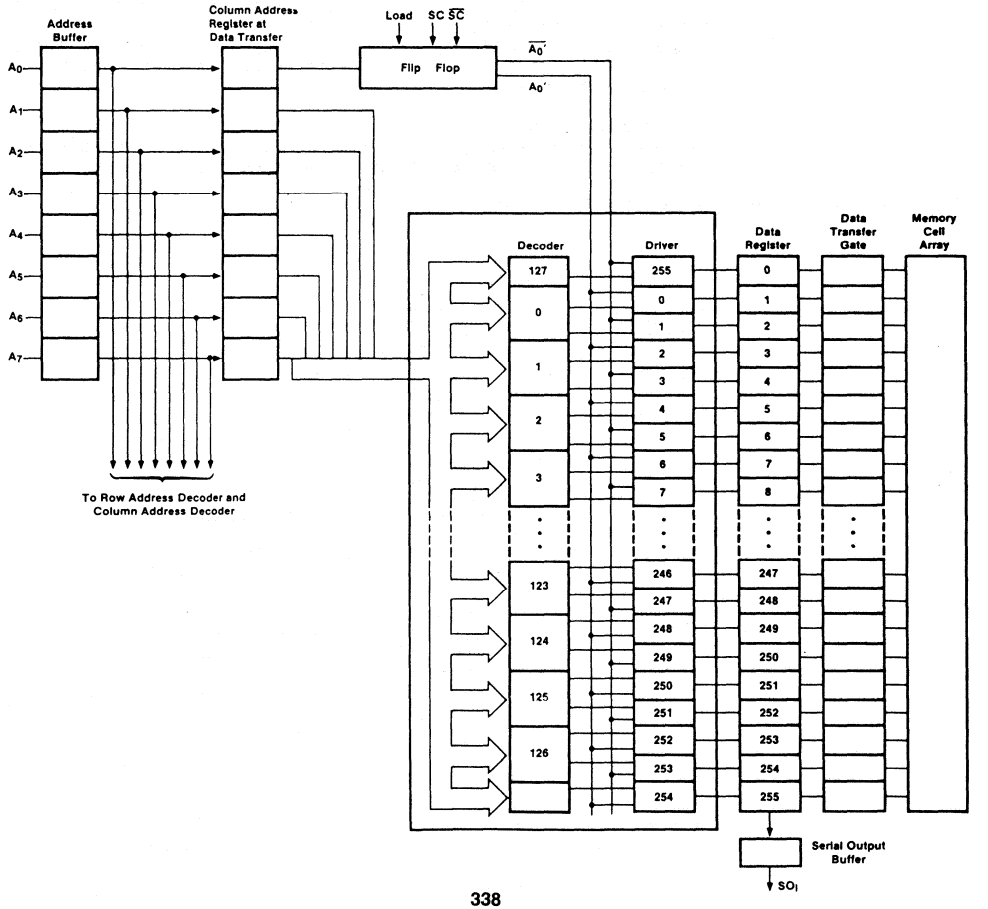
low level at the time of the $\overline{RAS}$ descent, then the mask data registers are enabled and each of them latches its input signal W_i according to its own timing. The output from each mask data register controls its own data input buffer and determines whether or not to take in the data at the next write timing.

Initially, we were not thinking about this function. We assumed that the random port should be an identical design to that of conventional RAMs and proceeded with our overall design accordingly. However, when we queried our users, domestic and abroad, they asked that a write mask capability be provided. Since then we have received strong requests saying that in graphic application fields in particular this function is a necessity. Hence, as our response we added this write-per-bit function.

Pointer Control Function

Figure 13 is a block diagram of the internal circuit that accomplishes the pointer control function. Up to now, we have explained the serialized data output in terms of a combined functioning of the counter and a selector serially selecting the contents of the data registers. Functionally, this explanation is not wrong; however, in reality it is more contrived as shown in figure 13.

Figure 13. Block Diagram of the Pointer Control Function



As a matter of fact, no counter is used. The row address is latched to the data transfer cycle and then decoded. As a result, of the 256 drivers shown in figure 13, only one is enabled and the contents of the corresponding data register are sent out to the serial output terminal. The decoder of figure 13 no longer gets involved in the subsequent serial operations. When the SC clock signal is received, the 256 drivers get serially enabled in a ring-register fashion and send out the data serially.

If a selector consists of a counter and a decoder, its power dissipation level gets high. This is because to operate the decoder at the maximum speed of 25 MHz, a static circuit must be adopted. Let us explain figure 13 somewhat more in detail. First, in the internal data transfer cycle, the row address is taken into the address register. Of the register outputs, A_1-A_7 get into the decoder, but A_0 only sets up staging the flip-flop for the next register action cycle. The two drivers are paired as a set and the output from the decoder enables only one such pair. The output of the flip-flop (A_0' and $\overline{A_0}$) further selects only one pair.

The 256 drivers in figure 13 are joined together. When the SC clock signal is input, after selecting one driver using the decoder during the data transfer cycle, the drivers at the next level become enabled in a serially cascading manner. The A_0' and $\overline{A_0}$' signals drive this mechanism.

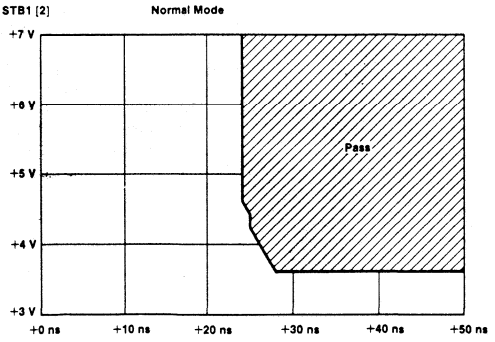
The flip-flopping output between A_0' and $\overline{A_0}$' is controlled by the toggling operation of the falling SC clock.

As seen in figure 13, the address of the drivers and those of the data registers are offset by one for each of their combinations. This is because to operate them at a high rate of speed, the action of the selector and the amplification of the serial data are pipelined. By doing it this way, it was possible to take the access time of the serial port down to 25 ns in actual measurement (see figure 14).

The contents of the data register corresponding to an enabled driver appear in the serial port. For the purpose of accomplishing the pointer control function, the row address of the data transfer is input to enable a specific driver. Each of the drivers is connected together, serially enabled by the SC signals.

As explained previously, the flip-flop action is accomplished by the falling SC signals. As shown in figure 13, the output signal of the selector (that is, the driver's output in figure 13) stays more or less constant prior to start-up of the SC signal of the next cycle. In the circuit of figure 9, in the start-up timing of the SC signal, the differential amplifier attached to a particular data register is already set up in enable state. As a result, the access time measured from the start-up timing of the SC signal includes only the operational time needed to amplify the signals from the serial output bus shown in figure 9.

Figure 14. Measured Serial Output Port Access Time (T_A = 25°C)



Going back to figure 9, let us examine the operations of the section that amplifies and outputs data from the serial output bus. For the serial bus, a transistor or balancer is used as in static RAMs. This transistor becomes on-state when the SC signal stays at a low level, hence short-circuiting the bus-lines. In order to speedily amplify new signals, the bus-lines need to be electrically charged to the same voltage beforehand. Simultaneously with the start-up of the SC signal, this transistor becomes off-state and the contents of the data register selected by the selector get amplified.

With regard to the switch to change over the readout channels, any one of the gates is "on" during the period the SC signal is at a high level. Both the SC/NM and SC/DT signals, which drive the switch, are the signals generated by the SC clock. The SC/DT signal is a signal consisting of only the SC pulse to access the beginning data after the internal data transfer. By contrast, the SC/NM signal consists of only those pulses taken from the SC clock that coincide with the SC/DT. This means that in ordinary serial cycles, the contents of the data registers are sent to the differential amplifiers in the beginning stage of the output buffer while the SC signals remain at a high level. It is only when the beginning data is accessed that the contents of the bypass channel are connected to the output terminal. In the differential amplifiers of the beginning stage of the output buffer, the $\overline{SC}$ signals, which are the inverted SC signals, are input as the enable signals. As a result, while the SC signals stay at a low level and all the changeover switches for the readout channels are "off", the previously mentioned data are kept at the output terminal.

Selector in the Pointer Control Function

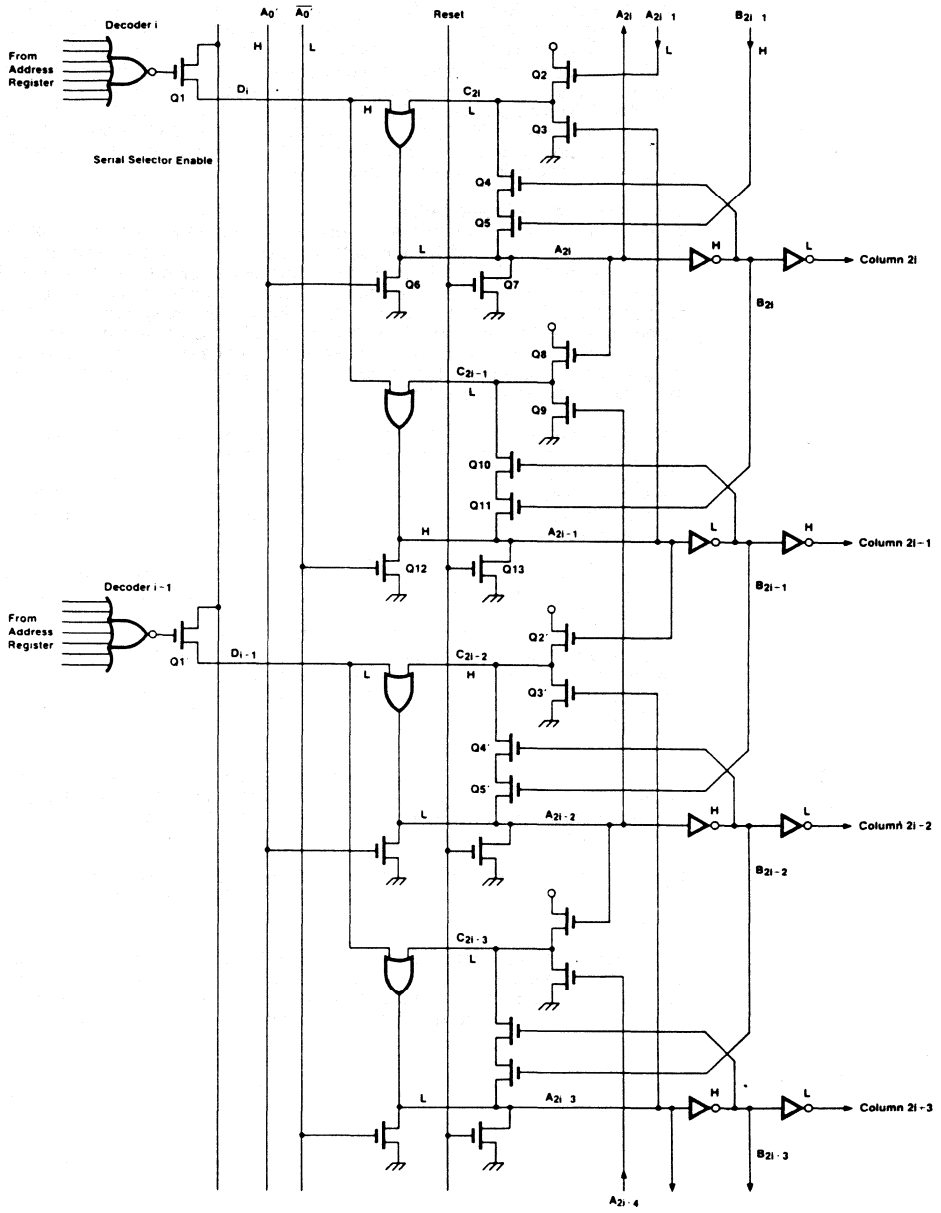
In the data transfer cycles, selector circuit of the figure 13 reads in a new row address and activates the decoder circuit. For this reason, it takes longer than an ordinary selector operation. Even so, since we adopted the previously mentioned circuit design, we could leave some margin of tolerance in the selector's operation time during this phase. Because the internal serial I/O bus is shut off the output terminal during this phase, unpredictable data cannot appear on the output terminal.

The details of the selector, consisting of decoders and drivers, are in figure 15. The figure is an excerpt showing only a portion of the 128 decoders and 256 drivers.

Let us start our explanation with operation of the internal data transfer cycle. Assume as given that the row address of this cycle causes the decoder (i) to be selected and that the least significant bit of the row address (A_0') is at a high level (H). First, when the $\overline{DT}$ signal of the data transfer cycle restores to H, a pulse with positive polarity is generated as a reset signal. As a result, Q7, Q13, etc. turn on and all the outputs are reset to a low level (L). After this, when a pulse with positive polarity is generated as the selector enabling signal, because the output from the decoder (i) is at H, node D_i is charged via Q1 and becomes H. The remaining 127 nodes will not get charged, since their corresponding decoders are at L. At this time, since A_0' is H, Q6 turns on and column 2i remains at L. In the meantime, since $\overline{A_0}$' is at L, Q12 is off and column 2i+1 becomes H.

This means that immediately after the internal data transfer, only the output from driver 2i+1 becomes H. This amounts to the same operation explained in conjunction with figure 13. In figure 15, we added the signal levels at each of the locations during this phase. In this state, node C_{2i+1} is at H. This is becuase Q2' is on whereas Q3' is off. All nodes of the other driver circuits corresponding to C_{2i+2} are at L.

Figure 15. Selector Circuit Diagram



When the next SC clock signal is input from this state, column 2i+1 becomes L and column 2i+2 in turn should become H. When the SC clock is input, the flip-flop shown in figure 13 reverses and A_0' of figure 15 becomes L and $\overline{A_0'}$ becomes H. As result, Q 12 turns on, the stray capacitane at node A_{2+1} is discharged, and column 2i+1 becomes L. In the meantime, Q5 turns off and the stray capacitance charge at node C_{2i+2} goes through the OR circuit, charging node A_{2i+2} into H level and causing column 2i+2 to become H. Similarly, when the next SC clock signal is input, column 2i+2 gets into L level, and column 2i+3 becomes H. Each time the SC clock signal is input and the flip-flop changes state, the output from the drivers changes into H in a chained series.

CPU Access to the Frame Buffer

In designing a frame buffer for graphic displays, the question of how to distribute the CPU access cycles and the data output cycles to the CRT becomes one of the keys in the system design. Typically, the conventional standard product or the single-port RAM is used. To avoid display flickers, we must resort to either the method of allowing the CPU access only during the blanking period, or the so-called cycle-stealing method. Either one of them brings about limitations in the access efficiency for the CPU. In many systems this constituted the bottleneck and the speed of refreshing the display data could not be increased. Moreover, timing their peripheral circuits would become complex.

If our dual-port memory is used, it becomes possible to allow the CPU random access while display data are being output to the CRT. And the operational efficiency of the CPU is freed from the restriction of the frame buffer(s). Not only does the system design get simplified, but also, even when the display specifications are changed, it is possible for the memory's peripheral circuits to respond to the changes more easily.

There is a broad range of applications for the dual-port memory. It can be used as a general-purpose product for frame buffers ranging from low-resolution to high-resolution displays. Let us introduce here three kinds of systems utilizing this memory. First, we will describe in detail a system with a display of 320 x 200 pixels. Next, we will introduce a section that will become the key to assembling frame buffers for a 640 x 456 pixel display using one of NEC's graphic display controllers. Finally we will describe a technique to be applied to a high-resolution display of 1280 x 1024 pixels.

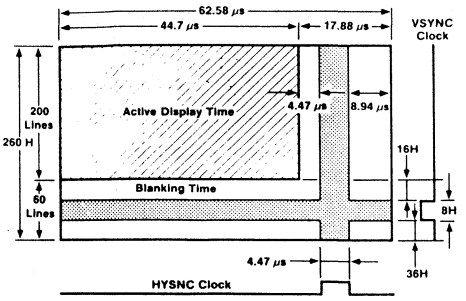
A320 x 200 Pixel Graphic Display System

Our first example is a demonstration circuit applied to a 320 x 200 pixel color graphic display system. Using the dual-port memory as the frame buffer, we created a board to directly connect to the RGB input terminal of the color display for NEC's PC-8001A personal computer.

Figure 16 shows the display specification of the PC-8001A. Since the horizontal display period is 44.7μs, in order to display 320 pixels on one scan line, the pixel rate is 139.7 ns.

In the demonstration circuit design, the frame buffer to match such a display specification called for the mapping scheme shown in figure 17. For each corresponding RGB plane, a data bus for the 8-bit based CPU was provided. This means that in one CPU cycle, 2 bits are accessed in each RGB plane.

Figure 16. Specifications of the 320 x 200 Pixel Graphic Display



Note:
[1] Horizontal display time = 44.7 μs [320 pixels]
Pixel rate = 44.7 μs/320 = 139.7 ns [7.158 MHz]
[2] Pixels in horizontal blank = 17.88 μs x 1000/139.7 ns = 128
[3] Total pixels in horizontal line = 320 + 128 = 448
[4] Pixel is derived from 2-bit P/S converter
[5] SC clock rate is one-half pixel clock rate
SC clock rate = CRTC clock rate = 3.58 MHz

For the memory capacity of the frame buffer, 320 pixels x 200 pixels x 3 planes means 24,000 bytes are required. If the real-time data transfer function of the dual-port memory is used, the frame buffer can be contained within this minimum memory capacity. However, in our current configuration, we came up with the mapping scheme shown in figure 17B. That is, we used two dual-port memories and the high-order 4 bits and low-order 4 bits of the CPU data bus were connected to the respective random ports. Then, we corresponded each horizontal scanning beam to a row of the memory. This resulted in an unused residue of memories as shown in figure 17B.

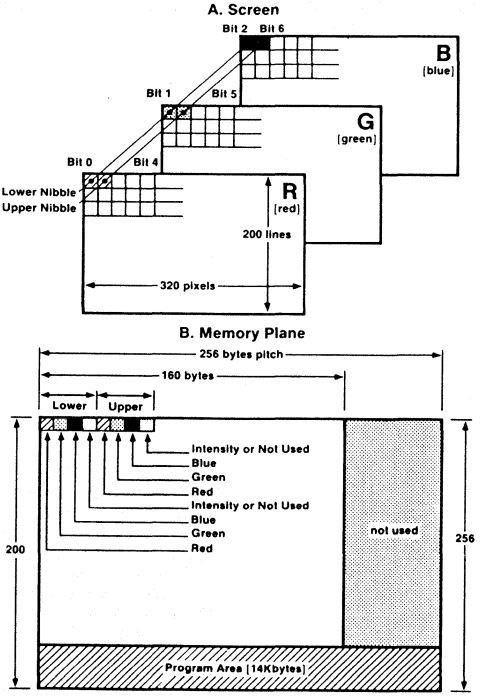
It should be noted that the main emphasis of this experimental assembly was to verify the faster refresh speed of the displayed data. For this reason, our design specification was to make the internal data transfer take place only during the horizontal blanking periods and allowed the memory usage efficiency to stay less than optimum. Nevertheless, the 14K bytes of unused memory cells (worth 56 rows) were effectively utilized as part of the program area to be used by the CPU.

Block Diagram

Figure 18 is a block diagram of the demonstration circuit. For the PC-8001A color display, the horizontal sync signal (HSYNC) and the vertical sync signal (VSYNC) are synchronized with the RGB video output signals. Without receiving any external restrictions, the CPU (Z80A) executes the program written in the PROM.

Although a CRT controller (6845) was used, it was merely a generator of the horizontal sync, vertical sync, and blanking signals. The timing generator and controller at the lower left side of figure 18 was made out of a standard TTL-type IC. The address output from the controller becomes the row address used by the dual-port memory when it internally transfers data. This address and the address sent

Figure 17. Memory Mapping Scheme



from the CPU are multiplexed and applied to the address input of the dual-port memory, which is the frame buffer. The multiplexer also performs the time-slice selection for row and column addresses.

The frame buffer in figure 17 consists of two 256K-bit dual-port memories. The setup makes it possible to connect their random-access ports directly to the data bus of the CPU. If a single-port memory were used, a cumbersome switching circuit would be needed. The output from the frame buffer goes into three 2-bit parallel-serial converter circuits, one for each of the RGB planes, and their outputs become the video signals. For refreshing the dual-port memories, the CAS-before-RAS refresh was used. This refresh is executed during a CPU's instruction fetch cycle.

From the display specification of figure 16, the PIXEL clock that operates the parallel-serial converter circuit is 7.16 MHz. From this we can determine the frequency of the SC clock, which operates the serial port of the dual-port memory, to be 3.58 MHz. The frequency of the clock used in the 6845 CRT controller is identical. However, the timing control circuit controls the SC clock in such a way that it is stopped during the blanking period. Although there is a residual moment of time left during the blanking period, between completion of internal data transfer by the dual-port memory and the beginning of the display, this is because the serial port is stopped during that time span. For the purpose of generating the foregoing clocking signals, a 14.318-MHz quartz oscillator was used. One advantage of a system using the dual-port memory is the ability to select the CPU clock independent of the display specifications. However, to keep the circuit simple, we chose the CPU clock also to be at 3.58 MHz.

Figure 18. Block Diagram of the Circuit for a 320 x 200 Pixel Graphic Display

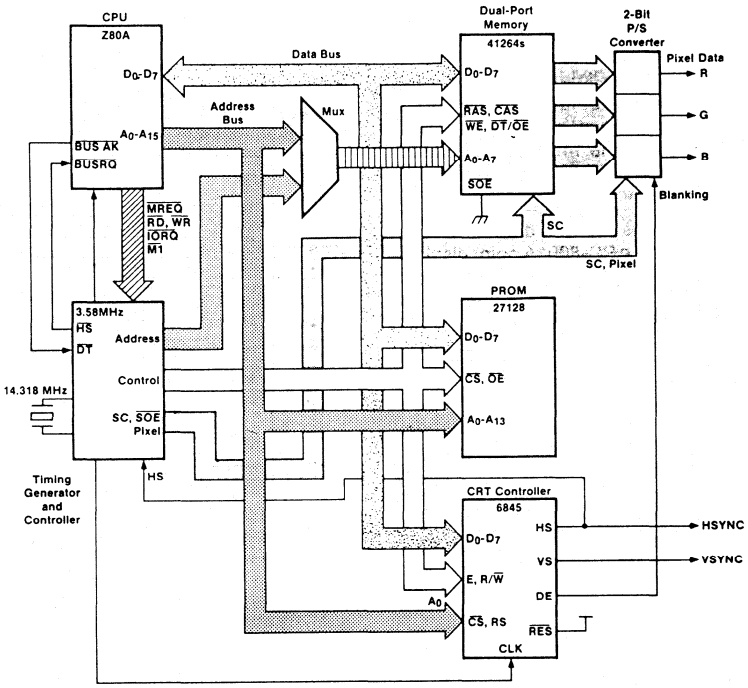
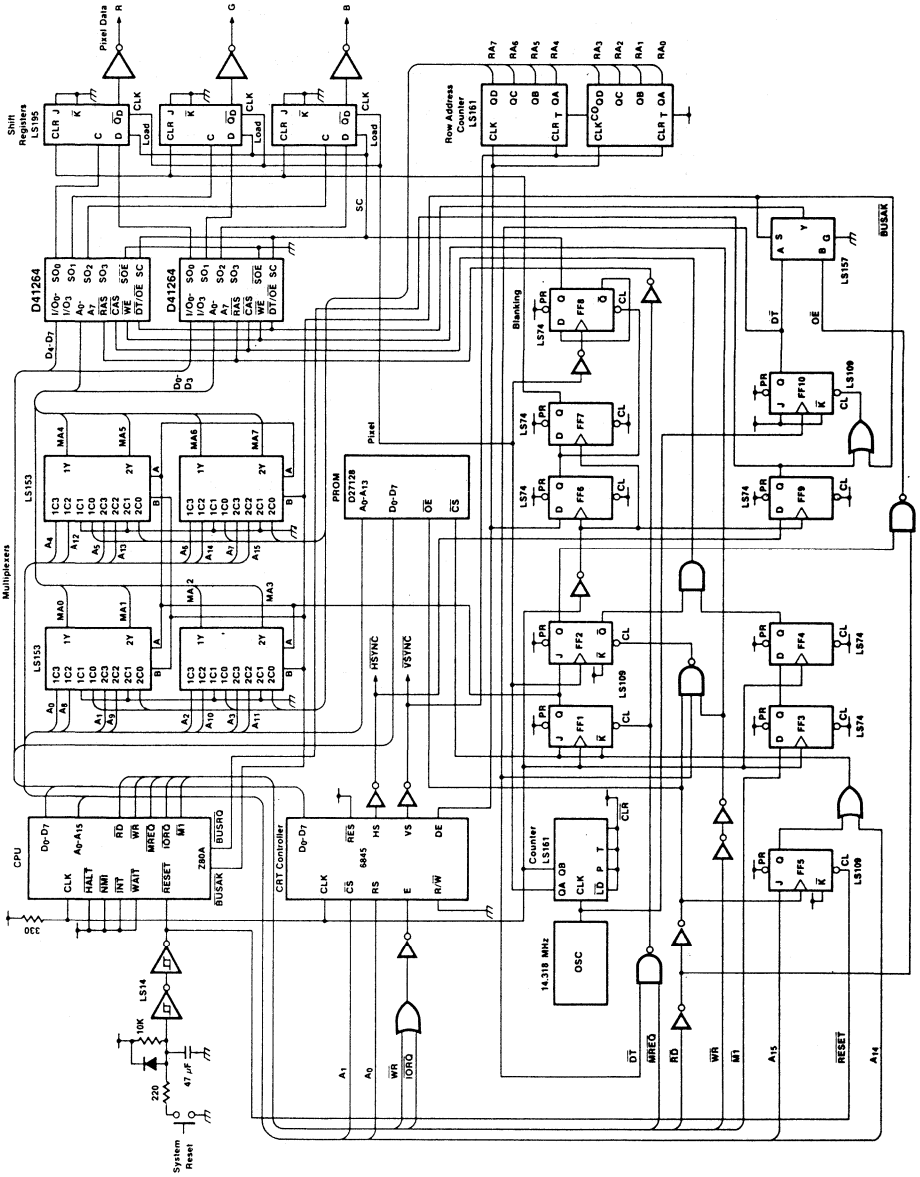


Figure 19. Connection Diagram of the 320 x 200 Pixel Graphic Display



Connection Diagram

A detailed connection diagram of our demonstration system and a photograph of its board are shown in figures 19 and 20. In addition to the CPU (Z80A), the CRT controller (6845), the PROM (27128), the two dual-port memories (41264s), the assembled unit included 25 standard TTL-type ICs. Table 3 summarizes the value setting given to the internal registers of the CRT controller. Following is a brief explanation for operation of the circuit shown in figure 19.

As can be surmised from figure 19, the timing control block of figure 18 is divided largely into four circuits: clock signal generator, DT/OE signal generator, SC clock generator, and address generation counter for data transfer.

Of these, the clock signal generator produces the clock signals needed by each of the others from a 14.318-MHz original clock oscillator. It provides 3.58-MHz clock signals to the CPU, the CRT controller, and the SC clock generator, while it outputs the 7.17-MHz PIXEL clock signals to the parallel-serial converter circuit. The $\overline{RAS}$ and $\overline{CAS}$ signals of the dual-port memory are also generated by this circuit. The $\overline{RAS}$ signal is created by adding the $\overline{MREQ}$ signal from the CPU and the $\overline{DT}$ signal from the DT/$\overline{OE}$ signal generator. To create the CAS timing of the CAS-before-RAS refresh, the $\overline{M1}$ signal from the CPU is also input. The selection signal for the multiplexer circuit to select the row and column addresses in a time-sliced fashion is also generated by means of this circuit (i.e., the A input for each multiplexer IC).

With regard to the generator circuit of the SC clock, the 3.58-MHz clock signal from the clock generator circuit is controlled so that it is kept at a low level during the blanking period, and then is sent out to the frame buffer and the parallel-serial converter circuit.

For the circuit of our discussion here, to prevent the CPU from having access to the internal data transfer cycle of the dual-port memory, we adopted a method of inputting the $\overline{BUSRQ}$ signals to the CPU prior to each cycle. The DT/OE signal generator circuit of figure 19 produces this signal.

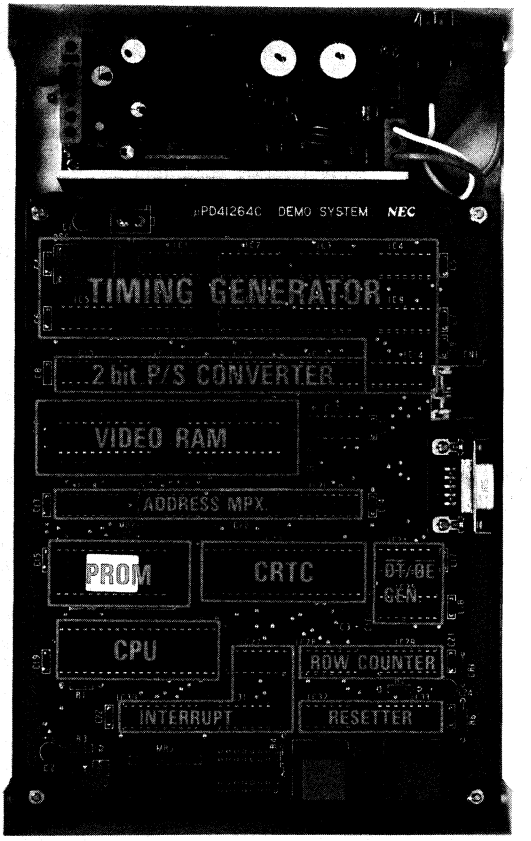
Table 3. Value Settings of CRT Controller (6845) Internal Registers

Register Number	Register Name	Setting Spec.	Set Value
R0	Number of all horizontal characters	224 characters/1H	223 = DFH
R1	Number of horizontally displayed characters	160 characters	160 = A0H
R2	Horizontally synchronous positions	180 characters	180 = 1B4H
R3	Width of horizontally synchronous pulses	15 characters	15 = 0FH
R4	Number of all vertical characters	128 rows/1V	127 = 7FH
R5	Total raster adjust horizontal characters	4 scan lines	4 = 04H
R6	Number of vertically displayed characters	100 rows	100 = 64H
R7	Vertically synchronous positions	108 rows	108 = 6CH
R8	Interlace mode	Non-interlaced	0 = 00H
R9	Maximum raster address	2 scan lines	1 = 01H
R10-R17			0 = 00H

The $\overline{BUSRQ}$ signal was produced from the HSYNC signal generated by the CRT controller. When this signal is input into the CPU, the CPU returns the $\overline{BUSAK}$ signal. The DT/OE signal generator receives this signal and generates the $\overline{DT}$ signal that controls the internal data transfer.

The $\overline{DT}$ signal and the $\overline{OE}$ signal of the CPU access cycle are switched around by the selector in the final stage, and hence the $\overline{DT}/\overline{OE}$ input signal of the dual-port memory is created.

Figure 20. Photograph of the 320 x 200 Pixel Graphic Display System Board



The row address generator counter for data transfer creates the row address for internal data transfer of the dual-port memory shown in figure 19. In this experiment, the row address of the memory was made to correspond to a horizontal scanning line of the display on a one-to-one basis and the data transfer cycle is executed during the horizontal blanking period. For this reason, the circuit of this section was simplified.

The address generator circuit for the data transfer counts the blanking signal DE, which is output from the CRT controller. The row address counters are cleared by $\overline{VSYNC}$ and their outputs sent to the multiplexer.

The multiplexer circuit of figure 19 selects the address of the dual-port memory. There are two functions involved. One is the function to select the row and column address in a time-sliced fashion. In this case, the function is controlled by an output from the clock signal generator circuit to the selection A input of the multiplexer ICs. The other function selects the CPU's address bus during ordinary CPU access cyles, but selects the transfer address during internal data transfer cycles. As we explained previously in connection with the DT/OE signal generator circuit, the $\overline{\text{BUSAK}}$ signal from the CPU controls this function via the selection B input to the multiplexer ICs. It should be noted that the multiplexer C1 inputs, which become the row address in internal data transfer cycles, are always low level in the demonstration circuit. If an output port is added to allow the CPU to control C1, it should become a simple task to accomplish the horizontal dot scrolling function.

Even with our demonstration circuit, in which we tried to keep the peripheral circuits as simple as possible, we could achieve an efficiency of 93.3 percent (figure 21A). If the real-time data transfer function is used effectively, it is possible to make the efficiency 98.28 percent (figure 21B).

If a signal as shown in figure 22 is input to the Draw- Wait terminal, the next cycle always becomes a display cycle. Even when the GDC is executing a graphic drawing cycle and updating the contents of the frame buffers, so long as such a signal is input from the outside, it is possible to force an interrupt in the access to frame buffers. Subsequently, the dual-port memory can execute the internal data transfer in the next cycle.

Figure 21. CPU Access Efficiency

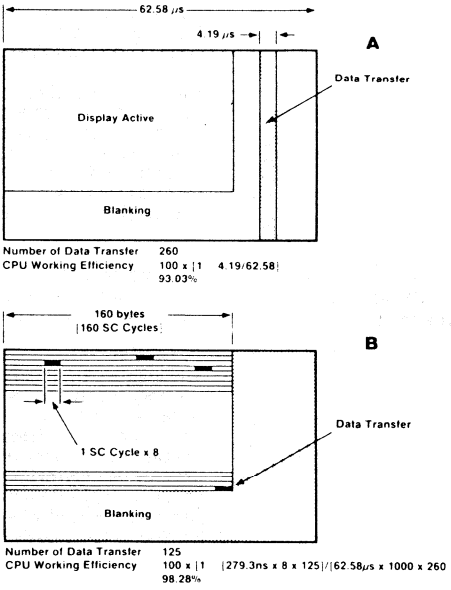
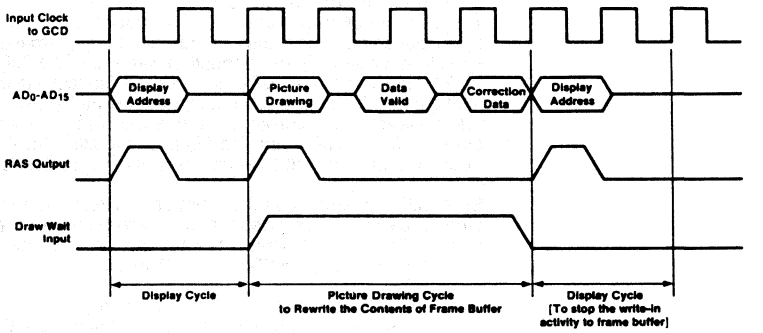


Figure 22. Draw-Wait Function Timing Diagram



Access Efficiency

Let us calculate the efficiency with which the CPU accesses the frame buffers in our demonstration circuit. As shown in figure 21A, the circuit always executes one data transfer cycle during one horizontal scanning period, including the vertical blanking period. From the figure we derive that the time ratio for the CPU to access the frame buffers is 93.30%. This value cannot be attained by means of a conventional single-port RAM.

If we can effectively use the real-time data transfer function, this value can be made even higher. As shown in figure 21B, if one row of the dual-port memory is corresponded to a display without waste, it is possible to reduce the number of data transfers for each frame to 125. If the circuit is designed so that the amount of time required for one cycle of data transfer is eight times that of the SC clock cycle, then using the calculation technique shown in figure 21B, the efficiency of the CPU access becomes 98.28%.

640 x 456 Pixel Graphic Display System

Next, we shall introduce an application example of a medium resolution system with 640 x 456 pixel display capability. For this we used an improved version of NEC's graphic display controller (GDC), μPD7220A.[14]

Draw-Wait

The improved version of the GDC was made into a product before the dual-port memory, but their development periods overlapped. For this reason, we could at least incorporate one function into the improved version of the GDC that would work in concert with the dual-port memory. This function is the Draw-Wait function. We provided a terminal (Draw-Wait) for temporarily halting externally the graphic drawing function of the GDC during its execution. In order to prevent an increase in the number of terminal ends, we piggy-backed this function with the existing light-pen input terminal. When the GDC is initialized, it is possible to decide whether this terminal is to be used for the light-pen input or the Draw-Wait input.

Referring to figure 22, when the terminal is used for the Draw-Wait input, an external signal is generated that is in sync with the GDC clock cycle and able to remain at a high level during at least four clock cycles. When the signal goes low, the GDC operates in a display cycle. This means that when the GDC executes a graphic drawing cycle and is updating the contents of the frame buffers, if an external signal is sent to the GDC (figure 22), in the next cycle the GDC halts the operation to update the frame buffers. It is possible to utilize this timing for the internal data transfer of the dual-port memory. In such an instance, it is also possible to utilize the display address output from the GDC as the pointer control address.

Flashing/Flashless Drawing Modes
Before we introduce the application example that combines the GDC and the dual-port memory, a brief explanation is in order for the graphic drawing mode of the GDC. The graphic drawing mode is divided into flashing mode and flashless mode. The flashless mode allows the graphic drawing action of the GDC only during the blanking period,whereas in the flashing mode graphic drawing can be performed even during display. Although the speed for screen display update increases in the flashing mode, in circuits using existing single-port RAMs as their frame buffers, the display is bound to incur flickering (flashing).

If the dual-port memory is used for the frame buffers, even when the GDC is in the flashing mode, there is no flickering in the display. It becomes possible to bring the drawing efficiency of the GDC close to 100 percent while keeping the display from being corrupted by flickers.

Graphic Drawing Speed
With an improved version of the GDC as the controller, and a circuit corresponding to a 640 x 456 pixel display, we examined the effect of improvements in aspects such as graphic drawing speed. The specifications of our demonstration board made it interchangeable with NEC's graphic memory board N5200 Model 05 (APC).

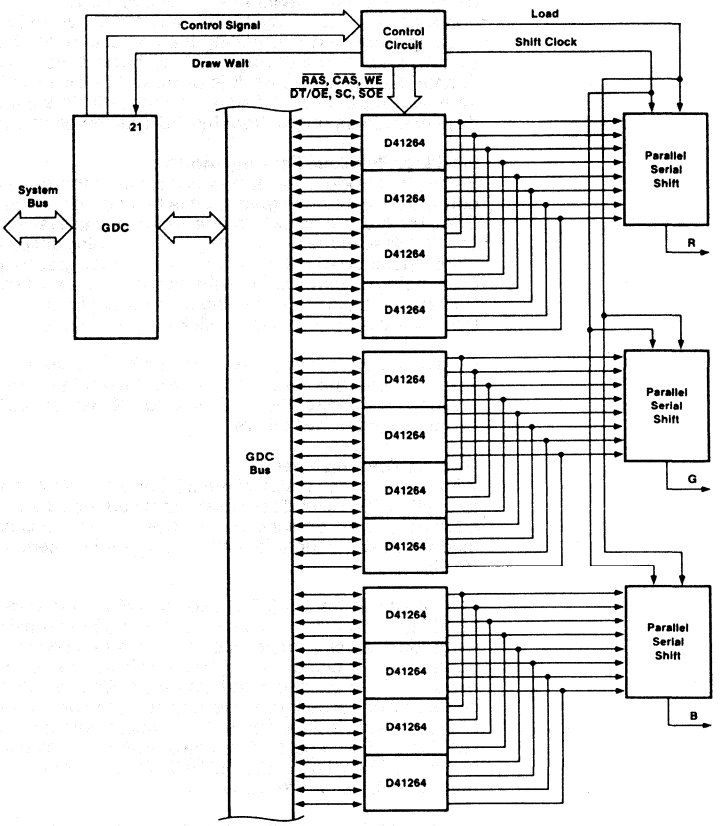
The N5200 Model 05 (APC) uses a 64K x 1-bit single-port RAM (μPD4164). By combining 16 such chips into a plane, and by internally assembling three planes, we made it possible to produce eight different colors at a time. Since the memory capacity of one plane is 1 megabit, the display area consisting of 640 x 456 pixels is extracted from the plane and displayed. When the dual-port memory is used in a configuration, its design architecture results in the diagram in figure 23. There, one plane consists of four chips. The random port can be directly connected to the GDC's bus. The serial port can be directly connected to the parallel-serial converter circuit. The $\overline{DT/OE}$, SC, and $\overline{SOE}$ signals that control the dual-port memory are generated by a control circuit.

For the parallel-to-serial converter circuits, we managed with an 8-bit circuit for each plane. This was accomplished by dividing the memory chips composing a plane into two groups, and then flip-flopping the serial output enable signal $\overline{SOE}$ as the input to each group. If four kinds of $\overline{SOE}$ signals, each offset in phase by 45 degrees were generated, it would also be possible to make the parallel-to-serial conversion circuit as a 4-bit circuit.

Since the frame buffer for each plane consists of four chips, it is possible to store 4,096 bits (256 x 4 x 4) of data in the data registers within one cycle of internal data transfer. If memory and display were matched in such a way that all data in the data registers is sent to the CRT as display data, because there are 640 horizontal pixels, internal data transfer would need to be performed at an approximate rate of once per 6.4 scanning lines.

For the purpose of externally interrupting the graphic drawing operation during the period of internal data transfer of the dual-port memory, we used the Draw-Wait function of the GDC. The GDC is an improved version and operated in flashing mode.

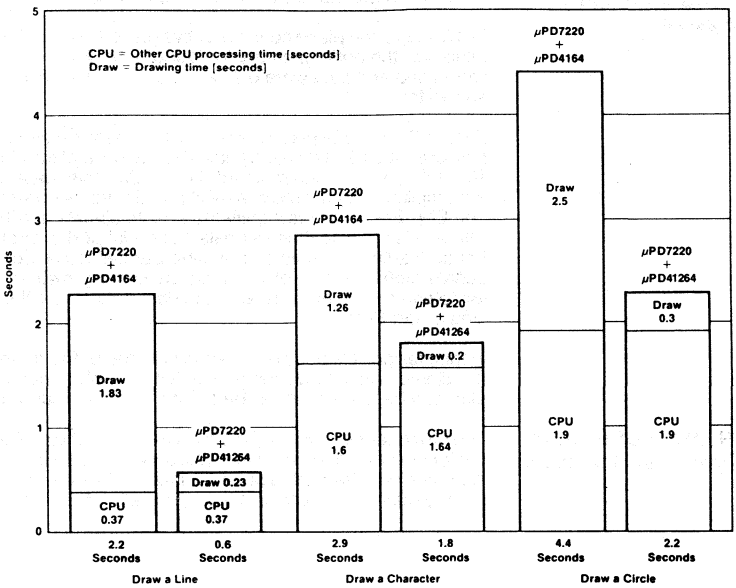
Figure 23. Block Diagram of the 640 x 256 Pixel Graphic Display



The GDC is capable of independently establishing the virtual width of the display memory and the number of display pixels during one horizontal scanning period on the basis of the number of characters. There are two different cases for our consideration. In the first case, width of the memory is made larger than the number of horizontally displayed pixels. If this is done, horizontal scrolling becomes possible only by offsetting the addresses for the memory readout. Only the parts to be displayed are sent to the CRT from the contents of the data registers while the data transfer needs to be done each time a horizontal blanking period comes around.

In the second case, the width of the memory is matched against the number of horizontal pixels. This allows all data stored in the data registers to be sent to the CRT as display data. During horizontal blanking periods, the SC clock is halted, and hence the data output is halted. Timing signals will also be generated to continue internal data transfer during the display period.

Figure 24. Comparison of Graphic Drawing Times



By connecting the demonstration board to the N5200, we examined the results of improvement. In the N5200 Model 05 (APC), we used an 8086 microprocessor as the CPU, with the operating speed set at 5 MHz. Here, the GDC was operated in the flashless mode with a 2.5-MHz clock. Since the demonstration circuit operates the GDC in flashing mode, it is possible to update the contents of the frame buffers at a speed approximately four times as fast. Moreover, we set the GDC's clock at 5 MHz. Considering all these factors, the update speed in our demonstration circuit should be approximately eight times as fast as in traditional circuits.

Figure 24 compares processing time of a system using the existing N5200 and one using our demonstration circuit. Software to display simple lines, characters, and circles is based on graphic software GSX from Digital Research Inc. As shown in figure 24, the results reduced the total amount of time to only one-half or so. But this is because the CPU processing time for other than accesses to the frame buffers is very long. If we separate graphic drawing time from other processing time, the drawing time was shortened to between 1/6 and 1/8.

1280 x 1024 Pixel Graphic Display System

Finally, as an application in high-resolution display, we introduce an example of assembling the frame buffers corresponding to 1280 x 1024 pixel displays.

In this case, one plane consists of five packets of the dual-port memory. In order to assemble the buffer memory for four planes, 20 packets of the dual-port memory were used and they were divided into five banks, from the CPU's view. Figure 25 shows this.

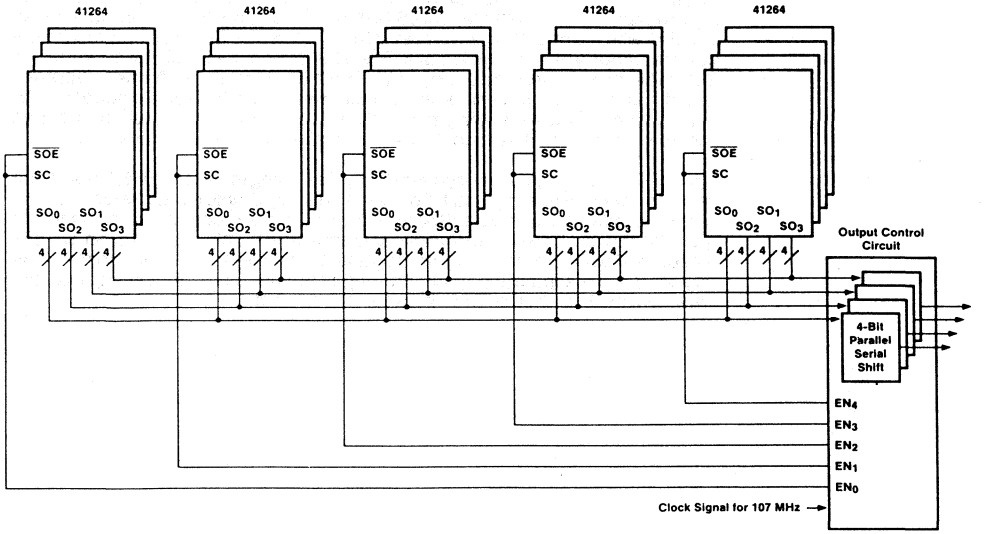
For the 1280 x 1024 pixel display, it is necessary to send the display data at a cycle time of about 9.3 ns for each pixel. This means that the clock frequency cycle will be 107 MHz. In the example of figure 25, this data output requirement was accomplished by means of a 4-bit parallel-serial converter circuit for each plane. The EN_0-EN_4 symbols signify the enable signals of a 186-ns period, each with a phase offset. Using these signals, the serial port of each bank is enabled serially, hence loading the data in the 4-bit parallel-serial converter circuits. Since the serialization cycle time of the dual-port memory is 40 ns minimum, this leaves room for tolerances of other related timings. This is not the case with the traditional single-port RAMs.

In this design, it is possible to assemble the buffer memories for four planes. The parallel-to-serial converter circuits for the high-speed output of data into the display can be accomplished by a 4-bit circuit for each plane.

Number of Product Types Will Increase

The new dual-port memory resolves almost all the problems that graphic systems designers have faced for many years. We are convinced that the three functions – real-time data transfer, pointer control, and write-per-bit – will become standard for any dual-port memory in first-generation frame buffers.[6]

Figure 25. Frame Buffer for a 1280 x 1024 Pixel Graphic Display



Since the initial announcement, we have received much feedback from users. We have requests for even newer design specifications pertaining to power consumption, packaging, new functions, and so on.

The serial port we introduced this time adopted a static circuit. There is no denying that its power consumption level is high. In order the reduce this level, it is necessary for us to investigate new circuit technologies or introduction of the CMOS process.

The package for this product is 400 mils (10.2 mm) wide, which makes it large in comparison with traditional RAMs. Some users expressed their strong desire for a 300-mil (7.6-mm) package. For this we would need to investigate ways to introduce the processing technology used in the 1-megabit dynamic RAM, which will appear in the near future as a commercial product, and to make the packing smaller. The idea of containing it within a PLCC SOJ or ZIP is also one of our subjects for future investigation.

As new functions, we can name the serial input function as the first. This makes it possible to directly input signals from TV cameras and scanners. We can also think of its applications in the communications field. We encountered a considerable number of requests stating that even without the serial input capability, a function to simply transfer additional data internally from the data registers to the memory cell array is needed. This would make it possible to clear the memory quickly. It appears in the CAD/CAM field that this function will be a required feature. It should be noted that for the purpose of merely clearing the memory quickly, there are other techniques that should also be considered. In addition, we can think of incorporating into the chip the logical and arithmetic functions for data. In the current trend in graphic processing, the so-called raster operation function appears to be becoming standard. The arithmetic function we refer to corresponds to this trend.

It is imminent that 1-megabit dynamic RAMs will be introduced as commercial products. It should be in 1985 when each firm will introduce samples. This may spur diversification in the types of memory products. Not only in x4-bit configuration, but also in x8-bit and x16-bit configurations, we will see commercialization of the dual-port memory. For the purpose of increasing the speed of random access ports, there should be attempts made to adopt static column and/or ripple modes in such products.

Acknowledgment

In acknowledgment, we would like to mention that the dual-port memory was developed by the joint efforts of many people, headed by Mr. Shoji Ishimoto. For the creation of this paper, we received advice on many occasions from them. We would like to express our deep sense of appreciation to all those who were involved.

References

[1] S. Ishimoto, A. Nagami, H. Watanabe, J. Kiyono, N. Hirakawa, Y. Okuyama, F. Hosokawa, and K. Tokushige, "A 256K Dual Port Memory," 1985 IEEE International Solid State Circuits Conference (ISSCC 85), Digest of Technical Papers, Thesis No. WAM3.1, pp. 38-39, Feb. 1985.

[2] Nagami and Hara, "A Direct I/O-type Dynamic Memory Dedicated to 320-row X 700-columns Graphic Display for the Field Memories of Televisions and VTR's," NIKKEI ELECTRONICS, Feb. 11, 1985 issue no. 362, pp. 219-239.

[3] Ishihara, Miyazawa, and Sakai, "A 256K CMOS Dynamic RAM Featuring the Static Column Mode of 50 ns Cycle time," op. cit., Feb. 11, 1985 issue no. 362, pp. 243-263.

[4] Baba, Mochizuki, and Miyasaka, "A Dynamic RAM with the Static Column Mode That Can Easily Increase the Speed of Memory Systems," op. cit., Sept. 12, 1983 issue no. 325, pp. 153-174.

[5] Saito and Shimogoshi, "Designing the Frame Buffers for a 1280X1024 Pixel Graphic Display Using 64K RAMs with the Nibble Mode," op. cit., Aug. 27, 1984 issue no. 350, pp. 227-245.

[6] Matsunaga, "The 256K Dual Port Memory Which Domestic and Overseas Manufactures Are Racing to Get Involved In," op. cit., May 20, 1985 issue no. 369, pp. 195-219.

[7] K. Guttag, "Video Controller and Dual-Port RAM Break Graphics Bottleneck," Integrated Circuits Magazine, pp. 47-54, Mar. 1985.

[8] Sussman, "Dual Port Memory Supports Bitmapped Displays," Electronic Imaging, Feb. 1985.

[9] "A Comparison of Memory Alternatives for Graphics Frame Buffer Design," AP Brief, Intel Corp., Jan. 1985.

[10] Whitten, M.C., "Memory Design for Raster Graphics Displays," IEEE Computer Graphics and Application, vol. 4, no. 3, pp. 48-65, Mar. 1984.

[11] D. Gulley, "Joining Text and Graphics Enhances Video Performance," Computer Design, vol. 23, no. 8, pp. 121-140. Aug. 1984.

[12] R. Pinkham, M. Novak, and K. Guttag, "Video RAM Excels at Fast Graphics," Electronic Design, vol. 31, no. 17, pp. 161-171, Aug. 18, 1983.

[13] Hayashi and Hagisawa, "A Dual-port 64K D-RAM with 256-bit Shift Registers for VRAM-TMS4161," INTERFACE, June 1984 issue no. 85, pp. 201-210.

[7] Oguchi, Takahashi, and Higuchi, "Manufacturing a Graphic Display Controller Using the μPD7220A," TRANSISTOR TECHNOLOGY, Feb. 1984 issue, vol. 21, no. 2, pp. 343-362.

DYNAMIC RAM MODULES

262,144 x 4-BIT DYNAMIC NMOS RAM MODULE

Description

The MC-41256A4 is a 262,144-word by 4-bit NMOS dynamic RAM module, designed to operate from a single + 5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A4 operates like four μPD41256 standard 256 K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes four μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

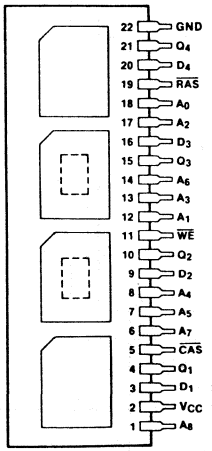
- ☐ 262,144-word by 4-bit organization
- ☐ Single + 5 V ±10 % power supply
- ☐ Standard 22-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates four 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 110 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A4-12	120 ns	220 ns	120 ns
MC-41256A4-15	150 ns	260 ns	145 ns

Pin Configuration

22-Pin SIMM, MC-41256A4A
(Glass-epoxy Substrate)



Pin Identification

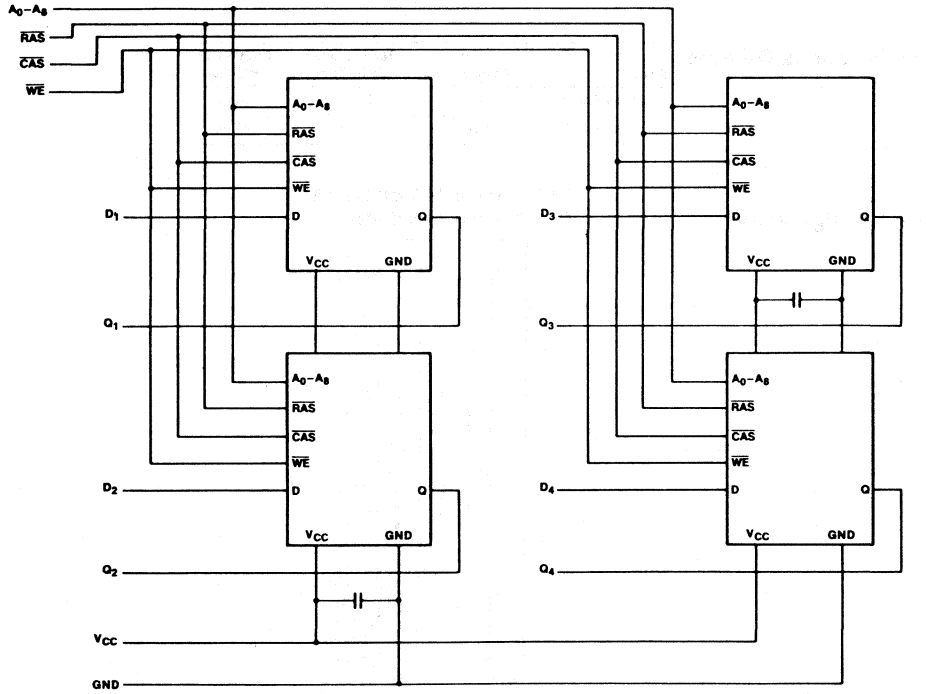
No.	Symbol	Function
1, 6-8, 12-14, 17, 18	A_0-A_8	Address inputs
2	V_{CC}	Power supply (+5.0 V)
3, 9, 16, 20	D_1-D_4	Data inputs
4, 10, 15, 21	Q_1-Q_4	Data outputs
5	$\overline{CAS}$	Column address strobe
11	$\overline{WE}$	Write enable
19	$\overline{RAS}$	Row address strobe
22	GND	Ground

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	4.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			40	pF	A_0-A_8
Input capacitance	C_{IR}			50	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			50	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			15	pF	D_1-D_4, Q_1-Q_4 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			20.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−40		40	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Data input leakage current	$I_{IL(D)}$	−10		10	μA	For D_1-D_4; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	Max	MC-41256A4-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		332		280	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Operating current, refresh mode, average	I_{CC3}		260		212	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Operating current, page mode, average	I_{CC4}		180		140	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		270		225	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	MC-41256A4-12 Max	MC-41256A4-15 Min	MC-41256A4-15 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

AC Characteristics (cont)

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

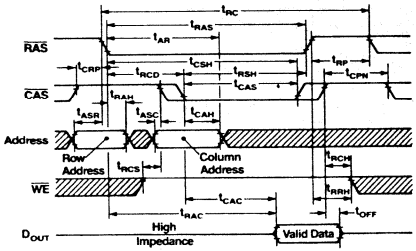
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

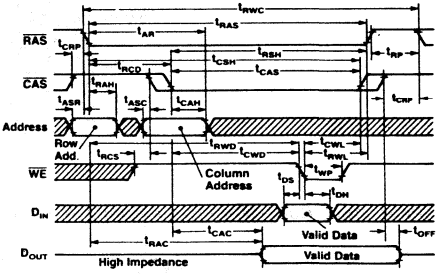
(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

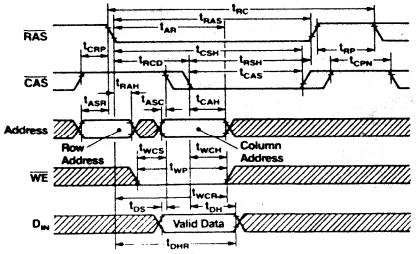
Read Cycle



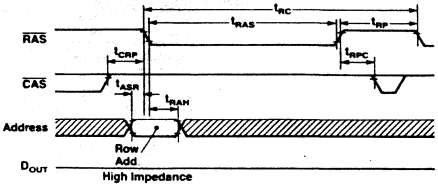
Read-Write/Read-Modify-Write Cycle



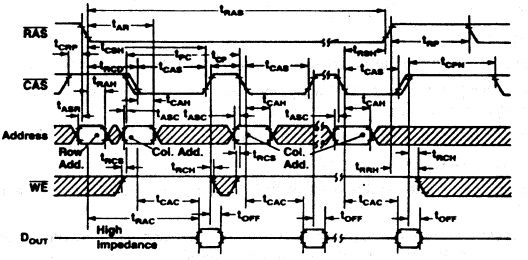
Write Cycle (Early Write)



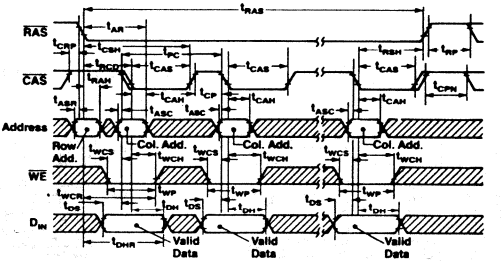
$\overline{RAS}$-Only Refresh Cycle



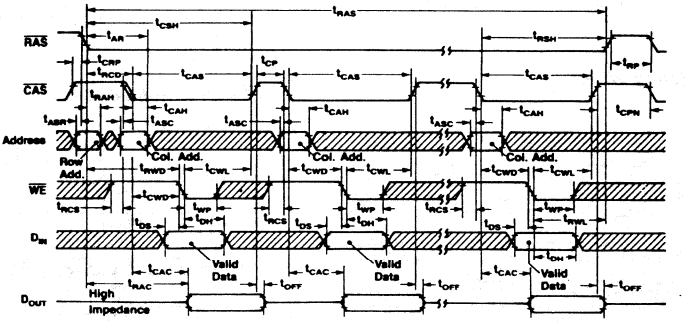
Page Mode Read Cycle



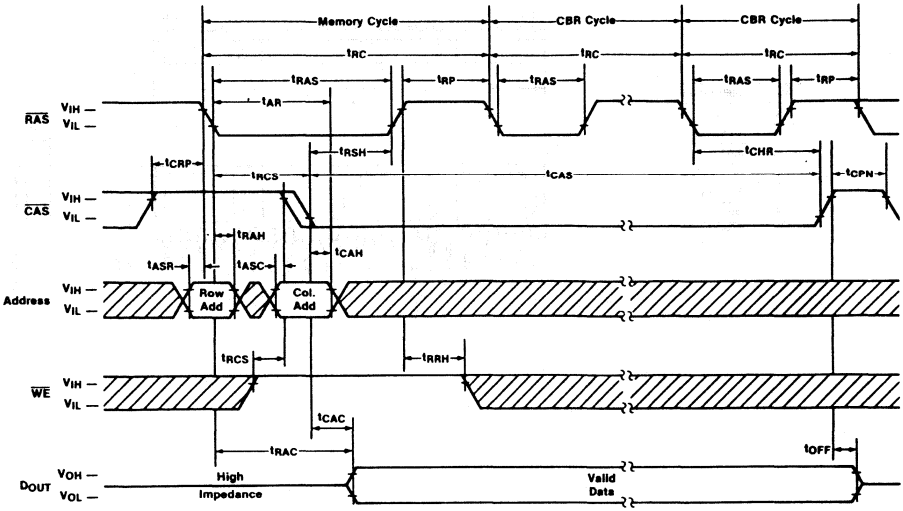
Page Mode Write Cycle (Early Write)



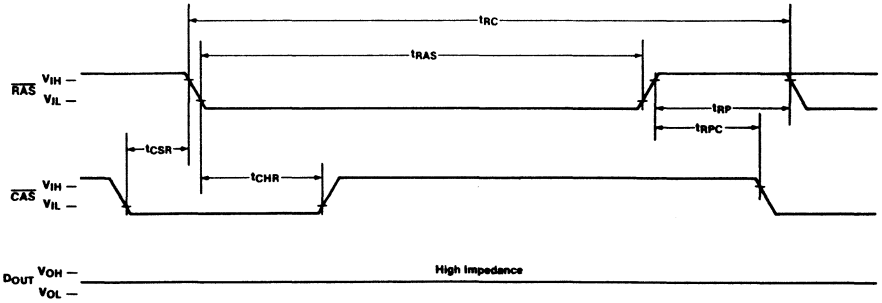
Page Mode Read-Write/Read-Modify-Write Cycle



Hidden Refresh Cycle



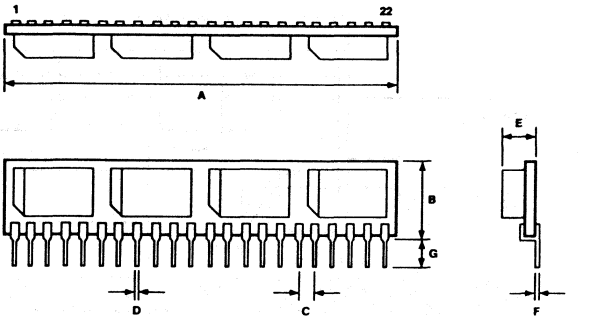
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

22-Pin SIMM, MC-41256A4A (Glass-epoxy Substrate)

Item	Millimeters
A	86.52
B	11.43 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



262,144 x 5-BIT DYNAMIC NMOS RAM MODULE

Description

The MC-41256A5 is a 262,144-word by 5-bit NMOS dynamic RAM module, designed to operate from a single + 5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A5 operates like five μPD41256 standard 256 K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes five μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

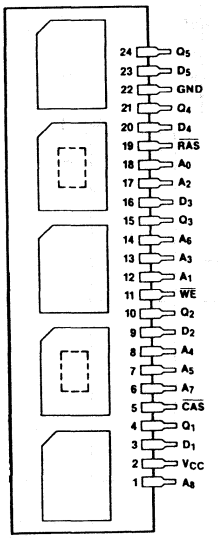
- ☐ 262,144-word by 5-bit organization
- ☐ Single + 5 V ±10 % power supply
- ☐ Standard 24-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates five 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 138 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A5-12	120 ns	220 ns	120 ns
MC-41256A5-15	150 ns	260 ns	145 ns

Pin Configuration

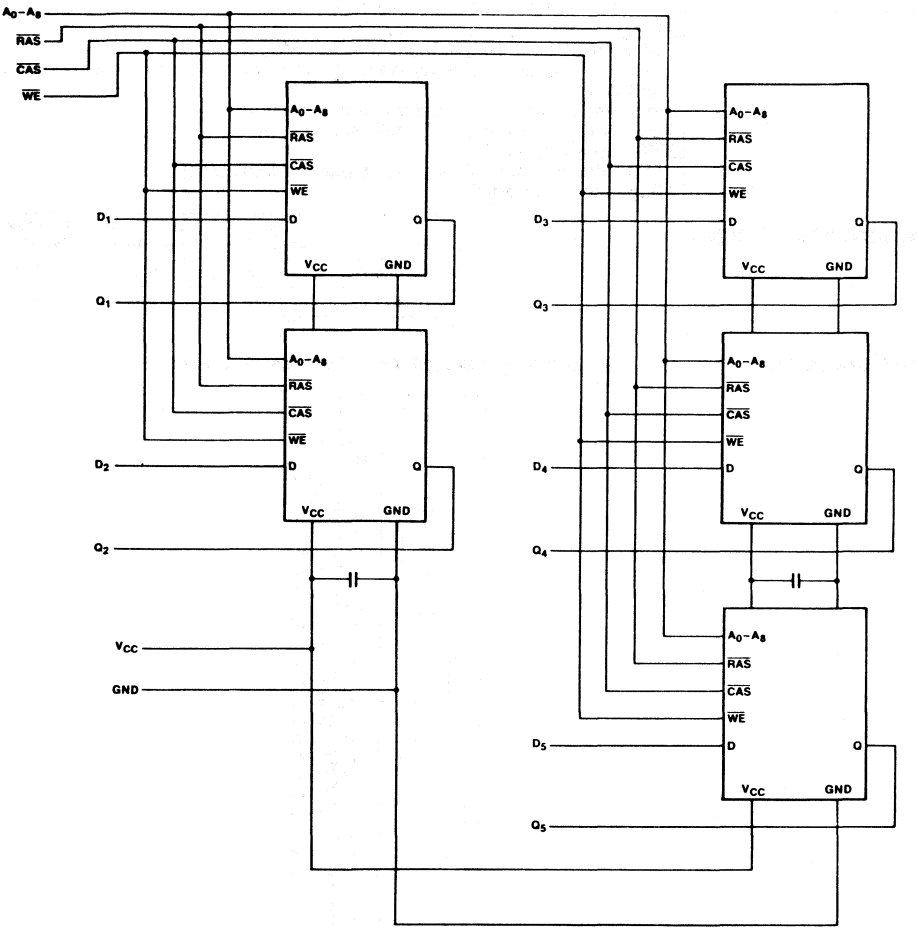
24-Pin SIMM, MC-41256A5A (Glass-epoxy Substrate)



Pin Identification

No.	Symbol	Function
1, 6-8, 12-14, 17, 18	A_0-A_8	Address inputs
2	V_{CC}	Power supply (+5.0 V)
3, 9, 16, 20, 23	D_1-D_5	Data inputs
4, 10, 15, 21, 24	Q_1-Q_5	Data outputs
5	$\overline{CAS}$	Column address strobe
11	$\overline{WE}$	Write enable
19	$\overline{RAS}$	Row address strobe
22	GND	Ground

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	5.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			45	pF	A_0-A_8
Input capacitance	C_{IR}			55	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			55	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			15	pF	D_1-D_5, Q_1-Q_5 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			25.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−50		50	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Data input leakage current	$I_{IL(D)}$	−10		10	μA	For D_1-D_5; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A5-12 Min	MC-41256A5-12 Max	MC-41256A5-15 Min	MC-41256A5-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		415		350	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		325		265	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		225		175	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		340		280	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A5-12 Min	MC-41256A5-12 Max	MC-41256A5-15 Min	MC-41256A5-15 Max	Unit	Test Conditions
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

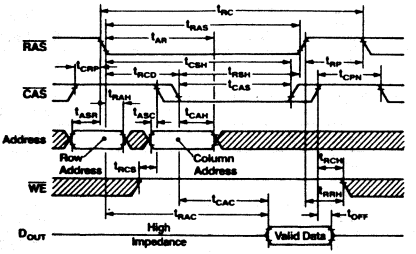
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

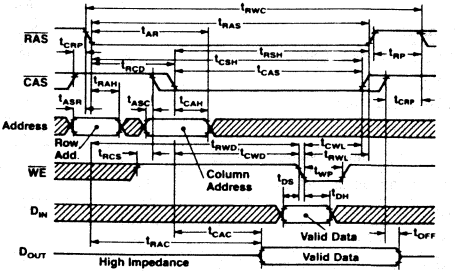
(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

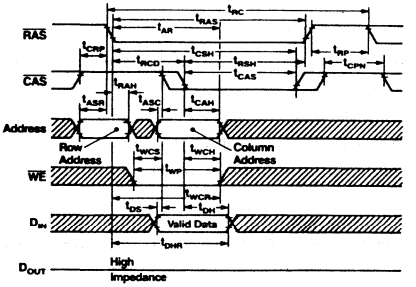
Read Cycle



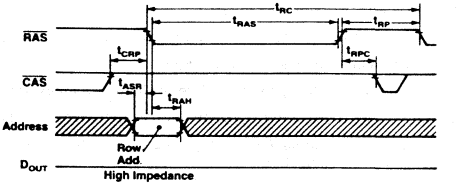
Read-Write/Read-Modify-Write Cycle



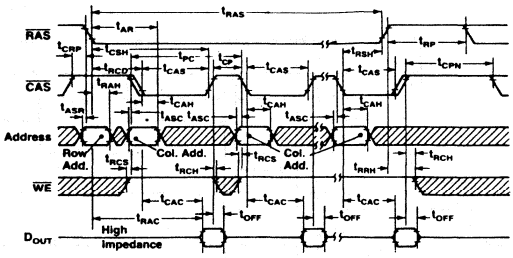
Write Cycle (Early Write)



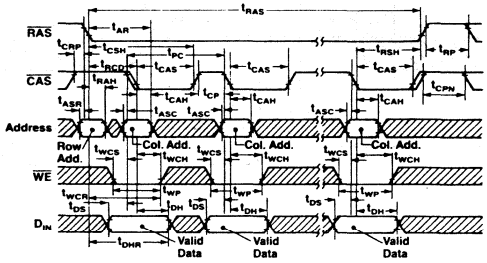
RAS-Only Refresh Cycle



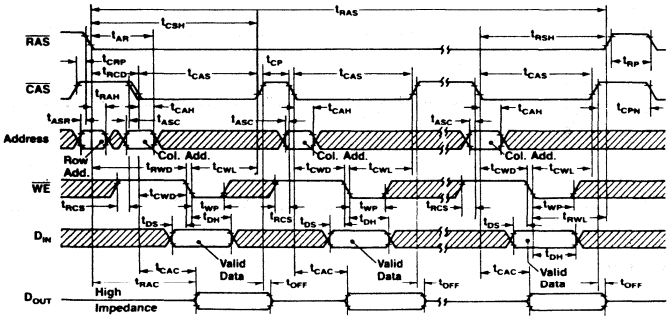
Page Mode Read Cycle



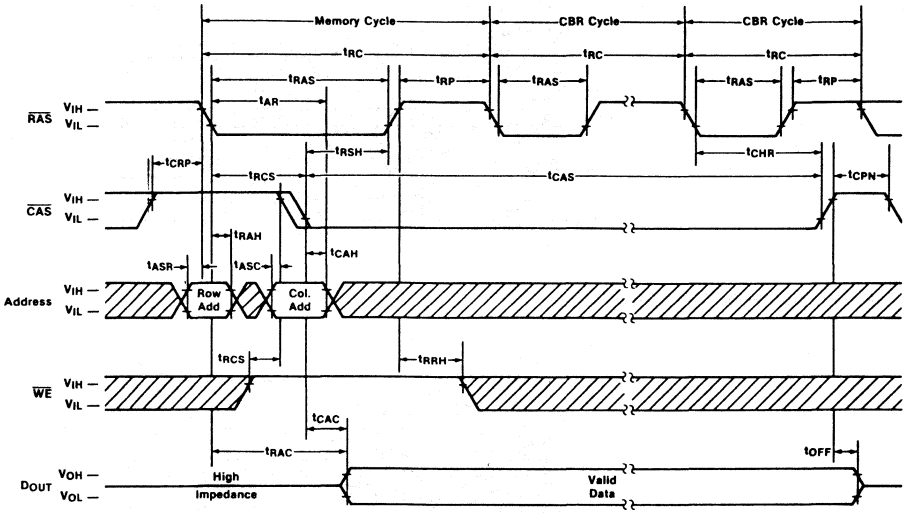
Page Mode Write Cycle (Early Write)



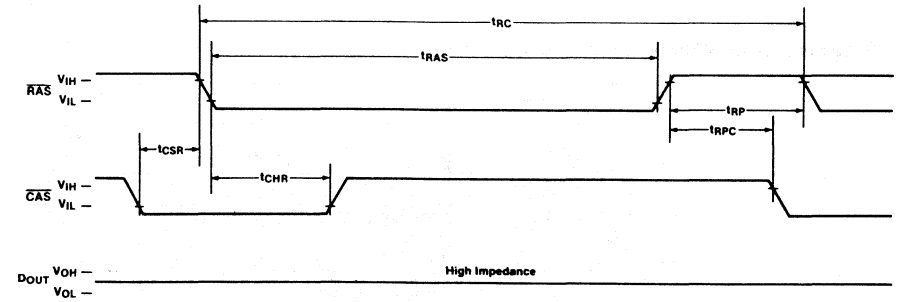
Page Mode Read-Write/Read-Modify-Write Cycle



Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

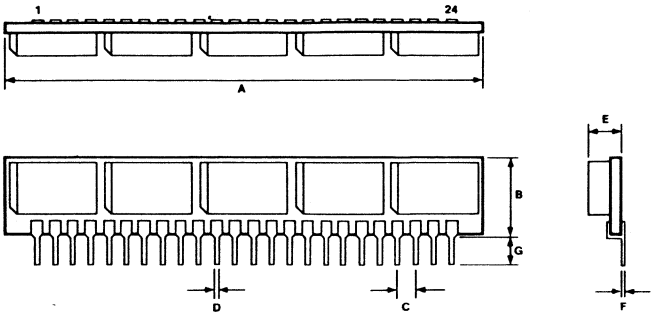


Note:
[1] $\overline{WE}$, Address: Don't Care.

Packaging Information

24-Pin SIMM, MC-41256A5A (Glass-epoxy Substrate)

Item	Millimeters
A	68.60
B	11.40 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



262,144 x 8-BIT DYNAMIC NMOS MODULE

Description

The MC-41256A8 is a 262,144-word by 8-bit NMOS dynamic RAM module, designed to operate from a single + 5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A8 operates like eight μPD41256 standard 256 K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes eight μPD41256s in PLCC packages and eight power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

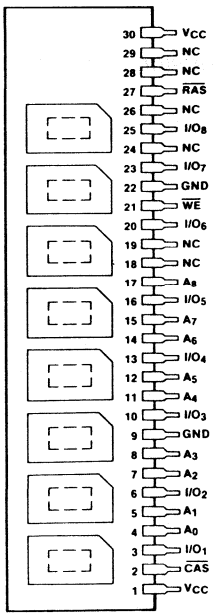
- ☐ 262,144-word by 8-bit organization
- ☐ Single + 5 V ±10 % power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates eight 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 220 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A8-12	120 ns	220 ns	120 ns
MC-41256A8-15	150 ns	260 ns	145 ns

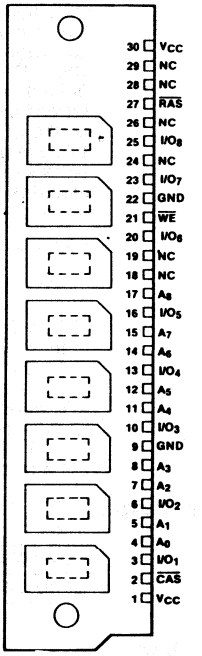
Pin Configuration

30-Pin SIMM, MC-41256A8A



Pin Configurations (cont)

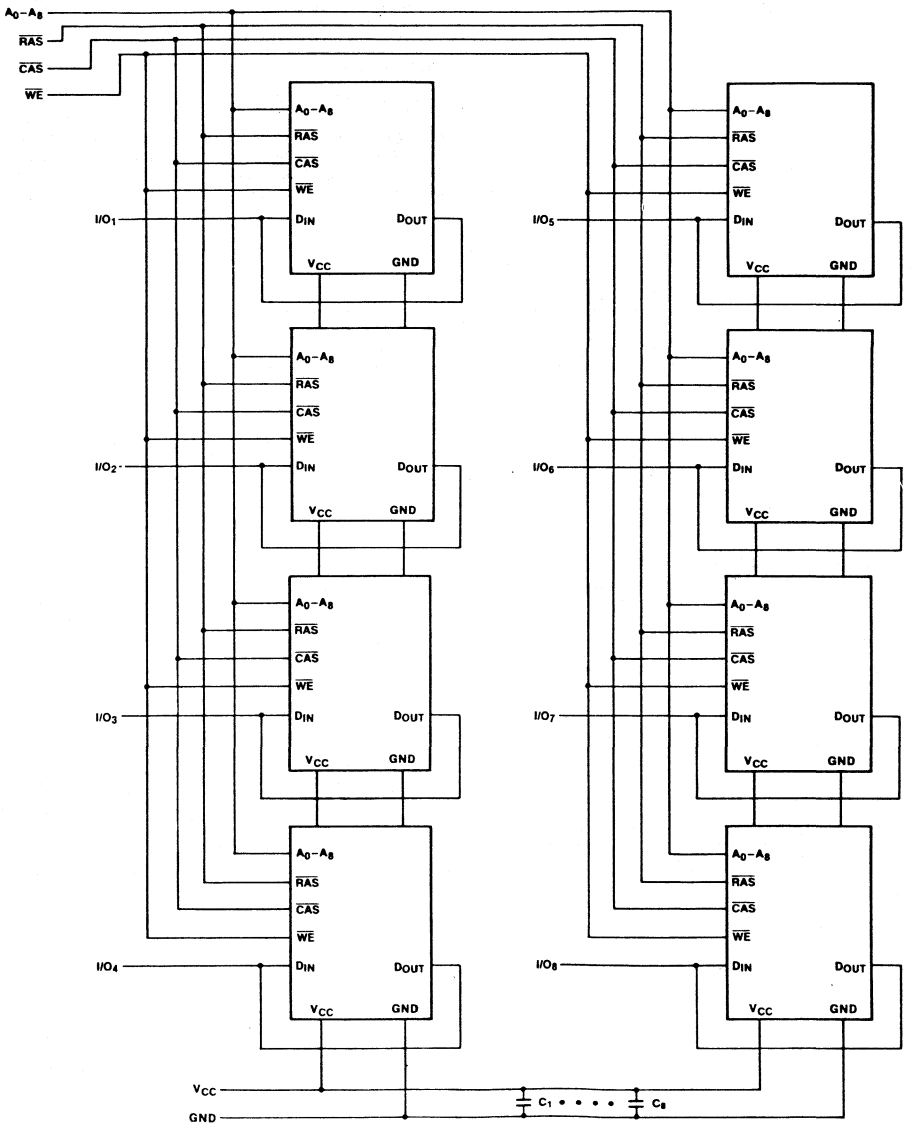
30-Pin SIMM. MC-41256A8B



Pin Identification

No.	Symbol	Function
1, 30	V_{CC}	Power supply (+5.0 V)
2	$\overline{CAS}$	Column address strobe
3, 6, 10, 13 16, 20, 23, 35	I/O_1-I/O_8	Common data inputs/outputs
4, 5, 7, 8, 11, 12, 14, 15, 17	A_0-A_8	Address inputs
9, 22	GND	Ground
18, 19, 24, 26 28, 29	NC	No connection
21	$\overline{WE}$	Write enable
27	$\overline{RAS}$	Row address strobe

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			55	pF	A_0-A_8
Input capacitance	C_{IR}			70	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			70	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			17	pF	I/O_1-I/O_8 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			40.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−80		80	μA	V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−20		20	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A8-12 Min	MC-41256A8-12 Max	MC-41256A8-15 Min	MC-41256A8-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		664		560	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Operating current, refresh mode, average	I_{CC3}		520		425	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Operating current, page mode, average	I_{CC4}		360		280	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		545		450	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A8-12 Min	MC-41256A8-12 Max	MC-41256A8-15 Min	MC-41256A8-15 Max	Unit	Test Conditions
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 15)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 15)

Note:

(1) All voltages referenced to GND

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

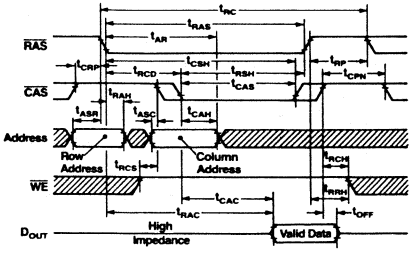
(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

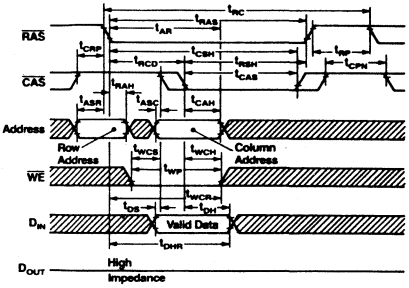
(14) These parameters are referenced to the leading edge of $\overline{CAS}$.

(15) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

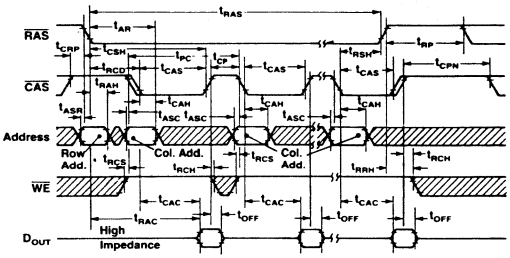
Read Cycle



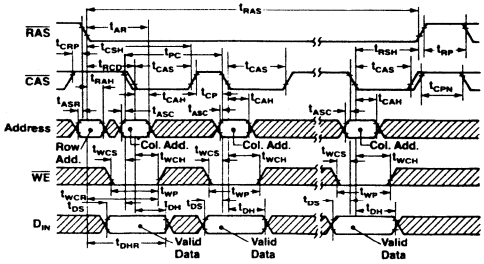
Write Cycle (Early Write)



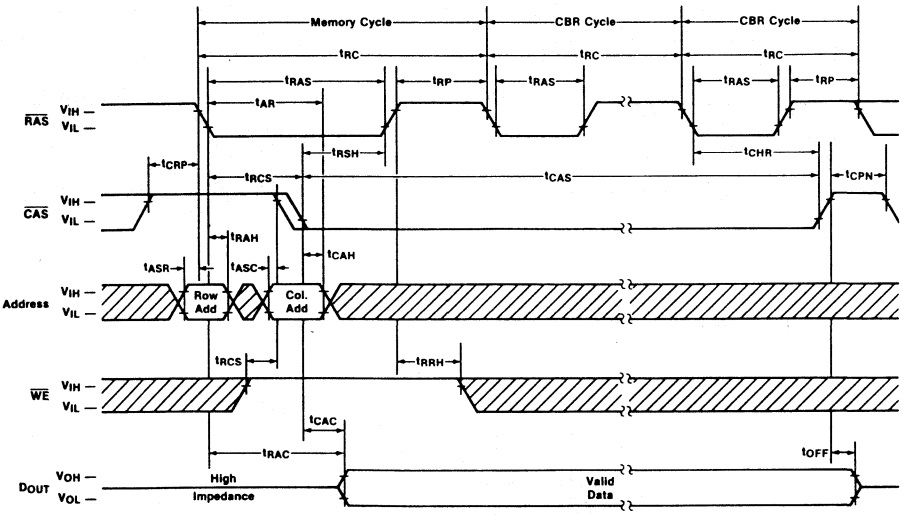
Page Mode Read Cycle



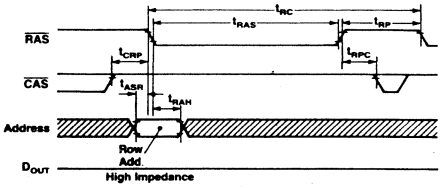
Page Mode Write Cycle (Early Write)



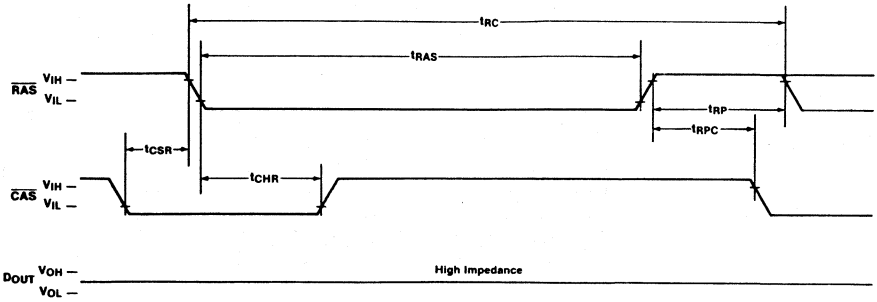
Hidden Refresh Cycle



RAS-Only Refresh Cycle



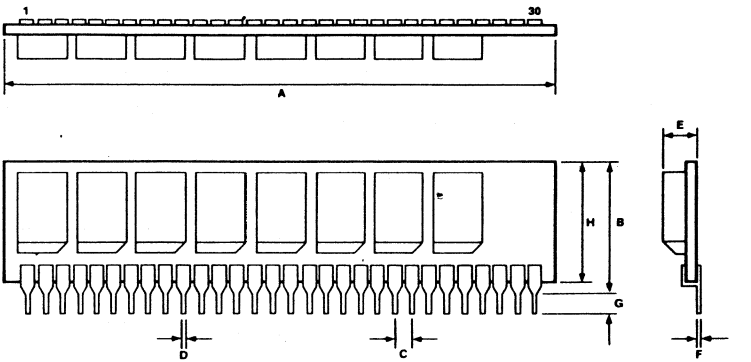
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

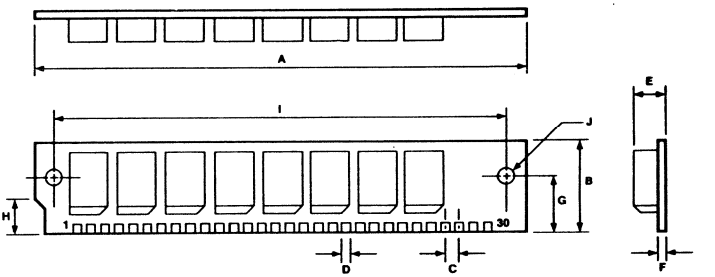
30-Pin SIMM, MC-41256A8A (Glass-epoxy Substrate)

Item	Millimeters
A	78.90
B	18.00 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00
H	16.76



30-Pin SIMM, MC-41256A8B (Glass-epoxy Substrate)

Item	Millimeters
A	88.90
B	16.90 max
C	2.54
D	1.78
E	5.08 max
F	1.27 ± .08
G	10.16
H	6.35
I	82.10
J	3.175 dia



262, 144 x 9-BIT DYNAMIC NMOS RAM MODULE

Description

The MC-41256A9 is a 262,144-word by 9-bit NMOS dynamic RAM module, designed to operate from a single + 5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A9 operates like eight μPD41256 standard 256 K DRAMs with a parity bit. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes nine μPD41256s in PLCC packages and nine power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

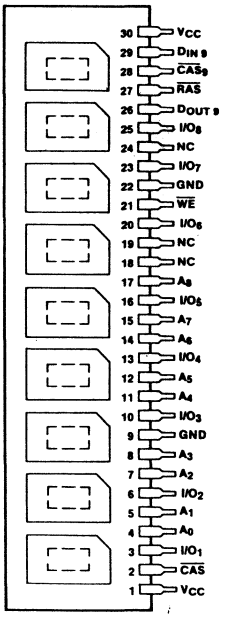
- ☐ 262,144-word by 9-bit organization
- ☐ Single + 5 V ±10 % power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates nine 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 248 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A9-12	120 ns	220 ns	120 ns
MC-41256A9-15	150 ns	260 ns	145 ns

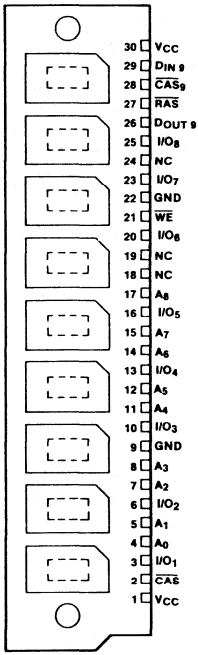
Pin Configurations

30-Pin SIMM, MC-41256A9A



Pin Configurations (cont)

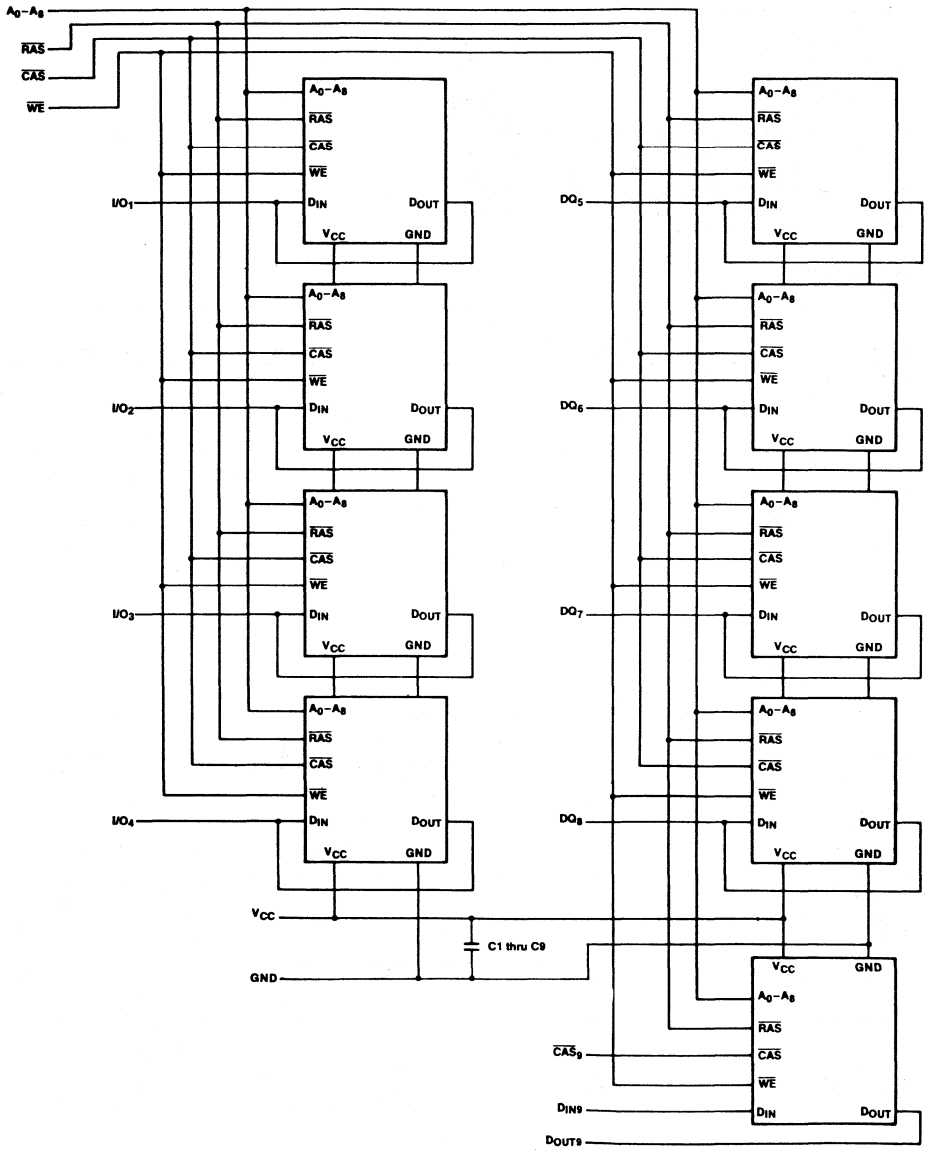
30-Pin SIMM, MC-41256A9B



Pin Identification

No.	Symbol	Function
1, 30	V_{CC}	Power supply (+5.0 V)
2	$\overline{CAS}$	Column address strobe
3, 6, 10, 13, 16, 20, 23, 25	I/O_1-I/O_8	Common data inputs/outputs
4, 5, 7, 8, 11, 12, 14, 15, 17	A_0-A_8	Address inputs
9, 22	GND	Ground
18, 19, 24	NC	No connection
21	$\overline{WE}$	Write enable
26	$D_{OUT\ 9}$	Data output 9
27	$\overline{RAS}$	Row address strobe
28	$\overline{CAS}_9$	Column address strobe for data output 9
29	$D_{IN\ 9}$	Data input 9

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70 °C
Storage temperature, T_{STG}	−55 to +85 °C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70 °C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			60	pF	A_0-A_8
Input capacitance	C_{IR}			75	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			70	pF	$\overline{CAS}$
Input capacitance	$C_{IC\,9}$			13	pF	$\overline{CAS}_9$
Input capacitance	$C_{IN\,9}$			17	pF	$D_{IN\,9}$
Input/output capacitance	C_{IO}			17	pF	I/O_1-I/O_8 (Note 1)
Output capacitance	$C_{OUT\,9}$			12	pF	$D_{OUT\,9}$ (Note 2)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

(2) $\overline{CAS}_9$ = V_{IH} to disable $D_{OUT\,9}$

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			45.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−90		90	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current	$I_{IL\,9}$	−10		10	μA	For $\overline{CAS}_9$, $D_{IN\,9}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−20		20	μA	For I/O_1-I/O_8; D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output leakage current	$I_{OL\,9}$	−10		10	μA	For $D_{OUT\,9}$; $D_{OUT\,9}$ disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	MC-41256A9-12 Min	MC-41256A9-12 Max	MC-41256A9-15 Min	MC-41256A9-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		747		630	mA	$\overline{RAS}$, $\overline{CAS}$,cycling, t_{RC} = t_{RC} min (Note 5)
Operating current, refresh mode, average	I_{CC3}		585		475	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Operating current, page mode, average	I_{CC4}		405		315	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		610		505	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Notes 6, 17)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A9-12 Min	MC-41256A9-12 Max	MC-41256A9-15 Min	MC-41256A9-15 Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15, 17)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15, 17)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15, 17)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

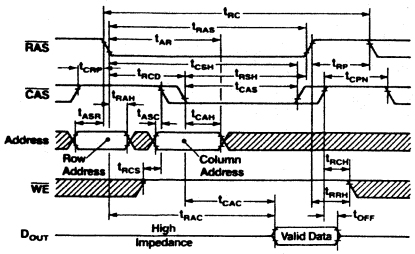
(15) For $D_{OUT\,9}$, t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

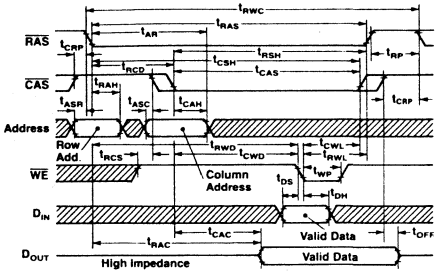
(17) Read-write/read-modify-write operation can be performed only by the PLCC controlled by $\overline{CAS}_9$ because of its separate data input and output terminals.

Timing Waveforms

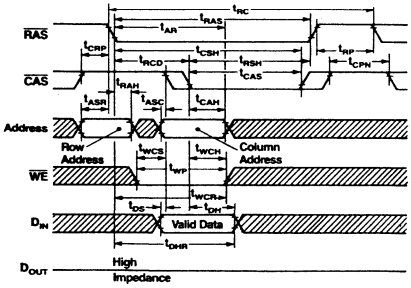
Read Cycle



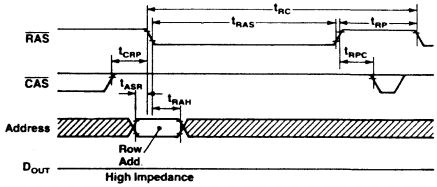
Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



Write Cycle (Early Write)

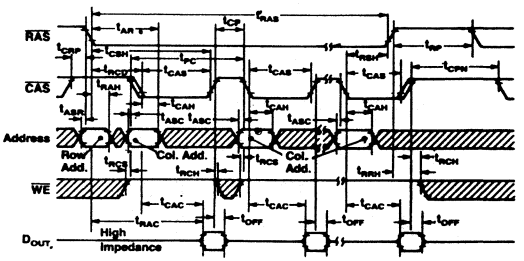


RAS-Only Refresh Cycle

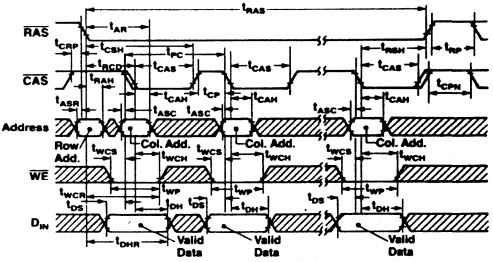


Timing Waveforms (cont)

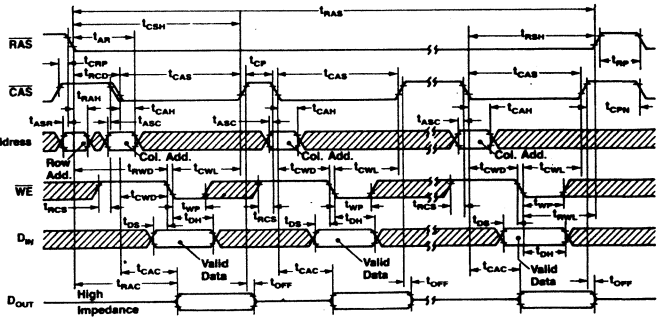
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

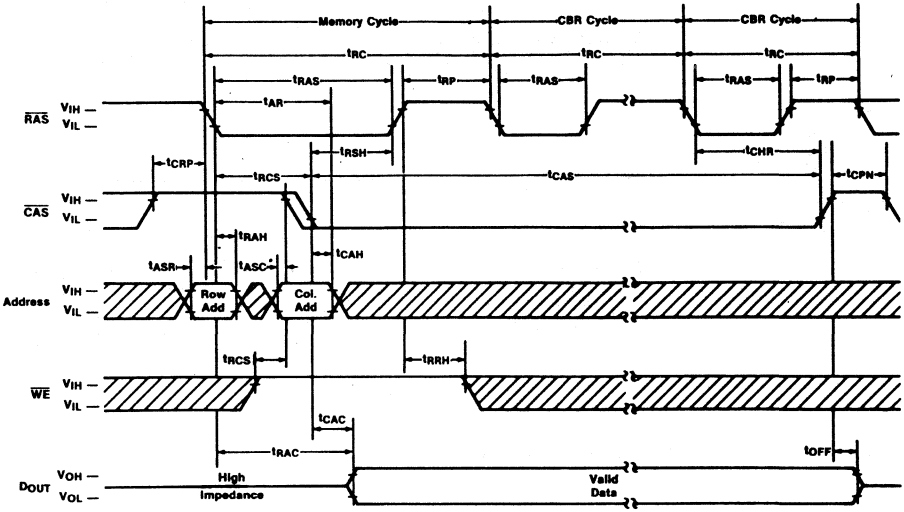


Page Mode Read-Write/Read-Modify-Write Cycle (D_{OUT} only)

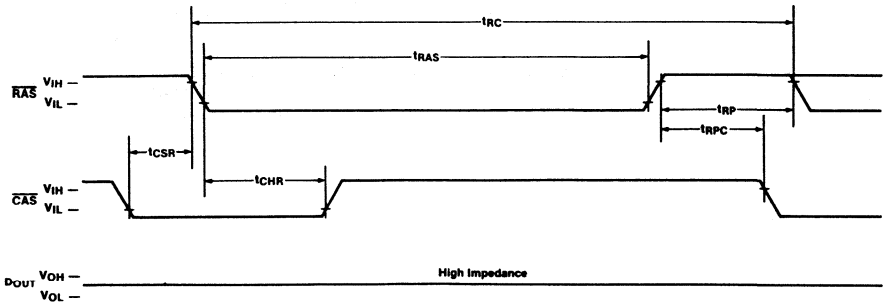


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

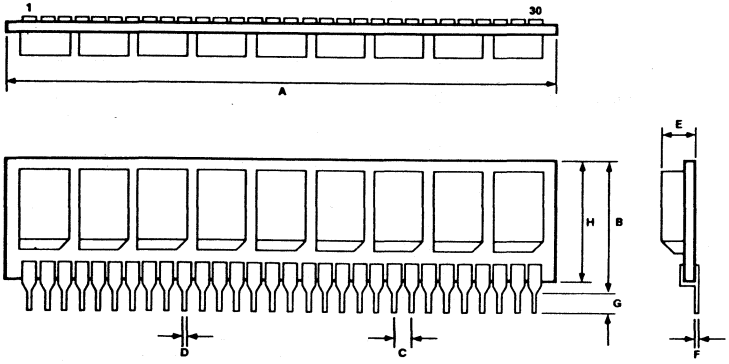


Note:
[1] $\overline{WE}$, Address: Don't Care.

Packaging Information

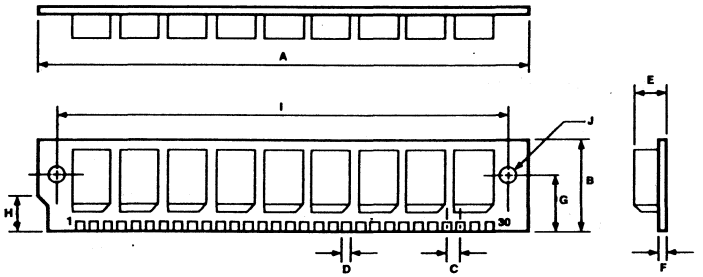
30-Pin SIMM, MC-41256A9A (Glass-epoxy Substrate)

Item	Millimeters
A	78.90
B	18.00 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00
H	16.76



30-Pin SIMM, MC-41256A9B (Glass-epoxy Substrate)

Item	Millimeters
A	88.90
B	16.80 max
C	2.54
D	1.78
E	5.08 max
F	1.27 ± .08
G	10.16
H	6.35
I	82.10
J	3.175 dia



Description

The MC-411000A1 is a 1,048,576-word by 1-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, sense amplifiers, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

Separate data input and data output pins from four μPD41256s are controlled by individual $\overline{RAS}$ pins and common $\overline{CAS}$ and $\overline{WE}$. Data pins are connected in parallel to provide single input and single output terminals. Refresh is accomplished on each of the four μPD41256s by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes four μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

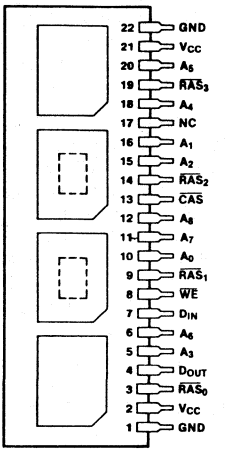
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 22-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates four 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 110 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	*Page Mode Cycle Time
MC-411000A1-12	120 ns	220 ns	120 ns
MC-411000A1-15	150 ns	260 ns	145 ns

Pin Configuration

22-Pin SIMM, MC-411000A1A



Pin Identification

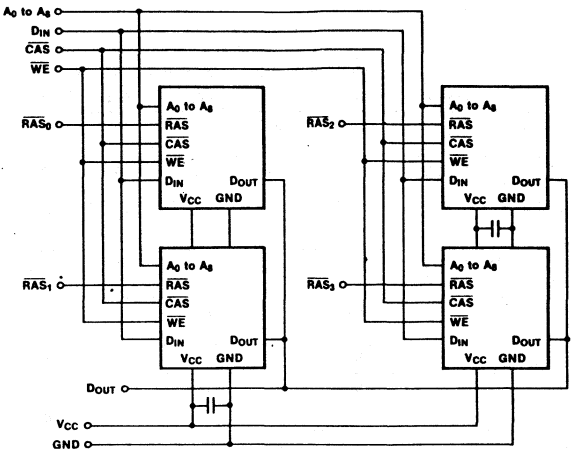
No.	Symbol	Function
1, 22	GND	Ground
2, 21	V_{CC}	Power supply (+5.0 V)
3, 9, 14, 19	$\overline{RAS}_0$-$\overline{RAS}_3$	Row address strobes
4	D_{OUT}	Data output
5, 6, 10-12, 15, 16, 18, 20	A_0-A_8	Address inputs
7	D_{IN}	Data input
8	$\overline{WE}$	Write enable
13	$\overline{CAS}$	Column address strobe
17	NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70 °C
Storage temperature, T_{STG}	−55 to +85 °C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IA}			40	pF	A_0-A_8, D_{IN}
Input capacitance	C_{IR}			15	pF	$\overline{RAS}_0$-$\overline{RAS}_3$
Input capacitance	C_{IW}			50	pF	$\overline{WE}$
Input capacitance	C_{IC}			50	pF	$\overline{CAS}$
Output capacitance	C_{OUT}			50	pF	D_{OUT} (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			20.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−40		40	μA	For A_0-A_8, D_{IN}, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current, $\overline{RAS}$ input	$I_{IL\ (RAS)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; untested $\overline{RAS}$ pins = V_{IH}; other pins = 0 V
Output leakage current	I_{OL}	−40		40	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-411000A1-12 Min	Limits MC-411000A1-12 Max	Limits MC-411000A1-15 Min	Limits MC-411000A1-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		98		85	mA	One $\overline{RAS}$ input and $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, refresh mode, average	I_{CC3}		80		68	mA	One $\overline{RAS}$ input cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, page mode, average	I_{CC4}		60		50	mA	One $\overline{RAS}$ input = V_{IL}, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		83		71	mA	One $\overline{RAS}$ input cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-411000A1-12 Min	Limits MC-411000A1-12 Max	Limits MC-411000A1-15 Min	Limits MC-411000A1-15 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles on each $\overline{RAS}$ input before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

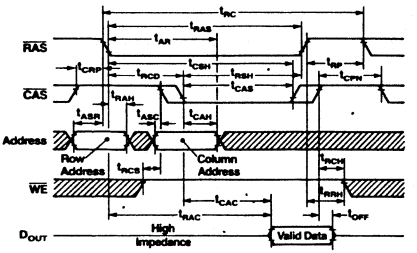
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

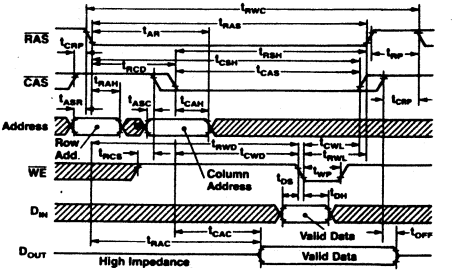
(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified. Refresh operations can be performed on all four μPD41256Ls simultaneously by the use of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles or $\overline{RAS}$-only refresh cycles. All other operations require that only one of the $\overline{RAS}_0$-$\overline{RAS}_3$ inputs is in the active state.

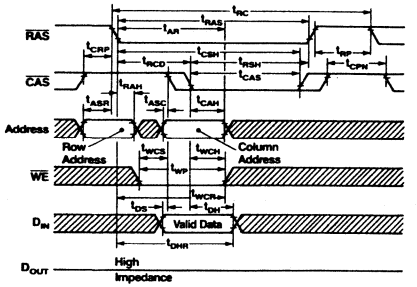
Read Cycle



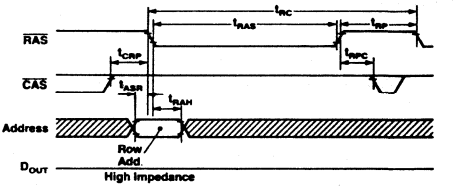
Read-Write/Read-Modify-Write Cycle



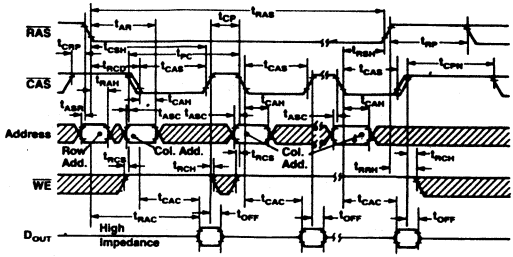
Write Cycle (Early Write)



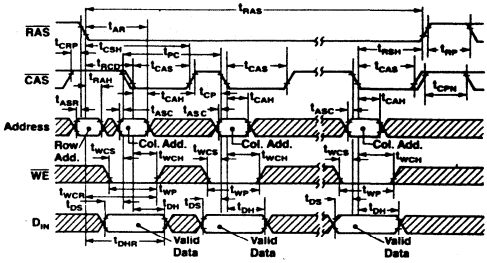
RAS-Only Refresh Cycle



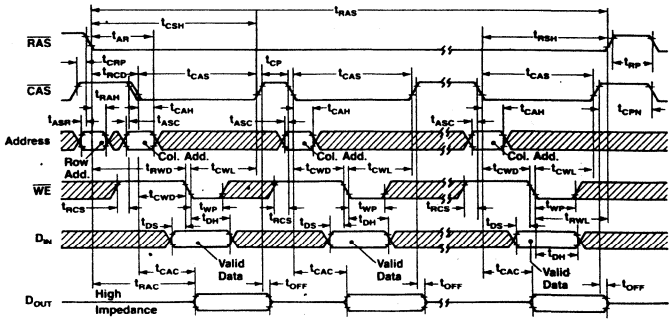
Page Mode Read Cycle



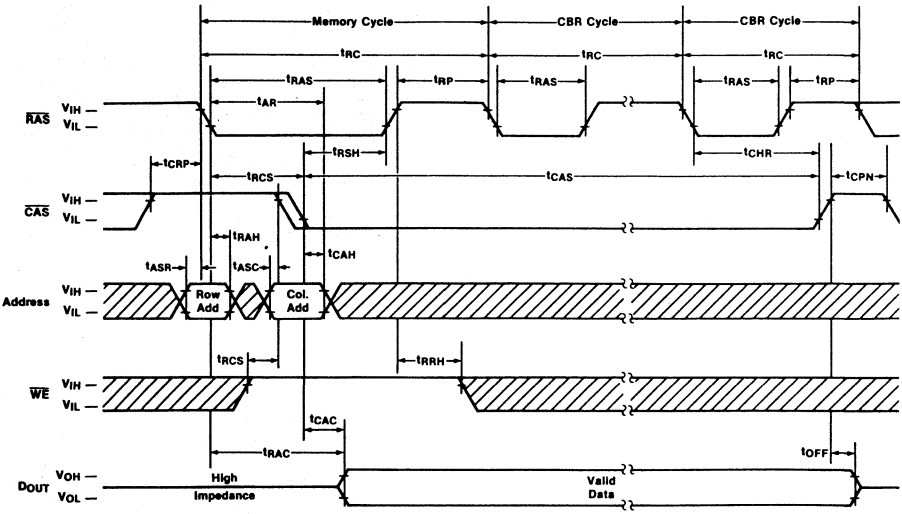
Page Mode Write Cycle (Early Write)



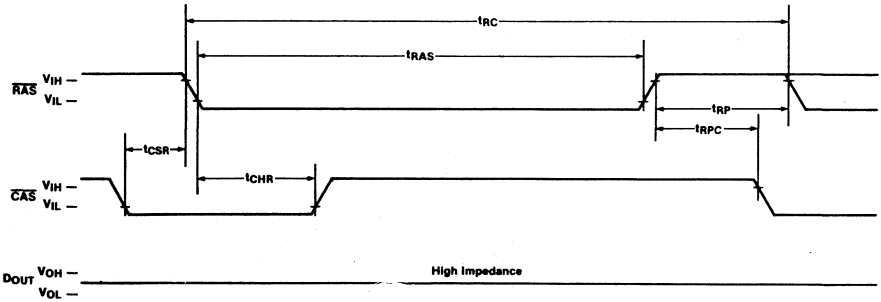
Page Mode Read-Write/Read-Modify-Write Cycle



Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

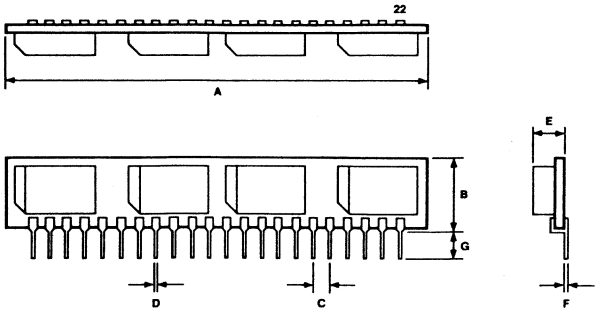


Note:
[1] $\overline{WE}$, Address: Don't Care.

Packaging Information

22-Pin SIMM, MC-411000A1A (Glass-epoxy Substrate)

Item	Millimeters
A	61.0
B	10.92 max
C	2.54
D	.45
E	5.30 max
F	.25
G	4.00



ECL RAMs

256 X 4 BIT 10 K ECL RAM

Description

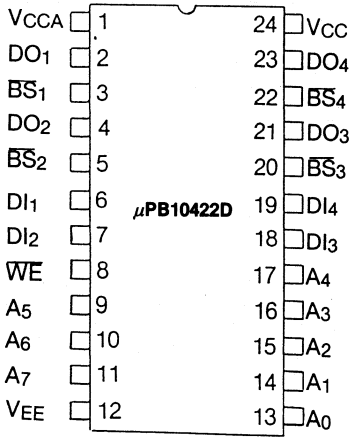
The NEC μPB10422 is a very high-speed ECL 10K interface Random-Access Memory. The device is organized as 256 words by 4 bits, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 7ns max (μPB 10422-7) and 10ns max (μPB10422-10).
The μPB1422 is available in a hermetic, 400mil, 24-lead DIP and is compatible with Fairschild's F10422® and Hitachi's HM 10422®
®= Registered trademarks.

Features

- ☐ 256 word x 4-bit organization
- ☐ ECL 10K interface compatible with Fairchild's F10422 and Hitachi's HM10422
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 24-lead, 400mil, DIP
- ☐ 2 performance ranges:

Device	Package	Access Time	Power Consumption
μPB10422-7	DIP	7ns max.	1.2W max.
μPB10422-10	DIP	10ns max.	1.2W max.

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1	V_{CCA}	Power Supply (current switches and bias driver)
2, 4, 21, 23	DO_1-DO_4	Data Outputs
3, 5, 20, 22	$\overline{BS}_1$-$\overline{BS}_4$	Block Selects
6, 7, 18, 19	DI_1-DI_4	Data Inputs
8	$\overline{WE}$	Write Enable
9-11, 13-17	A_0-A_7	Addresses
12	V_{EE}	Power Supply
24	V_{CC}	Power Supply (output devices)

Truth Table

Input $\overline{BS}$	Input $\overline{WE}$	Input D_{IN}	Output	Mode
H	X	X	L	Not Selected
L	L	L	L	Write0
L	L	H	L	Write1
L	H	X	D_{OUT}	Read

Note: X = Don't care.

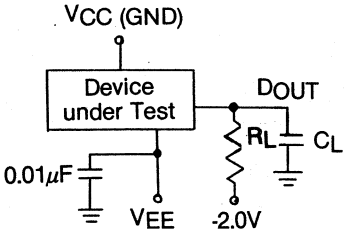
Absolute Maximum Ratings*

Supply Voltage, V_{EE} to V_{CC}	+0.5V to -7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current I_{OUT}	+0.1mA to -30mA
Storage Temperature, T_{STG}	-65°C to +150°C
Under Bias T_{STG} (Bias)	-55°C to +125°C

COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

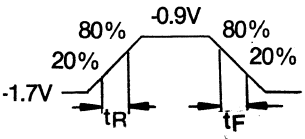
Capacitance

Parameter	Symbol	Limits 10422-7 Min.	Typ	Max.	10422-10 Min.	Typ	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}		4			4		pF	
Output Capacitance	C_{OUT}		5			5		pF	



Note: $R_L = 50\Omega$; $C_L = 30pF$.

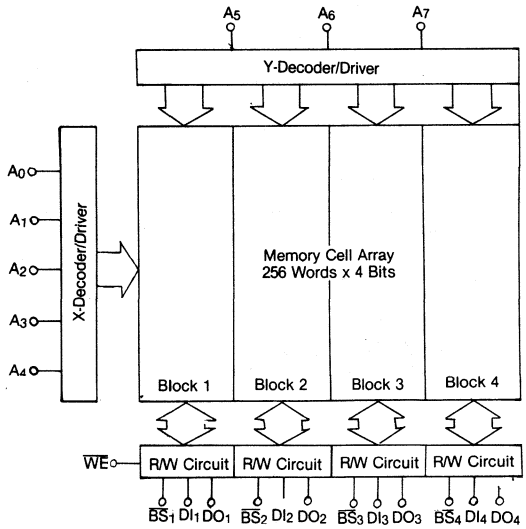
Figure 1: Loading Conditions Test Circuit



Note: $t_R = t_F = 2.5ns(typ)$.

Figure 2: Input Pulse Test Circuit

Block Diagram



DC Characteristics ①

$T_A = 0°C$ to $+75°C$; $V_{EE} = -5.2V \pm 5\%$; Output Load = 50Ω to -2V

Parameter	Symbol	T_A(°C)	Limits Min.	Typ	Max.	Unit	Test Conditions
Output Voltage	V_{OH}	0	-1000		-840	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
		+25	-960		-810		
		+75	-900		-720		
	V_{OL}	0	-1870		-1665		
		+25	-1850		-1650		
		+75	-1830		-1625		
Output Threshold Voltage	V_{OHC}	0	-1020			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
		+25	-980				
		+75	-920				
	V_{OLC}	0			-1645		
		+25			-1630		
		+75			-1605		
Input Voltage	V_{IH}	0	-1145		-840	mV	Guaranteed input voltage high for all inputs.
		+25	-1105		-810		
		+75	-1045		-720		
	V_{IL}	0	-1870		-1490		Guaranteed input voltage low for all inputs.
		+25	-1850		-1475		
		+75	-1830		-1450		
Input Current	I_{IH}	0 to +75			220	μA	$V_{in} = V_{IHA}$
	I_{IL}	0 to +75	0.5		170		$\overline{BS_1}$-$\overline{BS_4}$, $V_{IN} = V_{ILB}$
		0 to +75	-50				Others
Supply Current	I_{EE}	0 to +75	-220			mA	All inputs and outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec. maintained.

AC Characteristics ① ②

$T_A = 0°C$ to $+75°C$; $V_{EE} = -5.2V \pm 5\%$

Read Mode

Parameter	Symbol	Limits 10422-7 Min.	Typ	Max.	10422-10 Min.	Typ	Max.	Unit	Test Conditions
Block Select Access Time	t_{ABS}			5			5	ns	
Block Select Recovery Time	t_{RBS}			5			5	ns	
Address Access Time	t_{AA}			7			10	ns	

Write Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		10422-7			10422-10				
		Min.	Typ	Max.	Min.	Typ	Max.		
Write Pulse Width	t_W	5			6			ns	
Data Set-up Time	t_{WSD}	1			2			ns	
Data Hold Time	t_{WHD}	1			2			ns	
Address Set-up Time	t_{WSA}	1			2			ns	
Address Hold Time	t_{WHA}	1			2			ns	
Block Select Set-up Time	t_{WSBS}	1			2			ns	
Block Select Hold Time	t_{WHBS}	1			2			ns	
Write Disable Time	t_{WS}			5			5	ns	
Write Recovery Time	t_{WR}			6			9	ns	

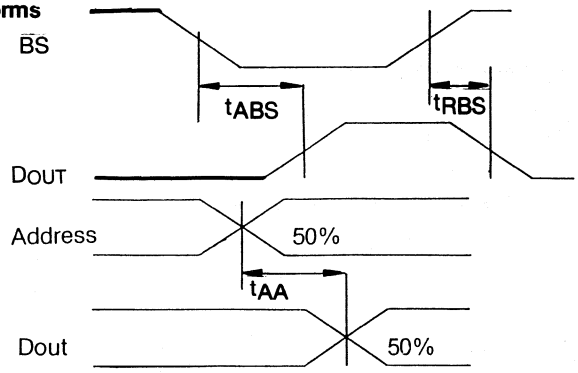
Output Rise and Fall Time

Parameter	Symbol	Limits						Unit	Test Conditions
		10422-7			10422-10				
		Min.	Typ	Max.	Min.	Typ	Max.		
Rise Time	t_R		2			2		ns	
Fall Time	t_F		2			2		ns	

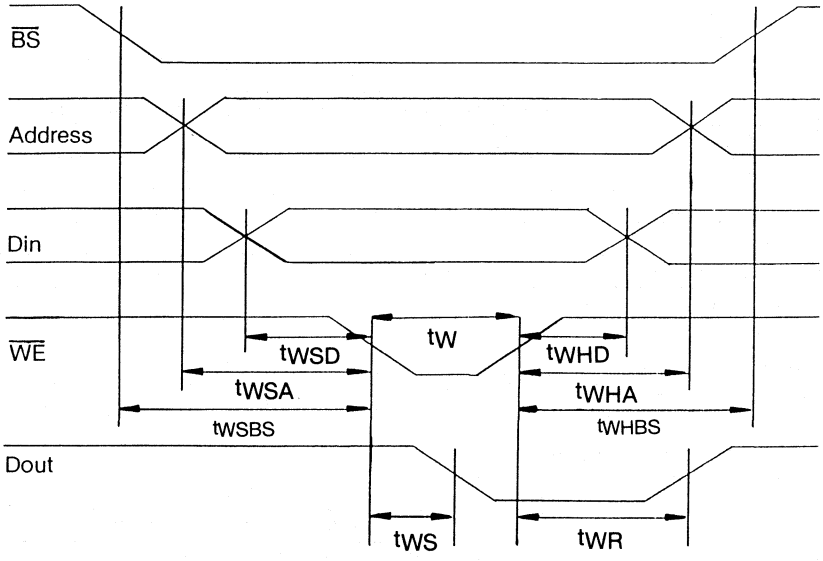
Notes: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.
② All timing measurements are referenced to 50% input levels

Timing Waveforms

Read Mode

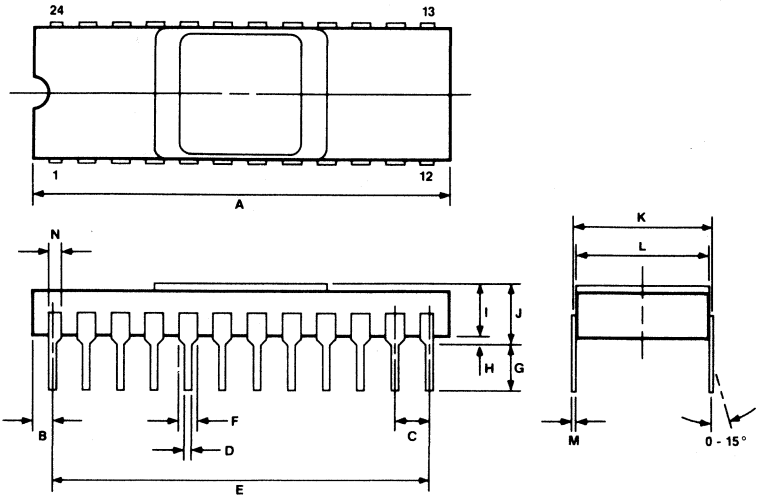


Write Mode



PACKAGE DIMENSIONS
24-PIN CERAMIC DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	27.94
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.74
J	4.57 max
K	10.16 [TP]
L	10.0
M	.25 ± .05
N	1.0 min



256 X 4-BIT 100 K ECL RAM

Description

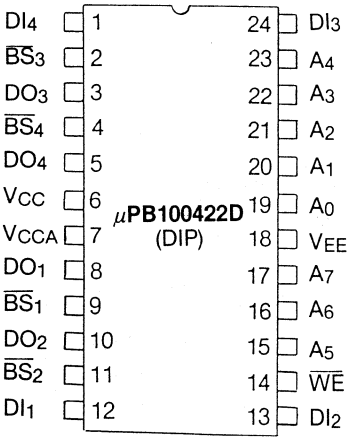
The NEC μPB100422 is a very high-speed ECL 100K interface Random-Access Memory. The device is organized as 256 words by 4 bits, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 7ns max (μPB100422-7) and 10ns max (μPB100422-10)
The μPB100422 is available in a hermetic, 400mil, 24-lead DIP (μPB100422D) or 24-lead flatpack (μPB100422B) version and is compatible with Fairchild's F100422® and Hitachi's HM 100422®.

Features

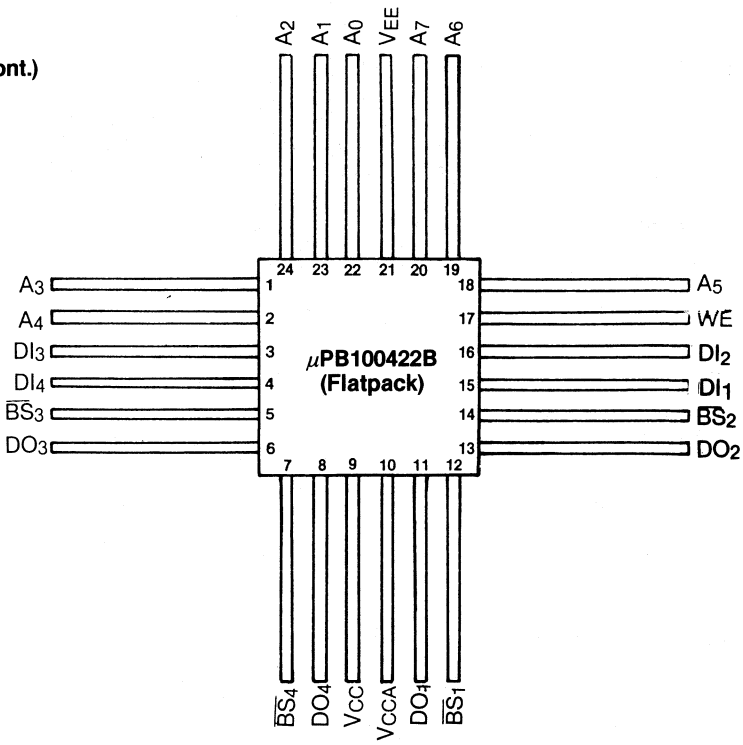
- ☐ 256-word x 4-bit organization
- ☐ ECL 100K interface compatible with Fairchild's F100422 and Hitachi's HM100422
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 24-lead, 400mil DIP or 24-lead flatpack
- ☐ 2 performance ranges:

Device	Package	Access Time	Power Consumption
μPB100422D-7	DIP	7 max	1W max
-10		10 max	1W max
μPB100422B-7	Flatpack	7 max	1W max
-10		10 max	1W max

Pin Configurations



Pin Configurations (Cont.)



Pin Identification

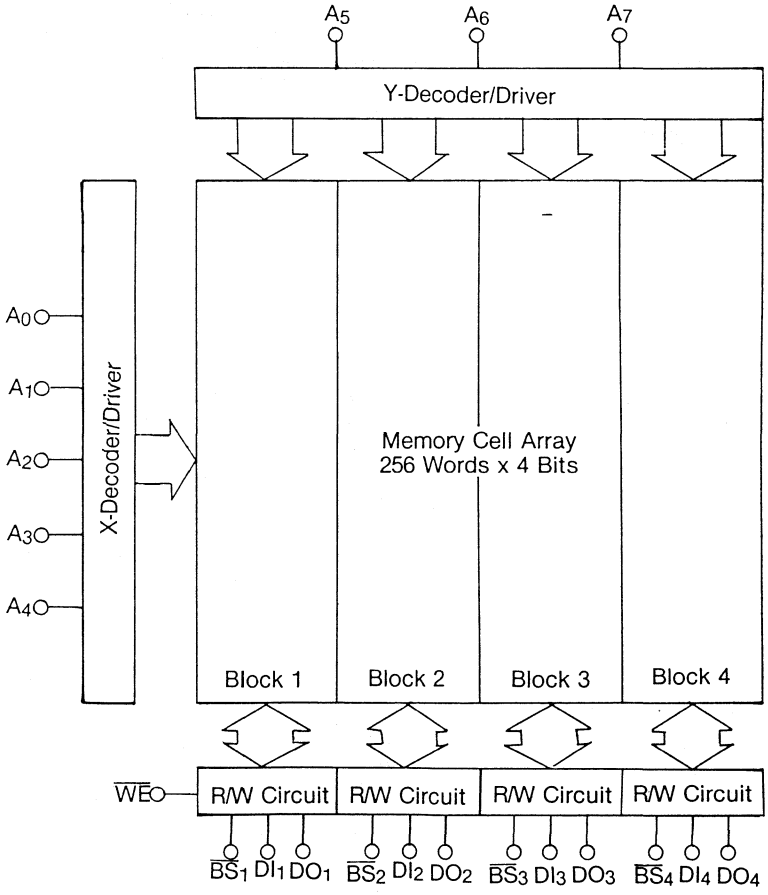
Pin Number		Symbol	Function
100422D	100422B		
1, 12, 13, 24	3, 4, 15, 16	DI_1-DI_4	Data Inputs
2, 4, 9, 11	5, 7, 12, 14	$\overline{BS_1}$-$\overline{BS_4}$	Block Selects
3, 5, 8, 10	6, 8, 11, 13	DO_1-DO_4	Data Outputs
6	9	V_{CC}	Power Supply (current switches and bias driver)
7	10	V_{CCA}	Power Supply (output devices)
14	17	$\overline{WE}$	Write Enable
15-17, 19-23	1, 2 18-20, 22-24	A_0-A_6	Addresses
18	21	V_{EE}	Power Supply

Truth Table

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Note: X = Don't care

Block Diagram



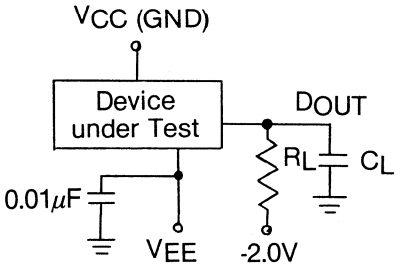
Absolute Maximum Ratings*

Supply Voltage, V_{EE} to V_{CC}	+ 0.5V to -7.0V
Input Voltage, V_{IN}	+ 0.5V to V_{EE}
Output Current I_{OUT}	+ 0.1mA to -30mA
Storage Temperature, T_{STG}	-65 °C to + 150 °C
Under Bias T_{STG} (Bias)	-55 °C to + 125 °C

COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

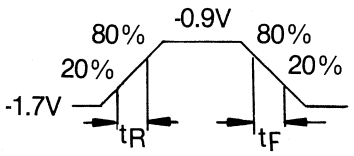
Capacitance

		Limits							
		100422-7			100422-10				Test
Parameter	Symbol	Min.	Typ	Max.	Min.	Typ	Max.	Unit	Conditions
Input Capacitance	C_{IN}		4			4		pF	
Output Capacitance	C_{OUT}		5			5		pF	



Note: $R_L = 50\Omega$; $C_L = 30pF$.

Figure 1: Loading Conditions Test Circuit



Note: $t_R = t_F = 2.5ns$ typ).

Figure 2: Input Pulse Test Circuit

DC Characteristics ①

$T_A = 0°C$ to $+85°C$; $V_{EE} = -4.5V \pm 5\%$; Output Load = 50Ω to −2V

Parameter	Symbol	T_A(°C)	Limits Min.	Typ	Max.	Unit	Test Conditions
Output Voltage	V_{OH}	0 to +85	-1025		-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
	V_{OL}	0 to +85	-1810		-1620		
Output Threshold Voltage	V_{OHC}	0 to +85	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
	V_{OLC}	0 to +85			-1610		
Input Voltage	V_{IH}	0 to +85	-1165		-880	mV	Guaranteed input voltage high for all inputs
	V_{IL}	0 to +85	-1810		-1475		Guaranteed input voltage low for all inputs.
Input Current	I_{IH}	0 to +85			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0 to +85	0.5		170		$\overline{BS_1}$-$\overline{BS_4}$, $V_{IN} = V_{ILB}$
		0 to +85	-50				Others
Supply Current	I_{EE}	0 to +85	-220			mA	All inputs and outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics ① ②

$T_A = 0°C$ to $+85°C$; $V_{EE} = -4.5V \pm 5\%$

Read Mode

Parameter	Symbol	Limits 100422-7 Min.	Typ	Max.	100422-10 Min.	Typ	Max.	Unit	Test Conditions
Block Select Access Time	t_{ABS}			5			5	ns	
Block Select Recovery Time	t_{RBS}			5			5	ns	
Address Access Time	t_{AA}			7			10	ns	

Write Mode

Parameter	Symbol	Limits 10422-7 Min.	Typ	Max.	10422-10 Min.	Typ	Max.	Unit	Test Conditions
Write Pulse Width	t_W	5			6			ns	
Data Set-up Time	t_{WSD}	1			2			ns	
Data Hold Time	t_{WHD}	1			2			ns	
Address Set-up Time	t_{WSA}	1			2			ns	
Address Hold Time	t_{WHA}	1			2			ns	
Block Select Set-up Time	t_{WSBS}	1			2			ns	
Block Select Hold Time	t_{WHBS}	1			2			ns	
Write Disable Time	t_{WS}			5			5	ns	
Write Recovery Time	t_{WR}			6			9	ns	

AC Characteristics (Cont.)① ②

$T_A = 0°C$ to $+85°C$; $V_{EE} = -4.5V \pm 5\%$

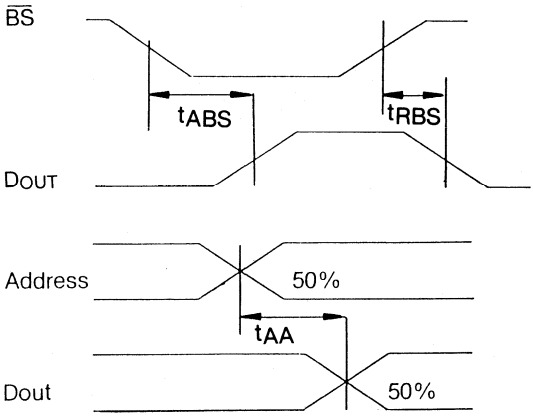
Output Rise and Fall Time

Parameter	Symbol	Limits						Unit	Test Conditions
		100422-7			100422-10				
		Min.	Typ	Max.	Min.	Typ	Max.		
Rise Time	t_R		2			2		ns	
Fall Time	t_F		2			2		ns	

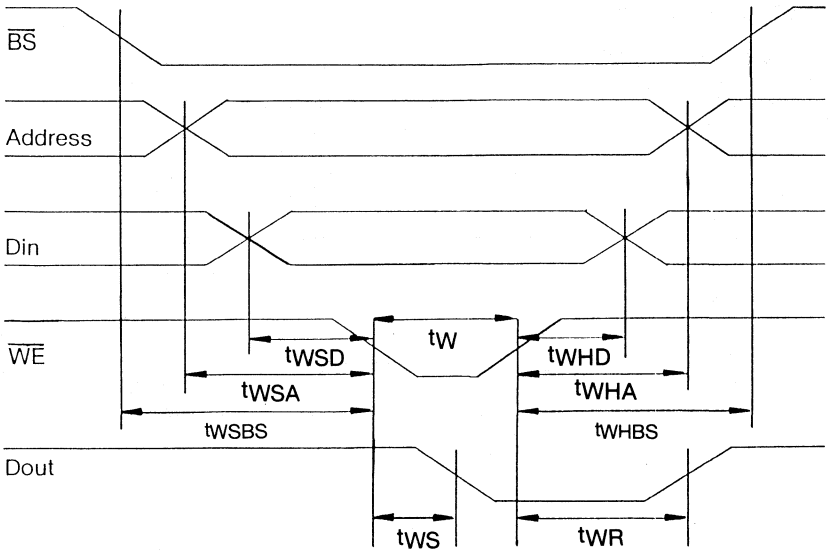
Notes: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.
② All timing measurements are referenced to 50% input levels

Timing Waveforms

Read Mode



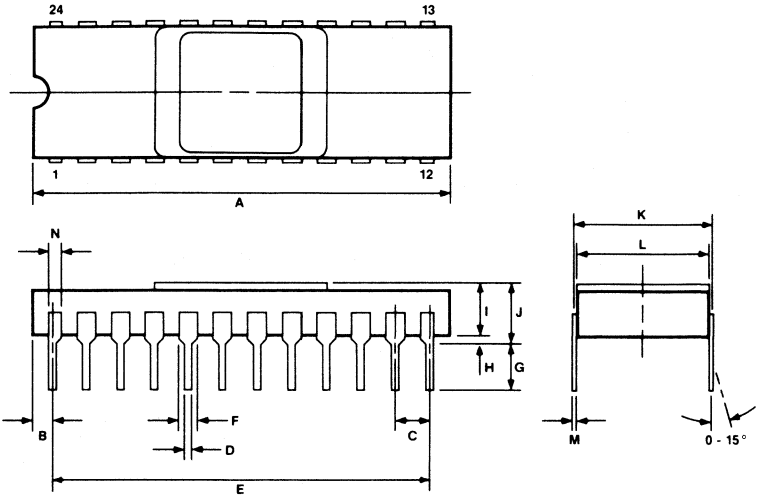
Write Mode


BS
Address
Din
WE
Dout
tWSD
tW
tWHD
tWSA
tWHA
tWSBS
tWHBS
tWS
tWR

PACKAGE DIMENSIONS

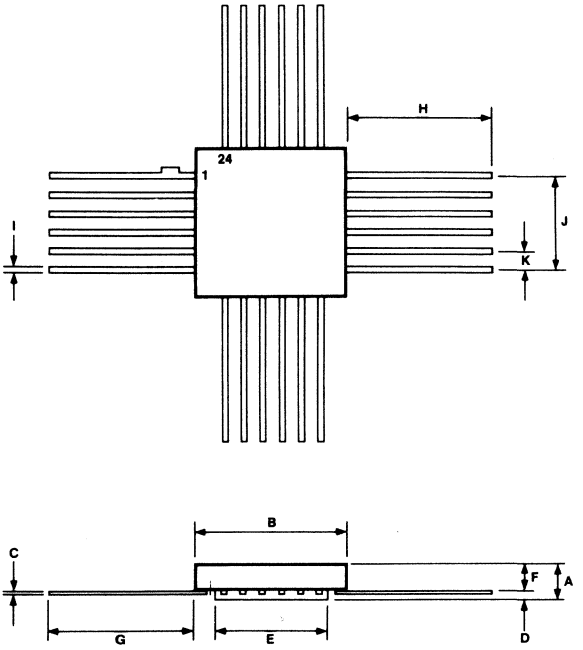
24-PIN CERAMIC DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	27.94
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.74
J	4.57 max
K	10.16 [TP]
L	10.0
M	.25 ± .05
N	1.0 min



24-PIN CERAMIC FLATPACK

Item	Millimeters
A	2.6 max
B	9.5
C	.13
D	.5
E	6.9
F	2.0
G	8.9
H	8.9
I	.43
J	6.35
K	1.27



4,096 x 1-Bit 10K ECL RAM

Description

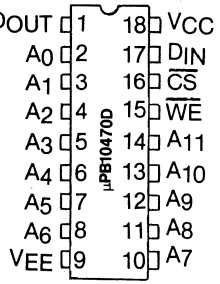
The NEC μPB10470 is a very high-speed ECL 10K interface Random-Access Memory. The device is organized as 4K words by 1 bit, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 10 ns max (μPB10470-10) and 15 ns (μPB10470-15).
The μPB10470 is available in a hermetic, 300 mil, 18-lead DIP and is compatible with Fairchild's F10470® and Hitachi's HM 10470®.
® = Registered trademarks.

Features

- ☐ 4K-word x 1-bit organization
- ☐ ECL 10K interface compatible with Fairchild's F10470 and Hitachi's HM 10470
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 18-lead, 300mil, DIP
- ☐ 2 performance ranges:

Device	Package	Access Time	Power Consumption
μPB10470-10	DIP	10ns max	1,2W max
μPB10470-15	DIP	15ns max	1,2W max

Pin Configuration



Pin Identification

Pin		Function
No.	Symbol	
1	D_{out}	Data Output
2-8 10-14	A_0-A_{11}	Addresses
9	V_{EE}	Power Supply
15	$\overline{WE}$	Write Enable
16	$\overline{CS}$	Chip Enable
17	D_{IN}	Data Input
18	V_{CC}	Power Supply

Truth Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{out}	Read

Note: X = Don't care.

Absolute Maximum Ratings*

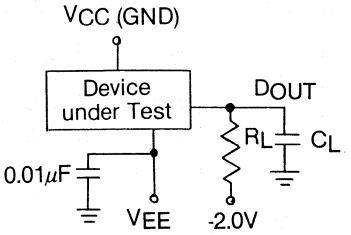
Supply Voltage, V_{EE} to V_{CC}	+0.5V to -7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current, I_{OUT}	+0.1mA to -30mA
Storage Temperature, T_{STG}	-65° to +150°C
Under Bias, T_{STG} (Bias)	-55°C to +125°C

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device ist not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

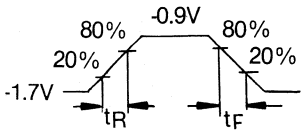
		Limits							
		10470-10			10470-15				Test
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
Input Capacitance	C_{IN}		4			4		pF	
Output Capacitance	C_{OUT}		5			5		pF	

Figure 1. Loading Conditions Test Circuit



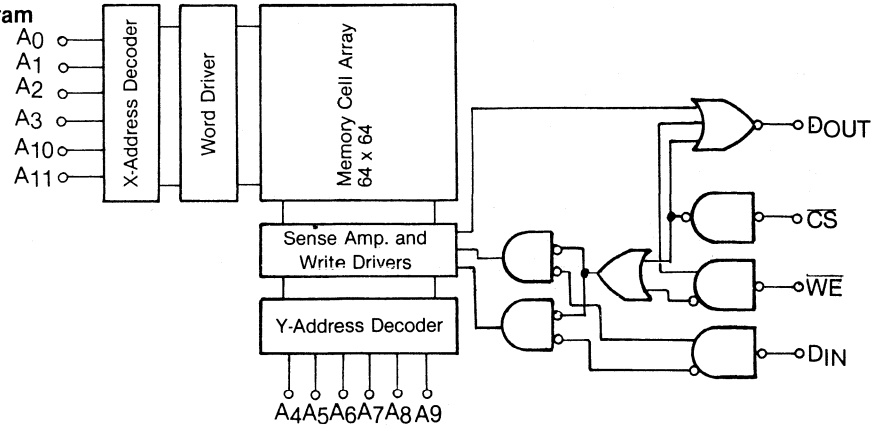
Note: R_L = 50Ω; C_L = 30pF.

Figure 2. Input Pulse Test Circuit



Note: $t_R = t_F = 2.5$ns (typ).

Block Diagram



DC Characteristics ①

$T_A = 0°$ C to $+75°$ C; $V_{EE} = -5.2V \pm 5\%$; Output Load = 50Ω to -2V

Parameter	Symbol	T_A(° C)	Limits Min	Typ	Max	Unit	Test Conditions
Output Voltage	V_{OH}	0	-1000		-840	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
		+25	-960		-810		
		+75	-900		-720		
	V_{OL}	0	-1870		-1665		
		+25	-1850		-1650		
		+75	-1830		-1625		
Output Threshold Voltage	V_{OHC}	0	-1020			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
		+25	-980				
		+75	-920				
	V_{OLC}	0			-1645		
		+25			-1630		
		+75			-1605		
Input Voltage	V_{IH}	0	-1145		-840	mV	Guaranteed Input voltage high for all inputs.
		+25	-1105		-810		
		+75	-1045		-720		
	V_{IL}	0	-1870		-1490		Guaranteed Input voltage low for all inputs.
		+25	-1850		-1475		
		+75	-1830		-1450		
Input Current	I_{IH}	0 to +75			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0 to +75	0.5		170		$\overline{CS}$: $V_{IN} = V_{ILB}$
		0 to +75	-50				Others: $V_{IN} = V_{ILB}$
Supply Current	I_{EE}	0 to +75	-220			mA	All Inputs and outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics ①

$T_A = 0°C$ to $+75°C$; $V_{EE} = -5.2V \pm 5\%$

Read Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		10470-10			10470-15				
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}			6			8	ns	
Chip Select Recovery Time	t_{RCS}			6			8	ns	
Address Access Time	t_{AA}			10			15	ns	

Note: ① The device under test (DUT) ist mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics (Cont.)①

$T_A = 0°C$ to $+75°C$; $V_{EE} = 5.2V \pm 5\%$

Write Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		10470-10			10470-15				
		Min	Typ	Max	Min	Typ	Max		
Write pulse width	t_W	10			15			ns	
Data set-up time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address set-up time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select set-up time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	

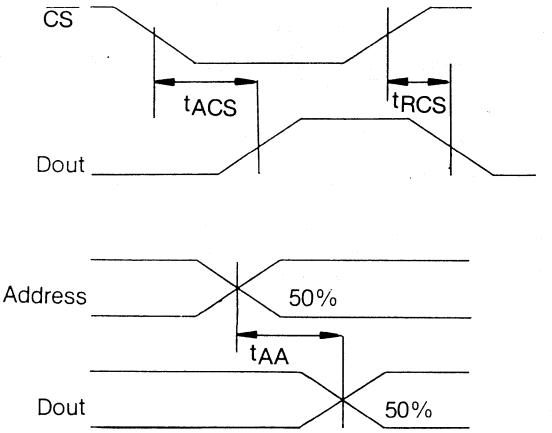
Output Rise and Falls Times

Parameter	Symbol	Limits						Unit	Test Conditions
		10470-10			10470-15				
		Min	Typ	Max	Min	Typ	Max		
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

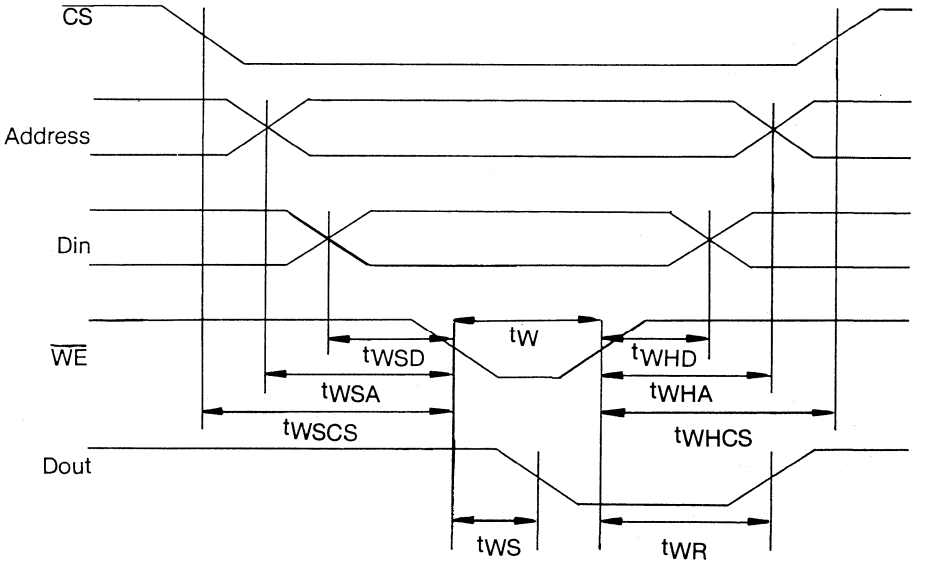
Note: ① The device under test (DUT) ist mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

Timing Waveforms

Read Mode

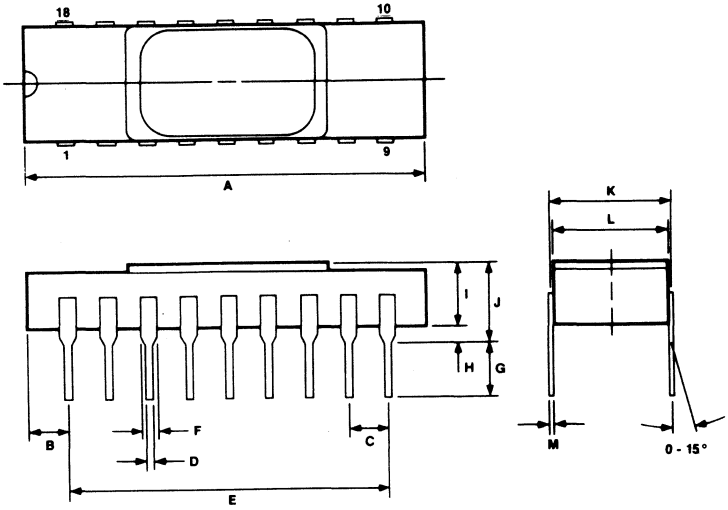


Write Mode



PACKAGE DIMENSIONS
18-PIN CERAMIC DIP

Item	Millimeters
A	25.40 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.90
J	4.57 max
K	7.62 [TP]
L	7.32
M	.25 ± .05



4,096x1-BIT 100K ECL RAM

Description

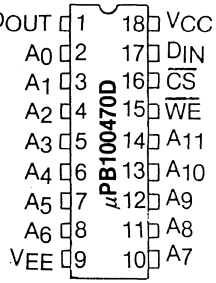
The μPB100470 is a very high-speed ECL 100K interface Random-Access Memory with full voltage and temperature compensation. The devise is organized as 4K words by 1 bit, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 10ns (μPB100470-10) and 15ns max (μPB100470-15).
The μPB100470 is available in a hermetic, 300mil, 18-lead DIP and is compatible with Fairchild's F100470® and Hitachi's HM 100470®)
® = Registered trademarks.

Features

- ☐ 4K-word x 1-bit organization
- ☐ ECL 100K interface
  - Full voltage and temperature compensation
  - Compatible with Fairchild's F100470 and Hitachi's HM100470
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 18-lead, 300 mil, DIP and LCC
- ☐ 2 performance ranges:

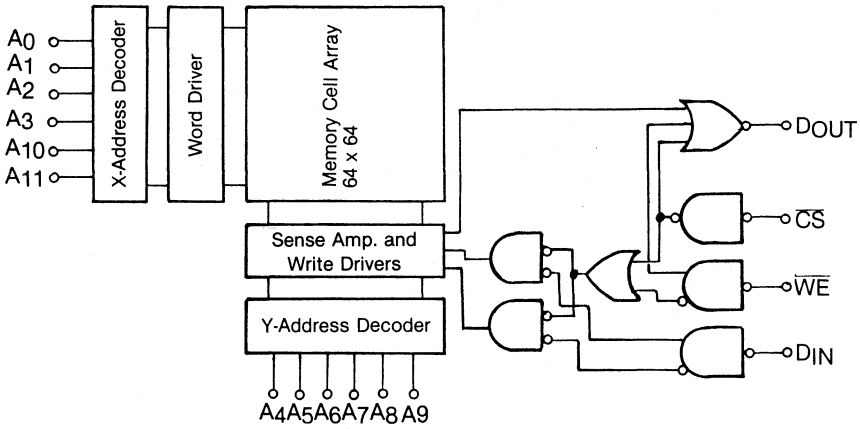
Device	Package	Access Time	Power Consumption
μPB100470-10	DIP	10ns max.	1W max.
μPB100470-15	DIP	15ns max.	1W max.

Pin Configuration



Pin Identification

Pin		
No.	**Symbol**	**Function**
1	D_{OUT}	Data Output
2-8, 10-14	A_0-A_{11}	Addresses
9	V_{EE}	Power Supply
15	$\overline{WE}$	Write Enable
16	$\overline{CS}$	Chip Select
17	D_{IN}	Data Input
18	V_{CC}	Power Supply



DC Characteristics ①

$T_A = 0°C$ to $+85°C$; $V_{EE} = -4.5V \pm 5\%$; Output Load = 50Ω to -2V

Parameter	Symbol	T_A(°)	Limits Min.	Typ	Max	Unit	Test Conditions
Output Voltage	V_{OH}	0 to +85	-1025		-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
	V_{OL}	0 to +85	-1810		-1620		
Output Threshold Voltage	V_{OHC}	0 to +85	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
	V_{OLC}	0 to +85			-1610		
Input Voltage	V_{IH}	0 to +85	-1165		-880	mV	Guaranteed Input Voltage high for all Inputs.
	V_{IL}	0 to +85	-1810		-1475		Guaranteed Input Voltage low for all Inputs.
Input Current	I_{IH}	0 to +85			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0 to +85	0.5		170		$\overline{CS}$
	I_{IL}	0 to +85	-50				Others $V_{IN} = V_{ILB}$
Supply Current	I_{EE}	0 to +85	-220			mA	All Inputs and Outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics ①

$T_A = 0°C$ to $+85°C$; $V_{EE} = -4.5V \pm 5\%$

Read Mode

Parameter	Symbol	Limits 100470-10 Min.	Typ	Max.	100470-15 Min.	Typ	Max.	Unit	Test Conditions
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Address access time	t_{AA}			10			15	ns	

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics (Cont.) ①

$T_A = 0°$ C to $+85°$ C; $V_{EE} = -4.5V \pm 5\%$

Write Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		100470-10			100470-15				
		Min.	Typ	Max.	Min.	Typ	Max.		
Write pulse width	t_W	10			15			ns	
Data set-up time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address set-up time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select set-up time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	

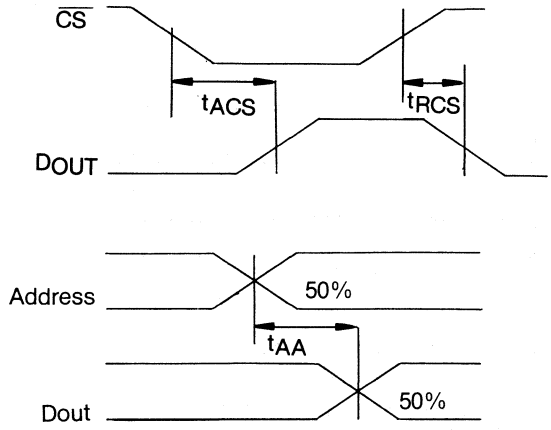
Output Rise and Fall Times

Parameter	Symbol	Limits						Unit	Test Conditions
		100470-10			100470-15				
		Min.	Typ	Max.	Min.	Typ	Max.		
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

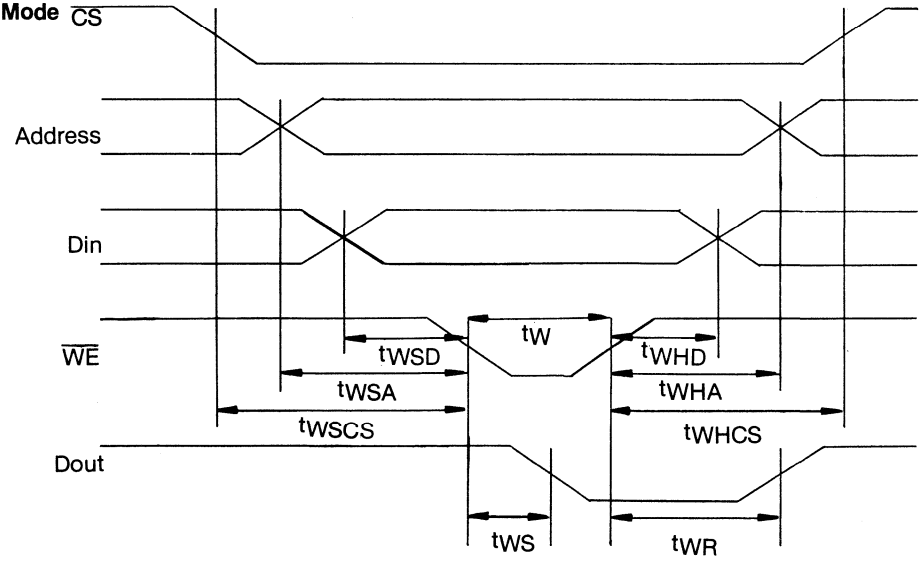
Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

Timing Waveforms

Read Mode



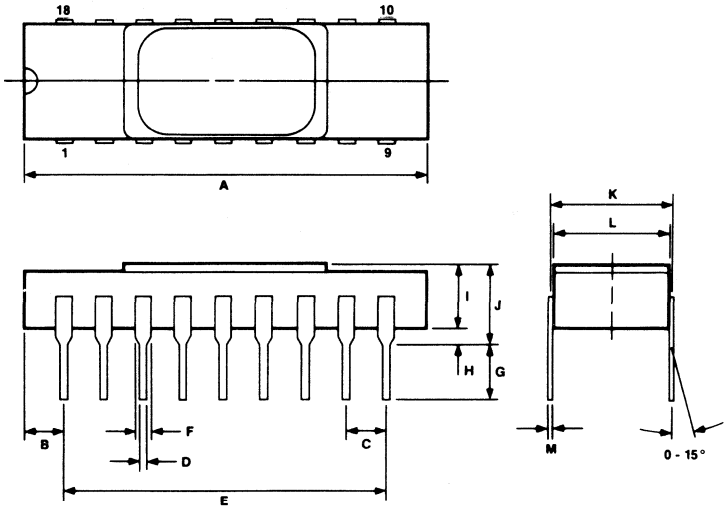
Write Mode



Package Dimensions

18 PIN Ceramic DIP (300 mil)

Item	Millimeters
A	25.40 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.90
J	4.57 max
K	7.62 [TP]
L	7.32
M	.25 ± .05



1,024x4-BIT 10K ECL RAM

Description

The NEC μPB10474 is a very high-speed ECL 10K interface Random-Access Memory. The device is organized as 1K words by 4 bits, with an open emitter output (noninverted), and low power consumption. Four fast access time versions are available: 8ns max (μPB10474-8), 9ns max (μPB10474-9), 10ns max (μPB10474-10) and 15ns max (μPB10474-15).

The μPB10474 is available in a hermetic, 400 mil, 24-lead DIP and is compatible with Fairchild's F10474® and Hitachi's HM10474®

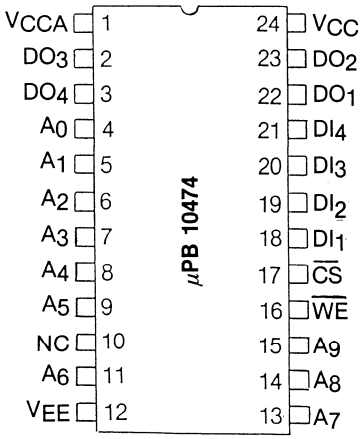
® = Registered trademarks.

Features

- ☐ 1K-word x 4-bit organization
- ☐ ECL 10K interface compatible with Fairchild's F10474 and Hitachi's HM10474
- ☐ Open emitter output (noninverted)
- ☐ Fast access time
- ☐ Low power consumption
- ☐ Available in 24-lead, 400 mil, DIP
- ☐ 4 performance ranges:

Device	Package	Access time	Power comsumption
μPB10474-8	**DIP**	**8ns max**	**1.2W max**
μPB10474-9	**DIP**	**9ns max**	**1.2W max**
μPB10474-10	**DIP**	**10ns max**	**1.2W max**
μPB10474-15	**DIP**	**15ns max**	**1.2W max**

Pin Configuration



Pin Identification

PIN No.	PIN Symbol	Function
1	V_{CCA}	Power supply (current switches and bias driver)
2. 3. 22-23	DO_1-DO_4	Data outputs
4-9. 11. 13-15	A_0-A_9	Addresses
10	NC	No Connection
12	V_{EE}	Power Supply
16	$\overline{WE}$	Write enable
17	$\overline{CS}$	Chip select
18-21	DI_1-DI_4	Data Inputs
24	V_{CC}	Power supply (output devices)

Truth Table

Input $\overline{CS}$	Input $\overline{WE}$	Input D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Note: X = Don't care.

Absolute Maximum Ratings*

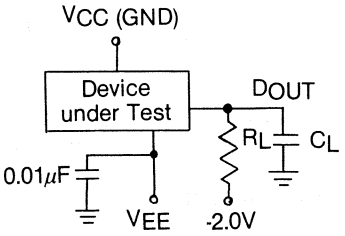
Supply Voltage, V_{EE} to V_{CC}	+0.5V to-7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current, I_{OUT}	+0.1mA to-30mA
Storage Voltage (under bias), T_{STG} (Bias)	-55°C to +125°C
Storage Temperature, T_{STG}	-65°C to +150°C

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

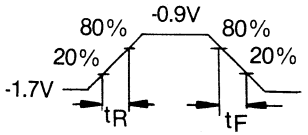
Parameter	Symbol	Limits 10474-8/9/10/15 Min.	Typ	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}		4		pF	
Output Capacitance	C_{OUT}		5		pF	

Figure 1.
Loading Conditions Test Circuit



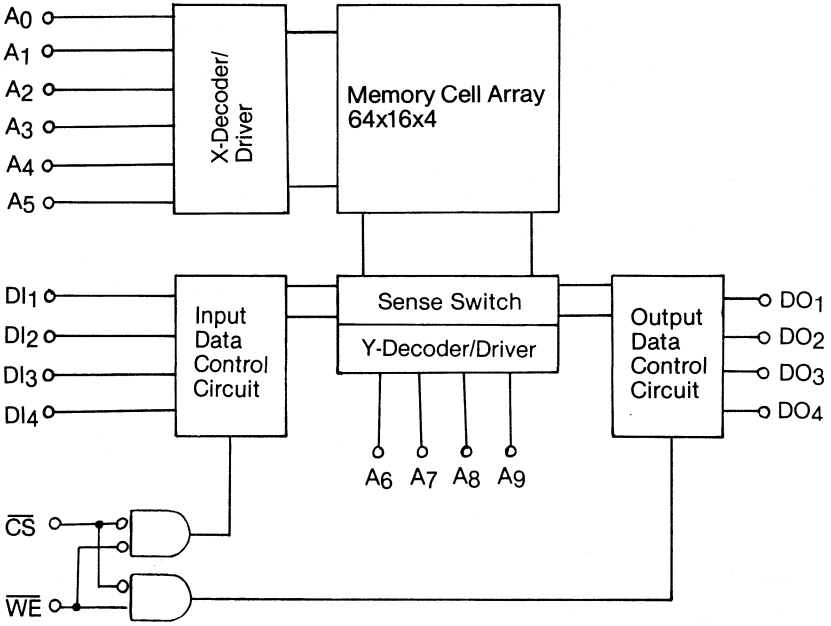
Note: $R_L = 50\Omega$; $C_L = 30pF$.

Figure 2.
Input Pulse Test Circuit



Note: $t_R = t_F = 2.5ns$ (typ).

Block Diagram



DC-Characteristics ①

$T_A = 0°$ C to $+75°$ C; $V_{EE} = -5.2V \pm 5\%$; Output Load = 50Ω to -2V

Parameter	Symbol	T_A (°C)	Limits Min.	Limits Typ	Limits Max.	Unit	Test Conditions
Output Voltage	V_{OH}	0	-1000		-840	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
		+25	-960		-810		
		+75	-900		-720		
	V_{OL}	0	-1870		-1665		
		+25	-1850		-1650		
		+75	-1830		-1625		
Output Threshold Voltage	V_{OHC}	0	-1020			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
		+25	-980				
		+75	-920				
	V_{OLC}	0			-1645		
		+25			-1630		
		+75			-1605		
Input Voltage	V_{IH}	0	-1145		-840	mV	Guaranteed Input Voltage high for all Inputs.
		+25	-1105		-810		
		+75	-1045		-720		
	V_{IL}	0	-1870		-1490		Guaranteed Input voltage low for all Inputs.
		+25	-1850		-1475		
		+75	-1830		-1450		
Input Current	I_{IH}	0 to +75			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0 to +75	0.5		170		$\overline{CS}$
		0 to +75	-50				Others $V_{IN} = V_{ILB}$
Supply Current	I_{EE}	0 to +75	-220			mA	All Inputs and outputs are open.

Note: ①The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium establisblished with a transverse air flow greater than 2,0m/sec. maintained.

AC Characteristics ①

$T_A = 0°$ C to $+75°$ C; $V_{EE} = -5.2V \pm 5\%$

Read Mode

Parameter	Symbol	Limits μPB10474-8 Min.	Typ	Max.	Limits μPB10474-9 Min.	Typ	Max.	Unit
Chip select access time	t_{ACS}	–	–	5	–	–	6	ns
Chip select recovery time	t_{RCS}	–	–	5	–	–	6	ns
Address access time	t_{AA}	–	–	8	–	–	9	ns

AC Characteritics (Cont.) ①

$T_A = 0°C$ to $+75°C$; $V_{EE} = -5.2V \pm 5\%$

Parameter	Symbol	Limits						Unit	Test Conditions
		10474-10			10474-15				
		Min.	Typ	Max.	Min.	Typ	Max,		
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Address access time	t_{AA}			10			15	ns	

Write Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		μPB10474-8			μPB10474-9				
		Min.	Typ	Max.	Min.	Typ	Max.		
Write pulse width	t_W	6			10			ns	
Data set-up time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address set-up time	t_{WSA}	1			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select set-up time	t_{WSCS}	1			2			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			6	ns	
Write recovery time	t_{WR}			8			10	ns	

Write Mode

Parameter	Symbol	Limits						Unit	Test Conditions
		10474-10			10474-15				
		Min.	Typ	Max.	Min.	Typ	Max.		
Write pulse width	t_W	10			15			ns	
Data set-up time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address set-up time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select set-up time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	

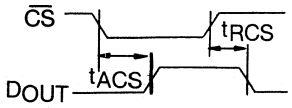
Output Rise and Fall Times

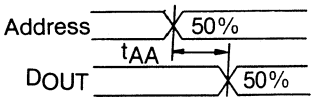
Parameter	Symbol	Limits 10474-8/9/10/15 Min.	Typ	Max.	Unit	Test Conditions
Rise time	t_R		2		ns	
Fall time	t_F		2		ns	

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transferse air flow greater than 2.0m/sec. maintained.

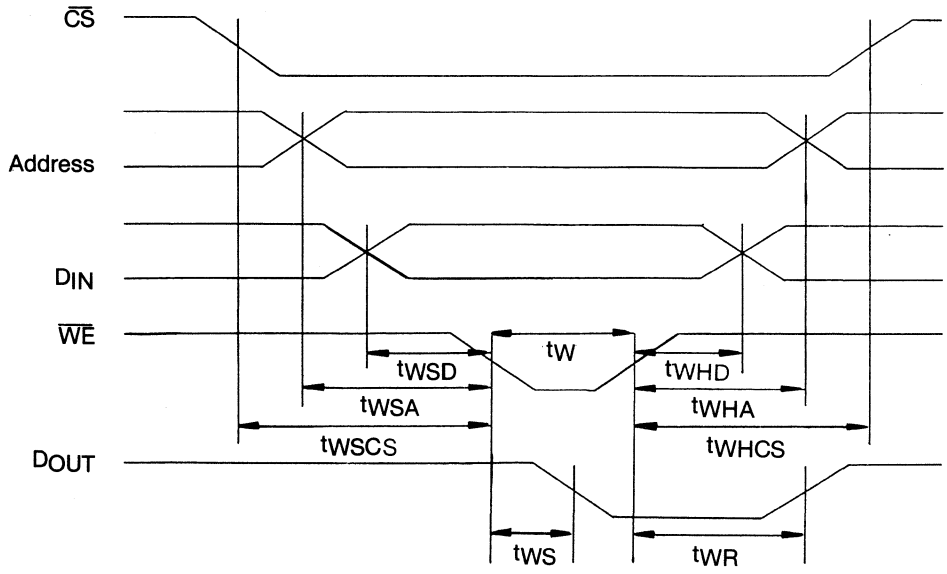
Timing Waveforms

Read Mode





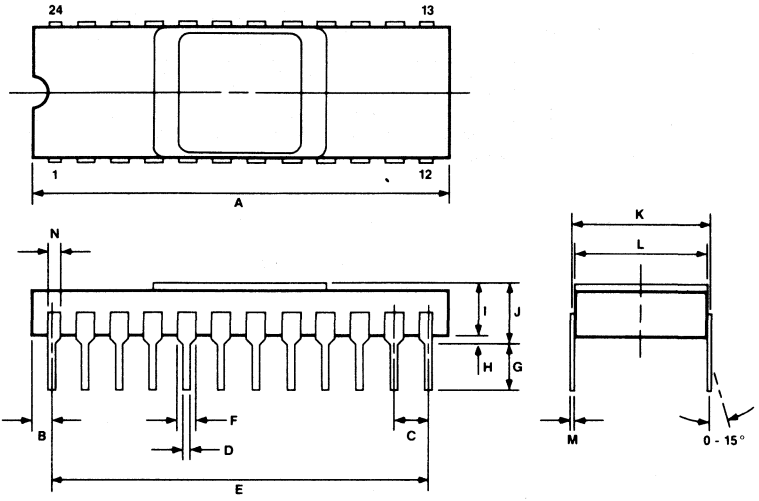
Write Mode



PACKAGE DIMENSIONS

24-PIN CERAMIC DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	27.94
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.74
J	4.57 max
K	10.16 [TP]
L	10.0
M	.25 ± .05
N	1.0 min



1.024x4 Bit 100K ECL RAM

Description

NEC's μPB100474 is a very high-speed ECL 100K interface Random-Access Memory. It operates with full voltage and temperature compensation and is compatible with Fairchild's F100474® and Hitachi's HM100474®.
The μPB100474 is organized as 1K words by 4 bits with fast access times (4.5ns to 15ns), open emitter outputs (noninverted) and low power consumption. It is available in a hermetic DIP (μPB100474D), leadless chip carrier (LCC) (μPB100474K), or flatpack, 24-lead package (μPB100474B) version.
® = Registered trademarks.

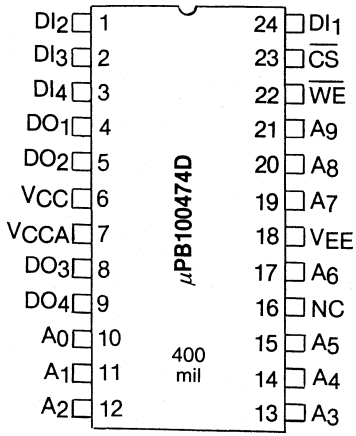
Features

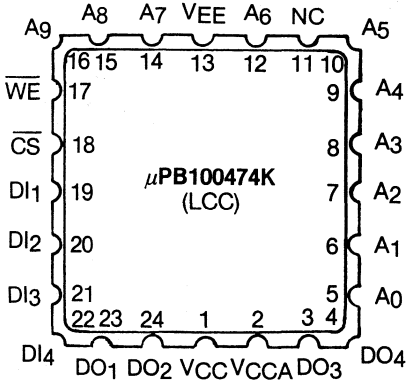
- ☐ 1K-word x 4-bit organization
- ☐ ECL 100K interface
  - -Full voltage and temperature compensation
  - -Compatible with Fairchild's F100474 and Hitachi's HM100474
- ☐ Open emitter output (noninverted)
- ☐ Fast access time
- ☐ Low power consumption
- ☐ Available in DIP, LCC, and flatpack versions
- ☐ 7 performance ranges:

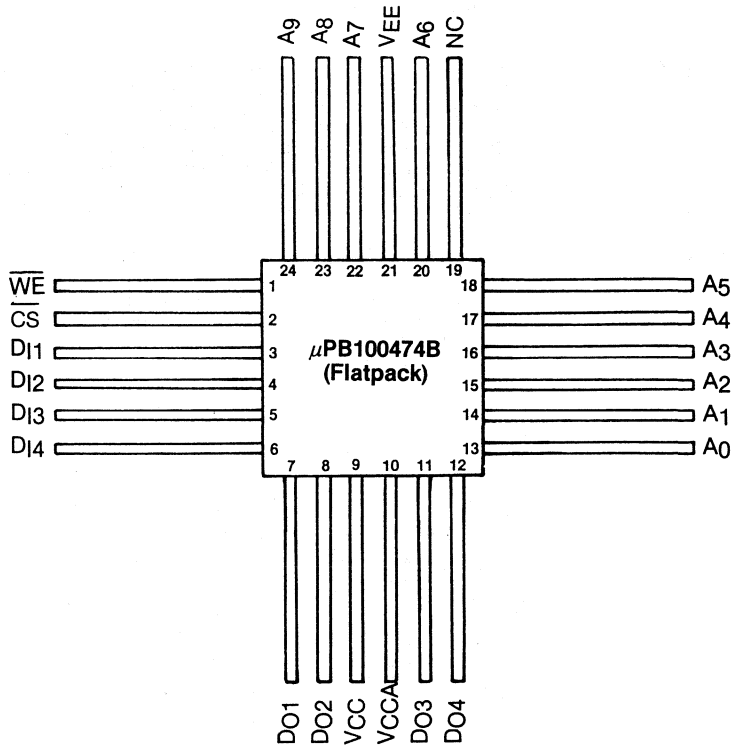
Device	Package Type	Access Time (max)	Power Consumption (max)
μPB100474 K/B-45	LCC/Flatpack	4,5ns	2W①
μPB100474 K/B-50	LCC/Flatpack	5ns	2W①
μPB100474 K/B-60	LCC/Flatpack	6ns	2W①
μPB100474 D/B-8	DIP/Flatpack	8ns	1W
μPB100474 D/B-9	DIP/Flatpack	9ns	1W
μPB100474 D/B-10	DIP/Flatpack	10ns	1W
μPB100474 D/B-15	DIP/Flatpack	15ns	1W

Note: ① Heatsink required, maximum case temperature = 95° C

Pin Configurations







Pin Identification

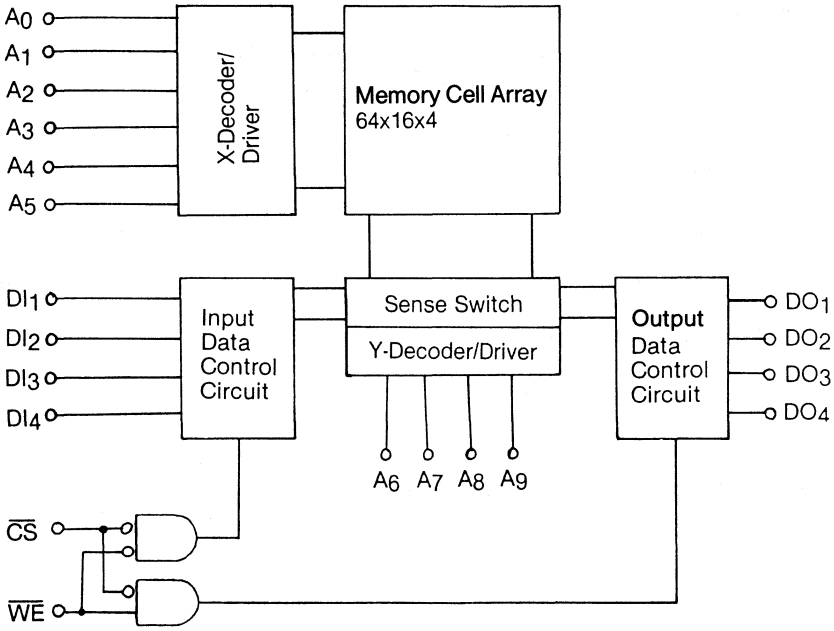
Pin Number				
100474D	100474K	100474B	Symbol	Function
1-3, 24	19-22	3-6	D_{I1}-D_{I4}	Data Inputs
4, 5, 8, 9	23, 24, 3, 4	7, 8, 11, 12	D_{O1}-D_{O4}	Data Outputs
6	1	9	V_{CC}	Power Supply
7	2	10	V_{CCA}	Power Supply
10-15, 17 19-21	5-10, 12 14-16	13-18, 20, 22-24	A_0-A_9	Addresses
16	11	19	NC	No Connection
18	13	21	V_{EE}	Power Supply
22	17	1	$\overline{WE}$	Write Enable
23	18	2	$\overline{CE}$	Chip Select

Truth Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Note: X = Don't care.

Block Diagram



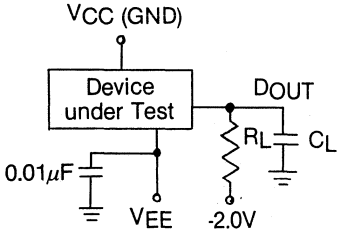
Absolute Maximum Ratings*

Supply Voltage, V_{EE} to V_{CC}	+0,5V to -7,0V
Input Voltage, V_{IN}	+0,5V to V_{EE}
Output Current, I_{OUT}	+0,1mA to -30mA
Storage Temperature, T_{STG}	-65°C to +150°C
Under bias T_{STG} (Bias)	-55°C to +125°C

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

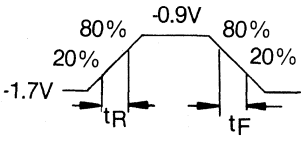
Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4		pF	
Output Capacitance	C_{OUT}		5		pF	



Note: $t_R = t_F = 2.0ns$

Figure 1. Loading Conditions Test Circuit



Note: RL = 50Ω:
For -8/9/10/15, CL = 30pF
For -45/50/60, CL = 5pF

Figure 2. Input Pulse Test Circuit

DC Characteristics ②

$T_A = 0°$ C to $+85°$ C; $V_{EE} = -4{,}5V$; Output Load = 50Ω to -2V

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Output Voltage	V_{OH}	-1025		-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
	V_{OL}	-1810		-1620	mV	
Output Threshold Voltage	V_{OHC}	-1035			mV	$V_{IN} = V_{ILB}$ or V_{ILA}
	V_{OLC}			-1610	mV	
Input Voltage	V_{IH}	-1165		-880	mV	Guaranteed Input Voltage high for all Inputs
	V_{IL}	-1810		-1475	mV	Guaranteed Input Voltage low for all Inputs
Input Current	I_{IH}			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0.5		170	μA	$\overline{CS}$
		-50			μA	Others $V_{IN} = V_{ILB}$
Supply Current	I_{EE}	-450	-360		mA	t_{AA} = 4,5/5/6 ns All Inputs and Outputs open note 1
		-220	-160		mA	t_{AA} = 8/9/10/15ns All Inputs and Outputs open

Note: ①When an LCC package is applied with a high-power (1.6W typ) chip, special measures must be taken to reduce the thermal resistance and to keep the function temperature less than 100 °C. Forced air and an appropriate type of FINs on the substrate on which the package is mounted, or on the package directly, are recommended. The thermal resistance junction to the case (bottom side) of an LCC or flatpack package is less than 10 °C/W.

②The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics① T_A=0°C to +85°C; V_{EE} = -4,5V±5%

Read Mode

Parameter	Symbol	Grade ②	Limits Min	Typ	Max	Units
Chip Select access Time	t_{ACS}	-15			8	ns
		-10			6	
		-9			6	
		-8			5	
		-60			4	
		-50			4	
		-45			4	
Chip Select Recovery Time	t_{RCS}	-15			8	ns
		-10			6	
		-9			6	
		-8			5	
		-60			4	
		-50			4	
		-45			4	
Address Access Time	t_{AA}	-15			15	ns
		-10			10	
		-9			9	
		-8			8	
		-60			6	
		-50			5	
		-45			4,5	

AC Characteristic ① (Cont.)

Write Mode

Parameter	Symbol	Grade ②	Limits Min	Limits Typ	Limits Max	Unit
Write Pulse Width	tW	-15	15			ns
		-10	10			
		-9	10			
		-8	6			
		-60	6			
		-50	5			
		-45	4,5			
Data Set-up Time	tWSD	-15	2			ns
		-10	2			
		-9	2			
		-8	1			
		-60	1			
		-50	1			
		-45	1			
Data Hold Time	tWHD	-15	2			ns
		-10	2			
		-9	2			
		-8	1			
		-60	1			
		-50	1			
		-45	1			
Address Set-up Time	tWSA	-15	3			ns
		-10	3			
		-9	3			
		-8	1			
		-60	1			
		-50	1			
		-45	1			
Address Hold Time	tWHA	-15	2			ns
		-10	2			
		-9	2			
		-8	1			
		-60	2			
		-50	2			
		-45	2			
Chip Select Set-up Time	tWSCS	-15	2			ns
		-10	2			
		-9	2			
		-8	1			
		-60	1			
		-50	1			
		-45	1			

AC Characteristics (Cont.) ① Write Mode (Cont.)

Parameter	Symbol	Grade ②	Limits Min	Typ	Max	Unit
Chip Select Hold Time	tWHCS	-15	2			ns
		-10	2			
		-9	2			
		-8	1			
		-60	1			
		-50	1			
		-45	1			
Write Disable Time	tWS	-15			8	ns
		-10			6	
		-9			6	
		-8			5	
		-60			4	
		-50			4	
		-45			4	
Write Recovery Time	tWR	-15			10	ns
		-10			10	
		-9			10	
		-8			8	
		-60			6	
		-50			5	
		-45			4,5	

AC Characteristics (Count.)

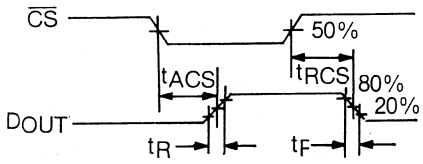
Rise and Fall Times

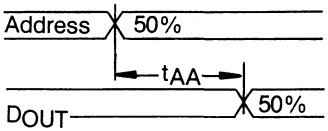
Parameter	Symbol	Grade ②	Min	Typ	Max	
Output Rise Time	t_R	-15		2		ns
		-10		2		
		-9		2		
		-8		2		
		-60		2		
		-50		2		
		-45		2		
Output Fall Time	t_F	-15		2		ns
		-10		2		
		-9		2		
		-8		2		
		-60		2		
		-50		2		
		-45		2		

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec. maintained.

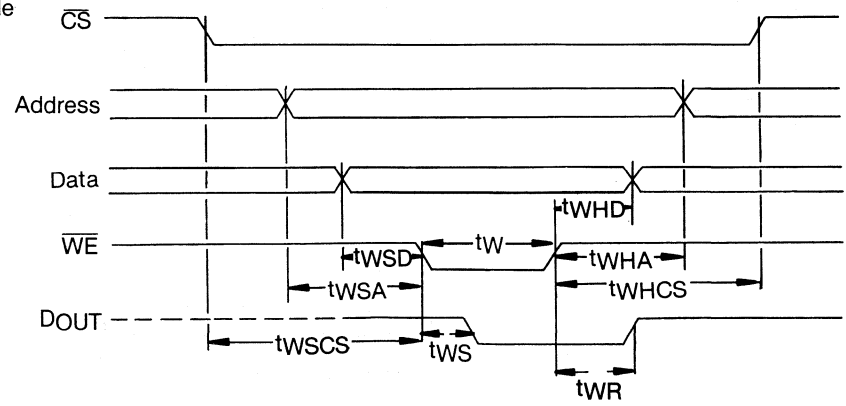
Timing Waveforms

Read Mode



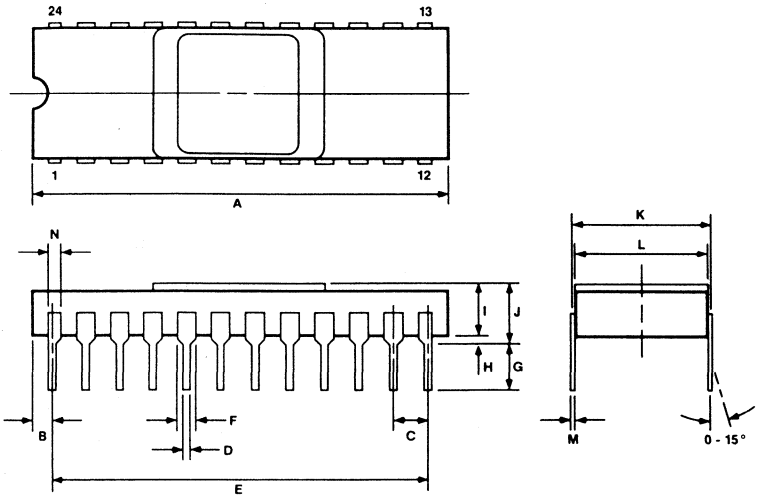


Write Mode



24-Pin Ceramic DIP

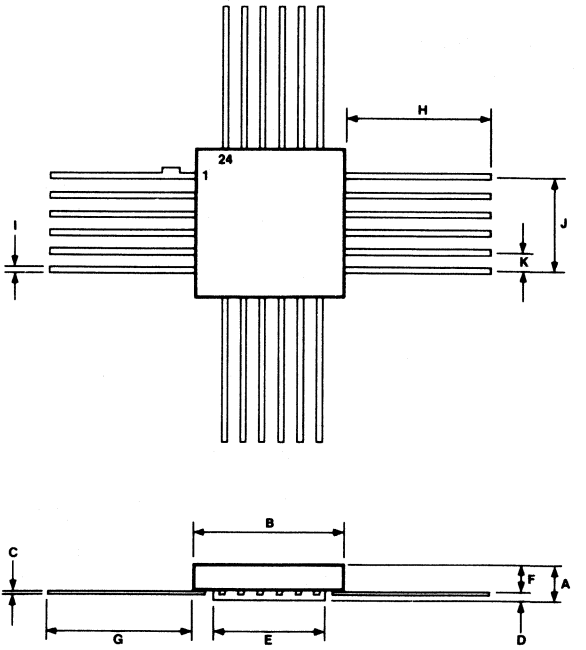
Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.46 ± .05
E	27.94
F	1.25 min
G	3.5 ± .3
H	.51 min
I	2.74
J	4.57 max
K	10.16 [TP]
L	10.0
M	.25 ± .05
N	1.0 min



Package Dimensions (Cont.)

24-Pin Ceramic Flatpack

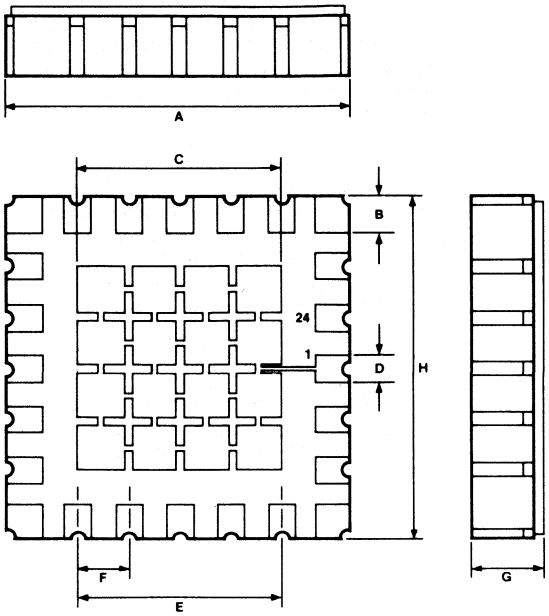
Item	Millimeters
A	2.6 max
B	9.5
C	.13
D	.5
E	6.9
F	2.0
G	8.9
H	8.9
I	.43
J	6.35
K	1.27



24 PIN Ceramic LCC

μPB100474K

Item	Millimeters
A	8.51
B	.89
C	5.14
D	.64
E	5.08
F	1.27
G	1.76
H	8.51



Heat Sink/Thermal Characteristics of 100474K 2 W versions

As shown in Fig. 1, thermal resistance of 100474K (2W, LCC) is conjectured as follows:

thermal resistance of LCC PKG: 4 deg C/W
thermal resistance of mother board: 3 deg C/W

Therefore, thermal resistance between the surface of die (junction) and the under surface of mother board is estimated to be approximately 7 deg C/W.
And termal rising is calulated as follows:

(7 deg C/W x (2W) = 14 deg C

Fig. 2 shows mother board idea of LCC. It is recommended that 4 pcs or 8 pcs of 100474K are mounted on one mother board.

4 pcs mounted: 6.5 W typ/8W max
8 pcs mounted: 13 W typ/16W max

In order to keep the junction temperature below 90 deg C, following thermal resistance is required per board.

mother board with 4 pcs of LCC:
thermal resistance (90°C – 14°C – 25°C)/8W = 6.4°C/W

mother board with 8 pcs of LCC:
thermal resistance (90°C – 14°C – 25°C)/16W = 3.2°C/W

It is considered that these figures can be obtained by FINs of 23 mm x 30 x mm, which are attached under the mother board.

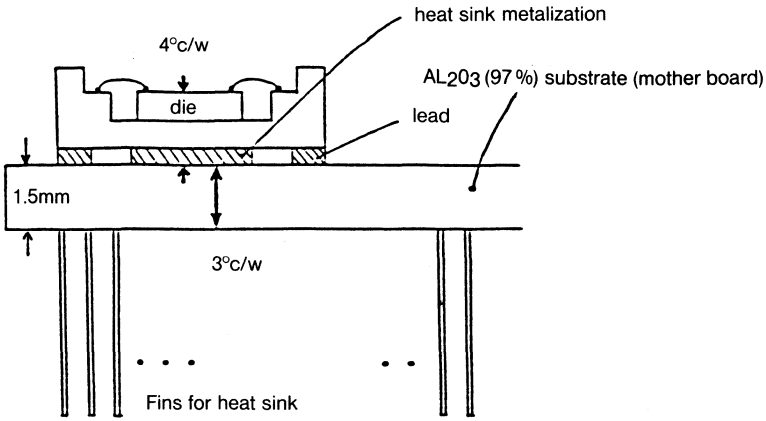
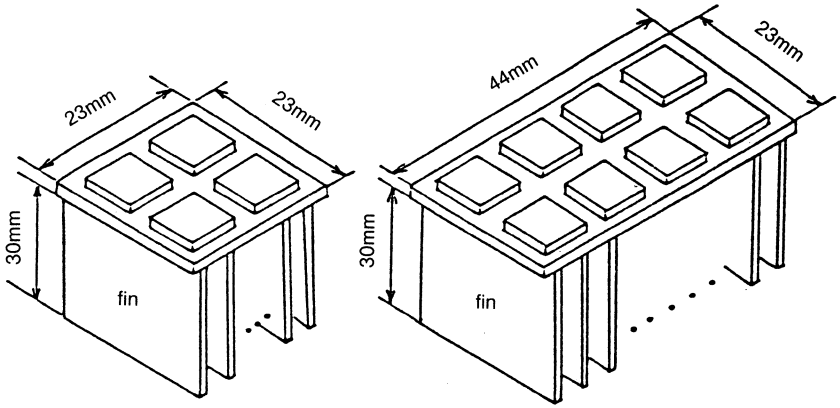


Fig. 1 Cross section of LCC and mother board



(1) 6.4 w typ/pkg
8 w max/pkg

(2) 13 w typ/pkg
16 w max/pkg

Fig. 2 mother board idea for LCC

BIPOLAR PROMs

256 BIT BIPOLAR TTL
PROGRAMMABLE READ ONLY MEMORY

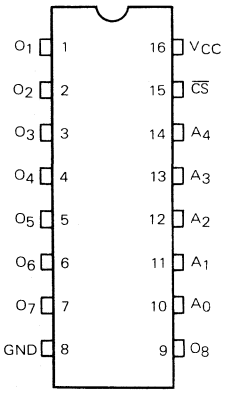
Description

The μPB400C, μPB400D, μPB410C and μPB410D are high speed, electrically programmable, fully decoded 256 bit TTL read only memories. On-chip address decoding, chip select input and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB400C, μPB400D, μPB410C and μPB410D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 32 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 30 ns MAX. (μPB400-1, μPB410-1)
- Medium power consumption: : 350 mW TYP.
- A chip select input for memory expansion
- Open-Collector outputs (μPB400C, μPB400D)/Three-state outputs (μPB410C, μPB410D)
- Cerdip 16-Lead Dual In-Line Package (μPB400D, μPB410D)
- Plastic 16-Lead Dual In-Line Package (μPB400C, μPB410C)
- Fast Programming time : 200μs/bit TYP.
- Replaceable with : Harris' HM7602/7603, MMI's 63S080/081 and equivalent devices (as a ROM)

Connection Diagram (Top View)



PIN NAMES

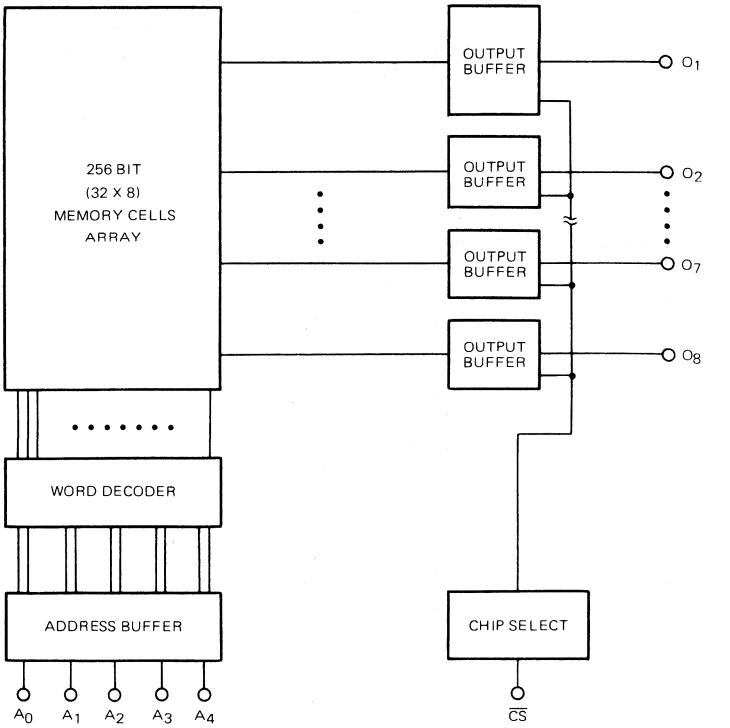
$A_0 \sim A_4$	: Address Inputs
$O_1 \sim O_8$	: Data Outputs
$\overline{CS}$	: Chip Select Input (Active Low)
V_{CC}	: Power Supply (+5 V)
GND	: Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Select input $\overline{CS}$ must be a logical one in order to disable the outputs. Second, the desired word is selected by the five address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, the Chip Select input must be a logical zero. The outputs then correspond to the data programmed in the selected words. When the Chip Select input is a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		60	100	mA	All Inputs Grounded.	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

* **Note:** Applicable to μPB410C and μPB410D.

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	μPB400C-1, μPB410C-1 μPB400D-1, μPB410D-1		μPB400C, μPB410C μPB400D, μPB410D		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		30		35	ns
Chip Select Access Time	t_{ACS}		20		25	ns
Chip Select Disable Time	t_{DCS}		20		25	ns

Note 1. Output Load: See Fig. 1.

Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.

Note 3. Measurement References: 1.5 V for both inputs and outputs.

Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

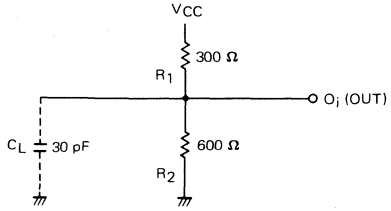


Fig. 1

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB400C, μPB400D, μPB410C and μPB410D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met,,four additional pulses are applied and the pulse train, then the sense current is terminated.

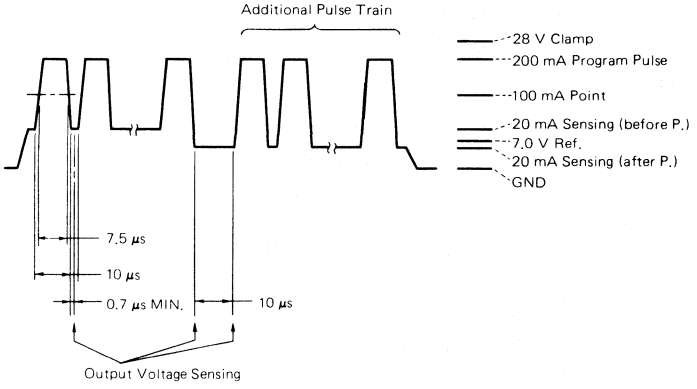
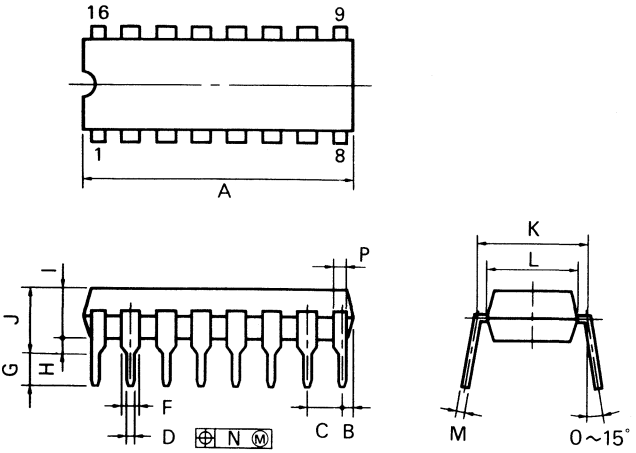


Fig. 2 Typical Output Voltage Waveform.

Package Dimensions

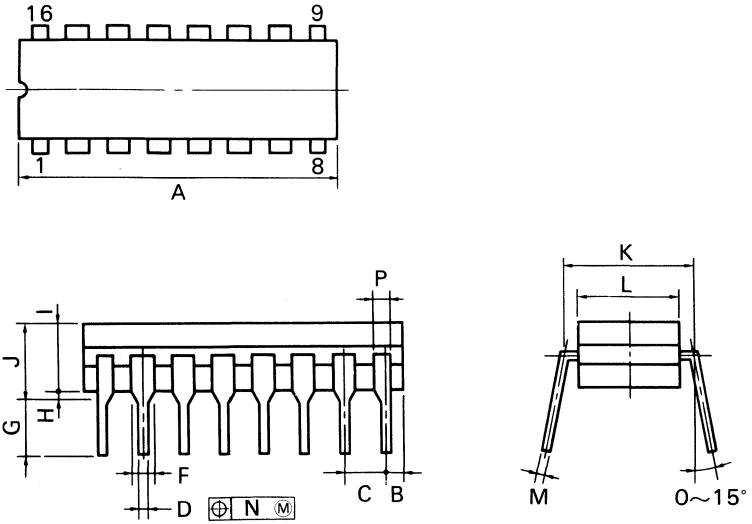
16PIN Plastic DIP

ITEM	MILLIMETERS
A	20.32 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.50^{\pm 0.10}$
F	1.2 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	1.0 MIN.



16PIN Cerdip DIP (300 mil)

ITEM	MILLIMETERS
A	20.32 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.46^{\pm 0.05}$
F	1.42 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	3.70
J	5.08 MAX.
K	7.62 (T.P.)
L	6.75
M	$0.25^{\pm 0.05}$
N	0.25
P	0.89 MIN.



1024 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

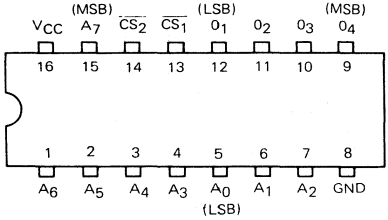
Description

The μPB403C, μPB403D, μPB423C and μPB423D are high speed, electrically programmable, fully decoded 1024 bit TTL read only memories. On-chip address decoding, two chip select inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB403C, μPB403D, μPB423C and μPB423D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 256 WORDS x 4 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 35 ns MAX. (μPB403-2, μPB423-2)
- Medium power consumption : 400mW TYP.
- Two chip select inputs for memory expansion
- Open-Collector outputs (μPB403C, μPB403D)/Three-state outputs (μPB423C, μPB423D)
- Cerdip 16-Lead Dual In-Line Package (μPB403D, μPB423D)
- Plastic 16-Lead Dual In-Line Package (μPB403C, μPB423C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : Signetics' 82S126/129, Harris' HM7610/7611 and equivalent devices (as a ROM)

Connection Diagram (Top View)



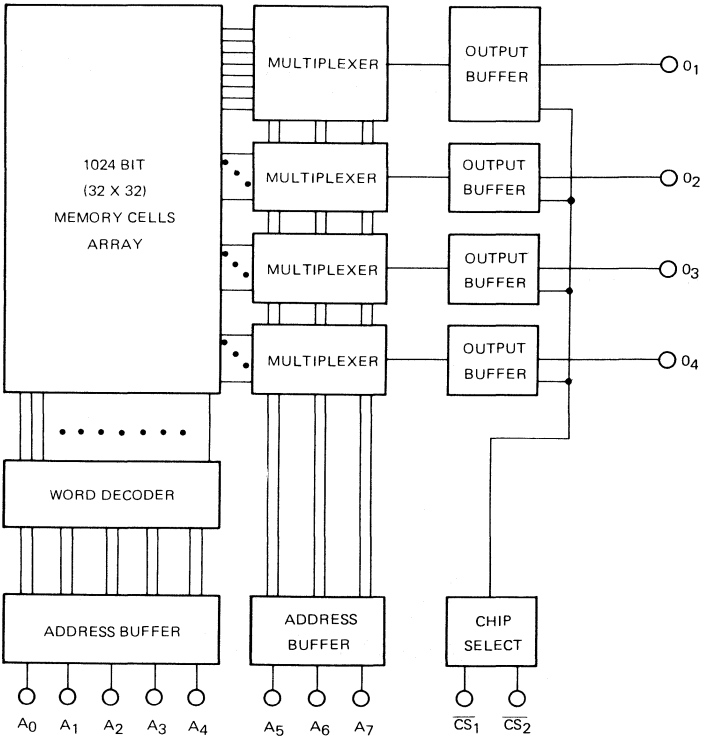
Pin names
A_0-A_7 : Address Inputs
O_1-O_4 : Data Outputs
$\overline{CS_1}$, $\overline{CS_2}$: Chip Select Inputs
V_{CC} = Power Supply (+5V)
GND = Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the eight address inputs in TTL levels. Either or both of the two chip select inputs should be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

Connection Diagram (Top View)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
	Input High Voltage	V_{IH}	2.0			V		
	Input Low Voltage	V_{IL}			0.85	V		
	Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
	Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
	Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
	Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
	Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
	Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
	Power Supply Current	I_{CC}		80	130	mA	All Inputs Grounded	V_{CC}=5.5 V
*	Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
*	Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

* Note: Applicable to μPB423C and μPB423D.

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	μPB403C-2, μPB423C-2, μPB403D-2, μPB423D-2		μPB403C-1, μPB423C-1, μPB403D-1, μPB423D-1		μPB403C, μPB423C, μPB403D, μPB423D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		35		45		60	ns
Chip Select Access Time	t_{ACS}		25		30		35	ns
Chip Select Disable Time	t_{DCS}		25		30		35	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

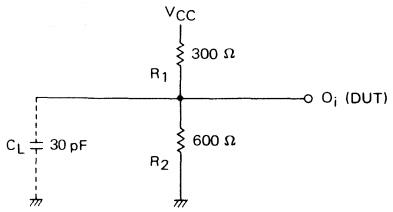


Fig. 1

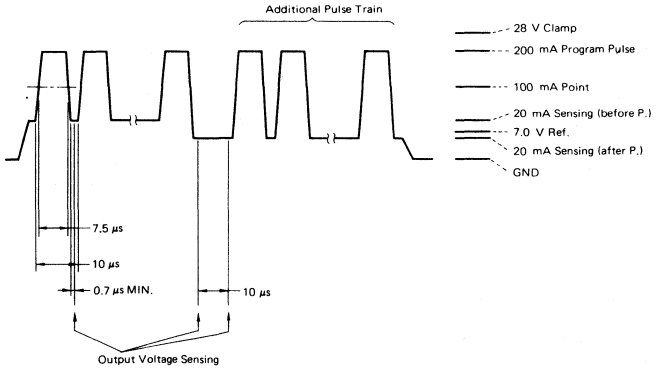
PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB403C, μPB403D, μPB423C and μPB423D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

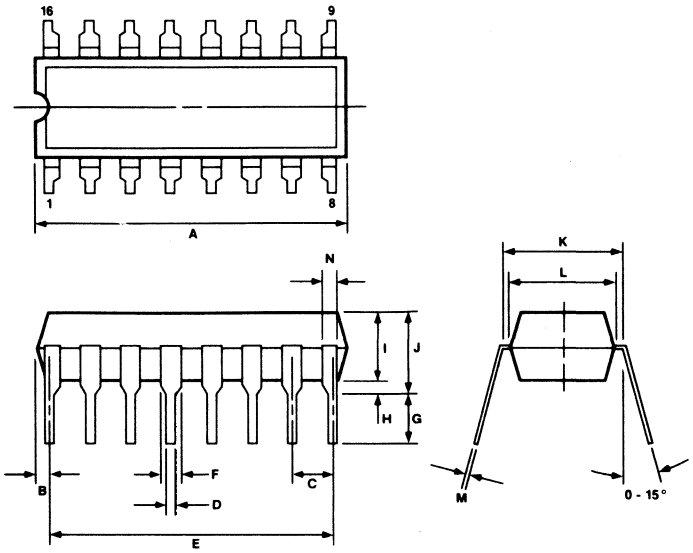
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

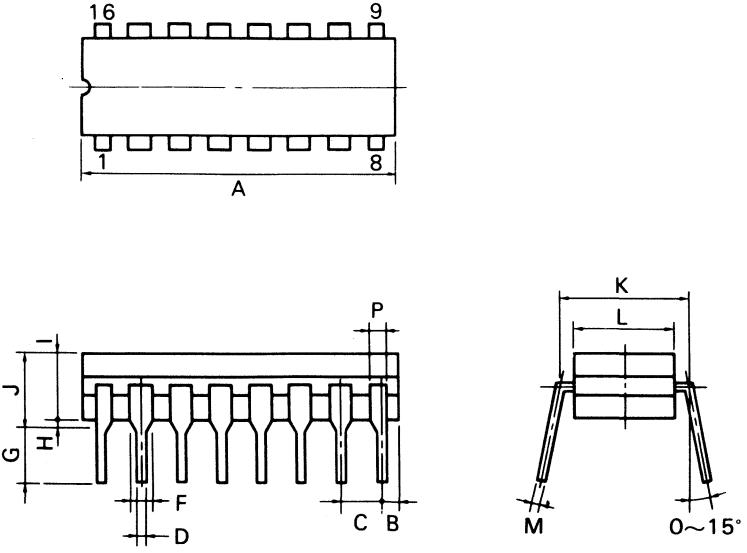
16PIN Plastic DIP (300 mil)

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.5 ± .03
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



16PIN Cerdip DIP (300 mil)

ITEM	MILLIMETERS
A	20.32 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.46^{\pm 0.05}$
F	1.42 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	3.70
J	5.08 MAX.
K	7.62 (T.P.)
L	6.75
M	$0.25^{\pm 0.05}$
N	0.25
P	0.89 MIN.



2048 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

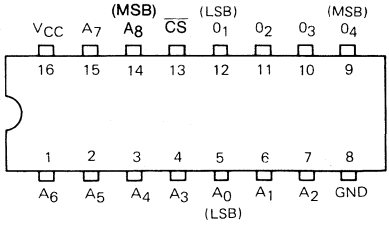
Description

The μPB412C and μPB412D are high speed, electrically programmable, fully decoded 2048 bit TTL read only memories. On-chip address decoding, one chip select input and three-state outputs allow easy expansion of memory capacity. The μPB412C and μPB412D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 512 WORDS x 4 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 35 ns MAX. (μPB412-1)
- Medium power consumption : 400 mW TYP.
- One chip select input for memory expansion
- Three-state outputs
- Cerdip 16-Lead Dual In-Line Package (μPB412D)
- Plastic 16-Lead Dual In-Line Package (μPB412C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : MMi's 63S241, Harris' HM7621 and equivalent devices (as a ROM)

Connection Diagram (Top View)



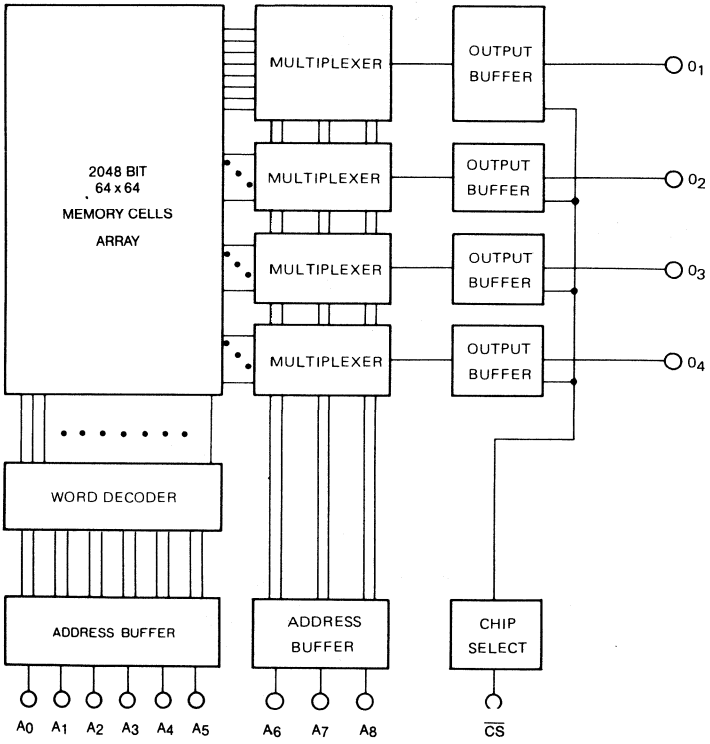
Pin names:
A0 to A8 : Address Inputs
O1 to O4 : Data Outputs
$\overline{CS}$: Chip Select Input
VCC : Power Supply (+5V)
GND : Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Select input $\overline{CS}$ must be a logical one in order to disable the outputs. Second, the desired word is selected by the address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, the Chip Select input should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When the chip select input is at logic one (high), all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		80	130	mA	All Inputs Grounded	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to 75°C)

Characteristic	Symbol	412C/D-1		412C/D		Unit
		min.	max.	min.	max.	
Address Access Time	t_{AA}		35		45	ns
Chip Select Access Time	t_{ACS}		25		30	ns
Chip Select Disable Time	t_{DCS}		25		30	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

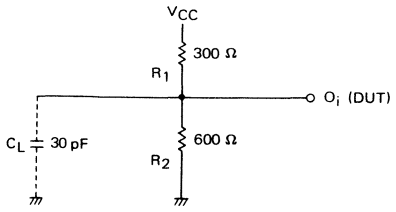


Fig. 1

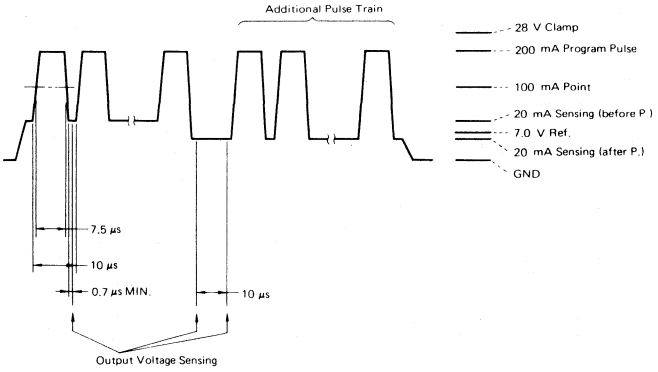
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB412C and 412D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

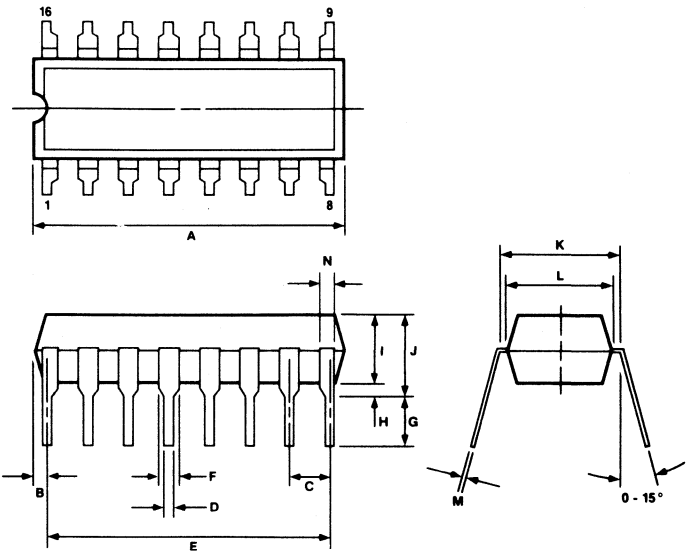
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

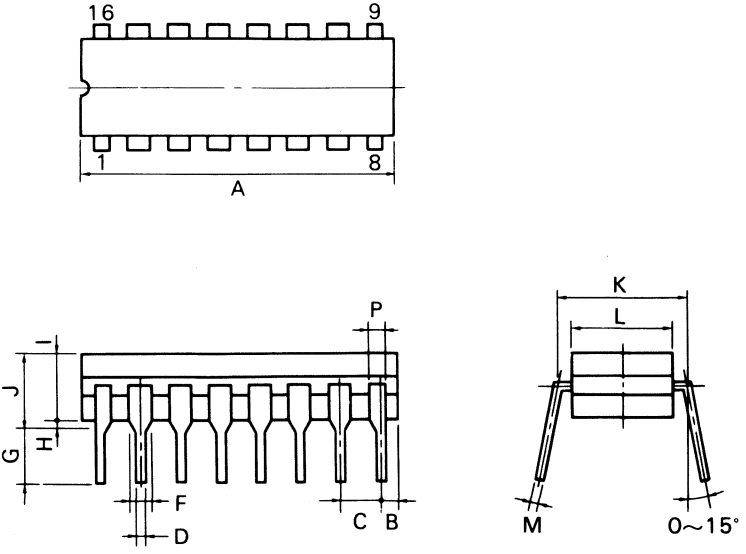
16 PIN Plastic DIP (300 mil)

Item	Millimeters
A	20.32 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	17.78
F	1.2 min
G	3.5 ± .03
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



16 PIN Cerdip DIP (300 mil)

ITEM	MILLIMETERS
A	20.32 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.46^{+0.05}$
F	1.42 MIN.
G	$3.5^{+0.3}$
H	0.51 MIN.
I	3.70
J	5.08 MAX.
K	7.62 (T.P.)
L	6.75
M	$0.25^{+0.05}$
N	0.25
P	0.89 MIN.



2048 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

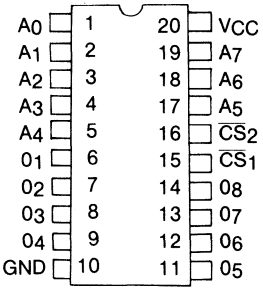
Description

The μPB421C and μPB421D are high speed, electrically programmable, fully decoded 2048 bit TTL read only memories. On-chip address decoding, two chip select inputs and three-state outputs allow easy expansion of memory capability. The μPB421C and μPB421D are fabricated with logic level zero (low); logic level one High) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 256 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 40 ns MAX. (μPB421-1)
- Medium power consumption : 500 mW TYP.
- Two chip select inputs for memory expansion
- Three-state outputs
- Cerdip 20-Lead Dual In-Line Package (μPB421D)
- Plastic 20-Lead Dual In-Line Package (μPB421C)
- Fast programming time : 200 μs/bit TYP.
- Compatibility with : MMI's 6309 and equivalent devices (as a ROM)

Connection Diagram (Top View)



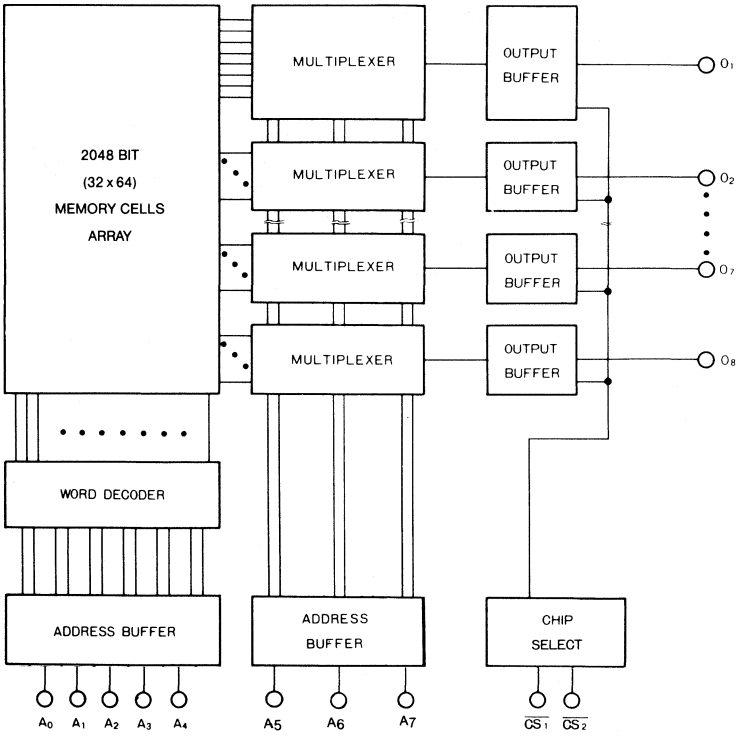
A0 to A7 : Address Inputs
O1 to O8 : Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$: Chip Select Inputs (Active Low)
VCC : Power Supply (+5V)
GND : Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the eight address inputs in TTL levels. Either or both of the Chip Select inputs should be at a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, both of the two Chip Select inputs must be held at a logical zero. The outputs then correspond to the data programmed in the selected words. When either or both of the two Chip Select inputs are at a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature (Cerdip Package)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic Package)	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		90	140	mA	All Inputs Grounded.	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75°C)

Characteristic	Symbol	μPB421C/D-1		μPB421C/D		Unit
		min.	max.	min.	max.	
Address Access Time	tAA		40		50	ns
Chip Select Access Time	tACS		30		30	ns
Chip Select Disable Time	tDCS		30		30	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

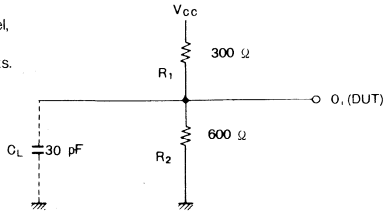


Fig. 1

Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB421C and μPB421D. NEC will not accept responsibilty for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

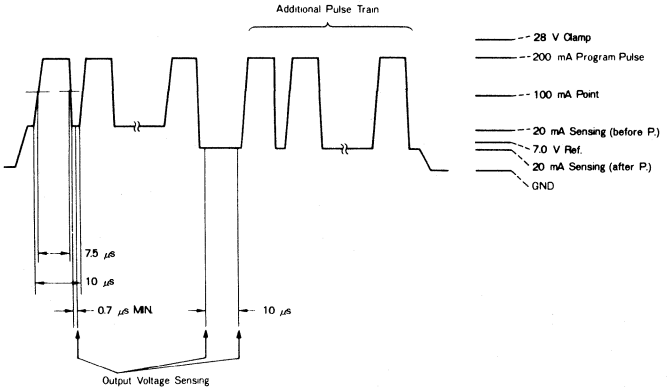
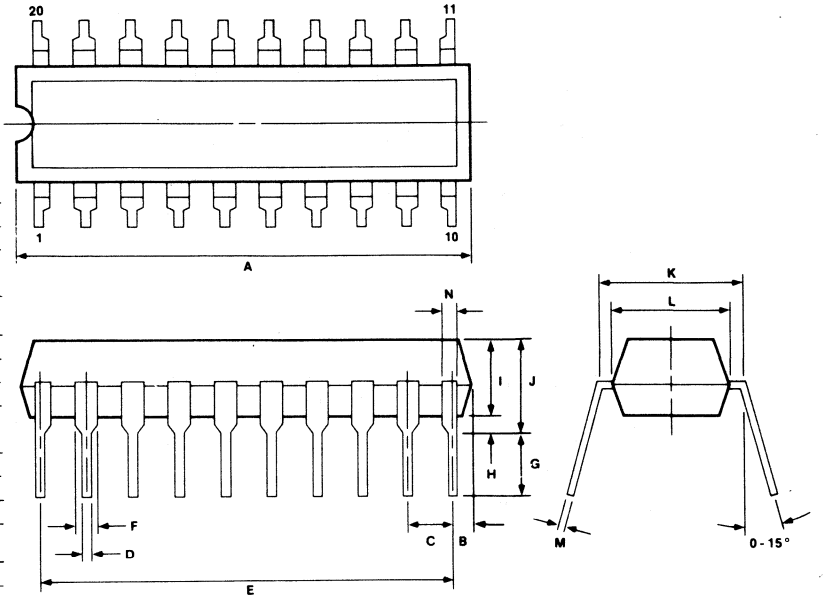


Fig. 2 Typical Output Voltage Waveform.

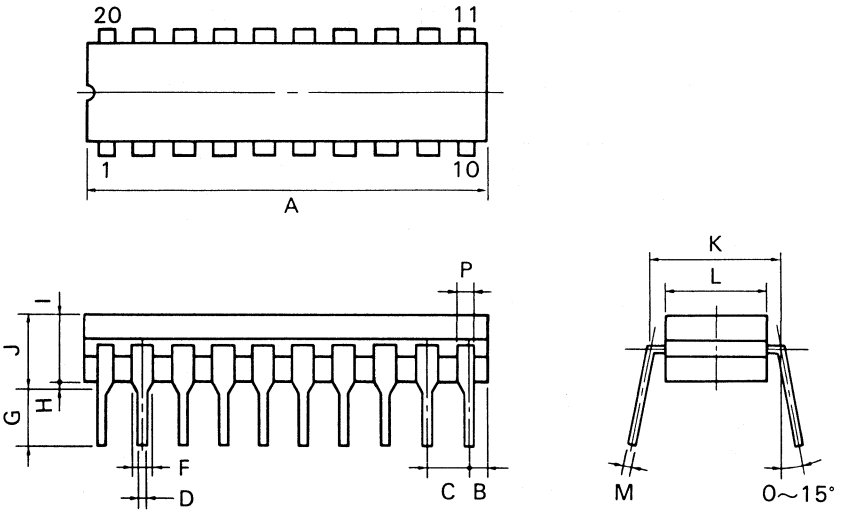
Package Dimensions

20PIN Plastic DIP



Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.1 min
G	3.5 ± .30
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	.9 min

Package Dimensions
20 PIN Cerdip (300mil)



ITEM	MILLIMETERS
A	25.40 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.46^{\pm 0.05}$
F	1.42 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	3.95
J	5.08 MAX.
K	7.62 (T.P.)
L	7.32
M	$0.25^{\pm 0.06}$
N	0.25
P	0.89 MIN.

4096 BIT BIPOLAR TTL
PROGRAMMABLE READ ONLY MEMORY

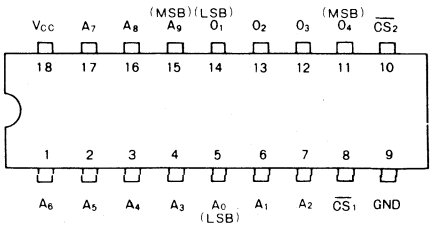
Description

The μPB406C, μPB406D, μPB426C and μPB426D are high speed electrically programmable fully decoded 4096 bit TTL read only memories. On-chip address decoding, two chip select inputs and open-collector / three-state outputs allow easy expansion of memory capacity. The μPB406C, μPB406D, μPB426C and μPB426D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 1024 WORDS x 4 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time : 35 ns MAX. (μPB406-3, μPB426-3)
- Medium Power Consumption : 500 mW TYP.
- Two Chip Select Inputs for Memory Expansion
- Open-Collector Output (μPB406C, μPB406D) / Three-State Outputs (μPB426C, μPB426D)
- Cerdip 18-Lead Dual In-Line Package (μPB406D, μPB426D)
- Plastic 18-Lead Dual In-Line Package (μPB406C, μPB426C)
- Fast Programming Time : 200 μs/bit TYP.
- Compatibility with : Signetics' 82S136 / 137, Harris' HPROM HM-7642 / 7643 and Equivalent Devices (as a ROM)

Connection Diagram (Top View)



Pin names

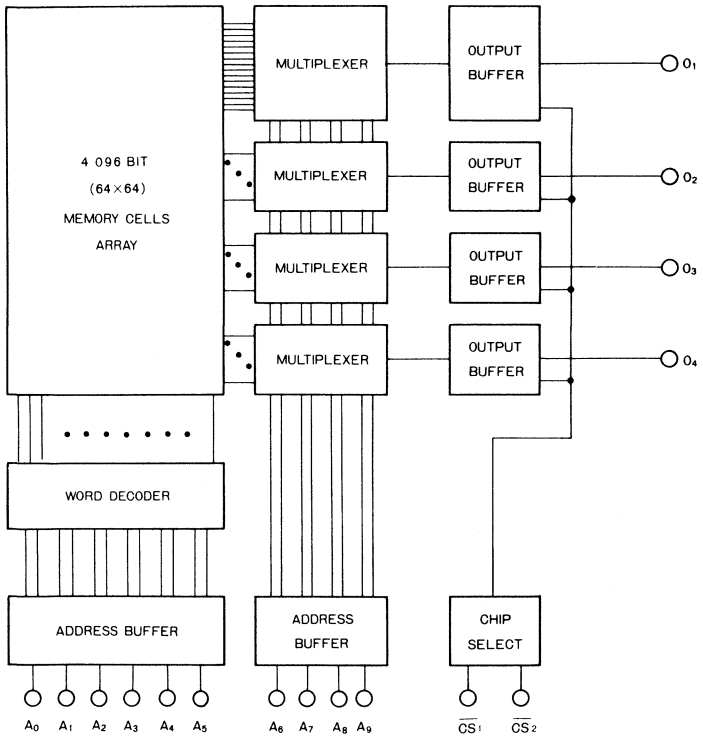
A_0–A_9	: Address Inputs
$\overline{O_1}$–$\overline{O_4}$	: Data Outputs
$\overline{CS_1}$, CS_2	: Chip Select Inputs
V_{CC}	: Power Supply (+5V)
GND	: Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs should be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature (Cerdip Package)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic Package)	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5to 5.5 V, T_a=0 to 75 °C)

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	Input High Voltage	V_{IH}	2.0			V	
	Input Low Voltage	V_{IL}			0.8	V	
	Input High Current	I_{IH}			40	μA	V_I=5.5 V V_{CC}=5.5 V
	Input Low Current	$-I_{IL}$			0.5	mA	V_I=0.4 V V_{CC}=5.5 V
	Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA V_{CC}=5.5 V
	Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V V_{CC}=5.5 V
	Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V V_{CC}=5.5 V
	Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA V_{CC}=4.5 V
	Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded. V_{CC}=5.5 V
*	Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA V_{CC}=4.5 V
*	Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V

* Note : Applicable to μPB426C and μPB426D.

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to 75 °C)

CHARACTERISTIC	SYMBOL	μPB406C-3, μPB406D-3 μPB426C-3, μPB426D-3		μPB406C-2, μPB406D-2 μPB426C-2, μPB426D-2		μPB406C-1, μPB406D-1 μPB426C-1, μPB426D-1		μPB406C, μPB406D μPB426C, μPB426D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		35		50		60		70	ns
Chip Select Access Time	t_{ACS}		25		30		40		45	ns
Chip Select Disable Time	t_{DCS}		25		30		40		45	ns

Note 1. Output Load : See Fig. 1.
Note 2. Input Waveform : 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References : 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

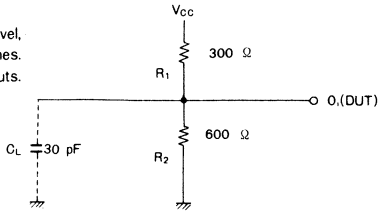


Fig. 1

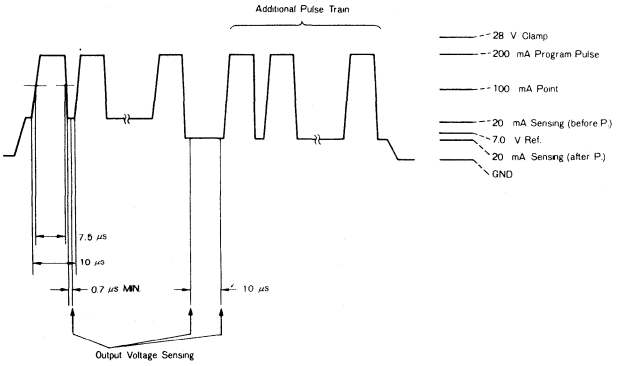
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB406C, μPB406D, μPB426C and μPB426D. NEC will not accept responsibility for any device found to be defective it it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5 %	μs	15 V point 150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point 150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

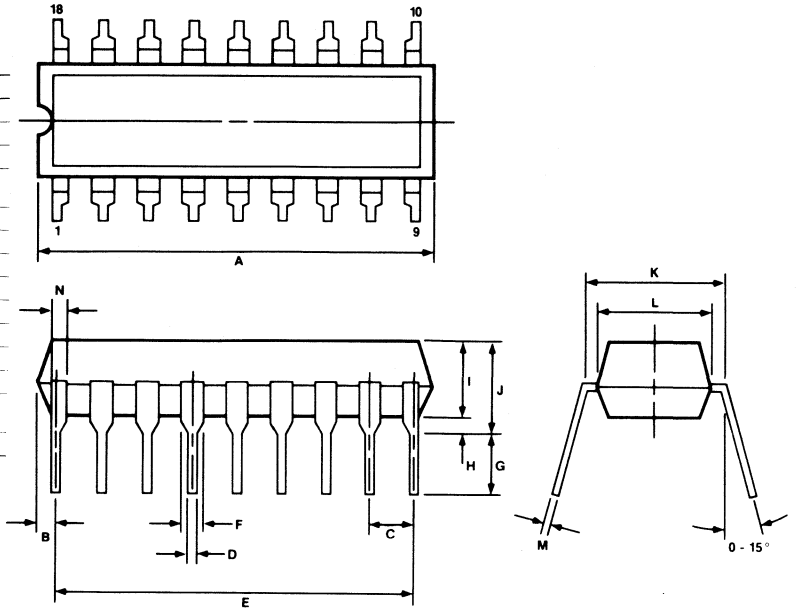
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

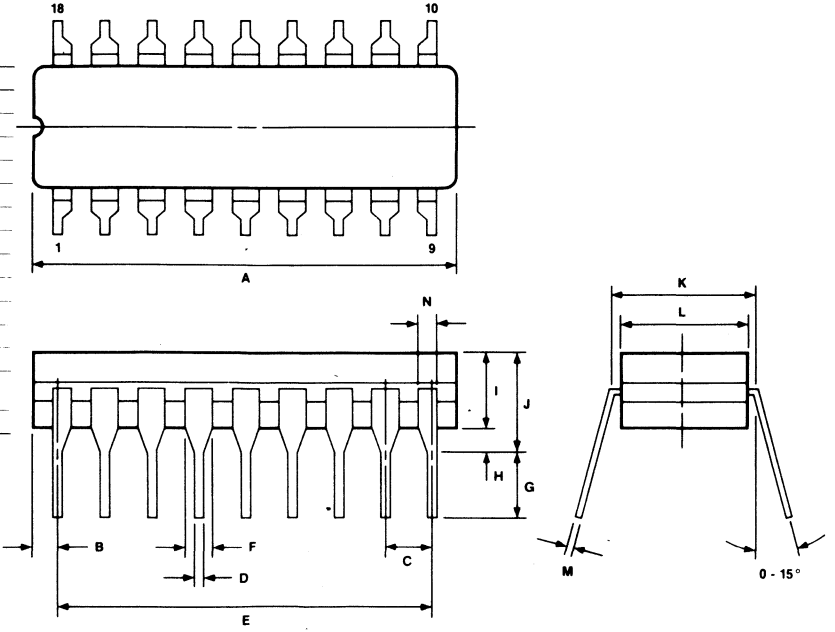
18PIN Plastic DIP

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.5 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



18PIN Cerdip

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.42 min
G	3.5 ± .3
H	.51 min
I	3.95
J	5.08 max
K	7.62 [TP]
L	6.60
M	.25 ± .05
N	.89 min



4096 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

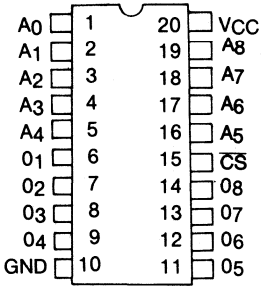
Description

The μPB424C and μPB424D are high speed, electrically programmable, fully decoded 4096 bit TTL read only memories. On-chip address decoding, chip select input and three-state outputs allow easy expansion of memory capacity. μPB424C and μPB424D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 512 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 40 ns MAX. (μPB424-1)
- Medium power consumption : 500 mW TYP.
- A chip select input for memory expansion
- Three-state outputs
- Plastic 20-Lead Dual In-Line Package (μPB424C)
- Cerdip 20-Lead Dual In-Line Package (μPB424D)
- Fast programming time : 200 μs / bit TYP.
- Replaceable with : MMI's 63S481, Harris' HM7649 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names:

A0 to A8	: Address Inputs
$\overline{O1}$ to $\overline{O8}$	: Data Outputs
$\overline{CS}$	: Chip Select Inputs (Active Low)
VCC	: Power Supply (+5V)
GND	: Ground

Operation

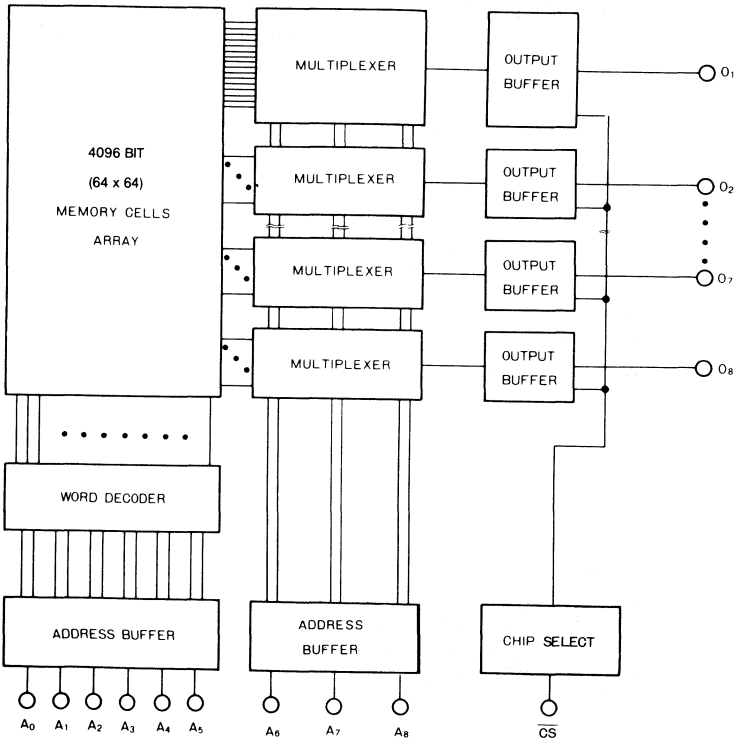
1. Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Select input $\overline{CS}$ must be a logical one in order to disable the outputs. Second, the desired word is selected by the nine address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading

To read the memory, the Chip Select input must be a logical lero. The outputs then correspond to the data programmed in the selected words. When the Chip Select input is a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	V_{CC}	−0.5 to +7.0	V
INPUT VOLTAGE	V_I	−0.5 to +5.5	V
OUTPUT VOLTAGE	V_O	−0.5 to +5.5	V
OUTPUT CURRENT	I_O	50	mA
OPERATING TEMPERATURE	T_{opt}	−25 to +75	°C
STORAGE TEMPERATURE			
CERDIP PACKAGE	T_{stg}	−65 to +150	°C
PLASTIC PACKAGE	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75°C)

Characteristic	Symbol	μPB424C/D-1		μPB424C/D		Unit
		min.	max.	min.	max.	
Address Access Time	t_{AA}		40		50	ns
Chip Select Access Time	t_{ACS}		30		30	ns
Chip Select Disable Time	t_{DCS}		30		30	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

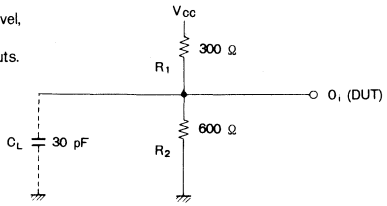


Fig. 1

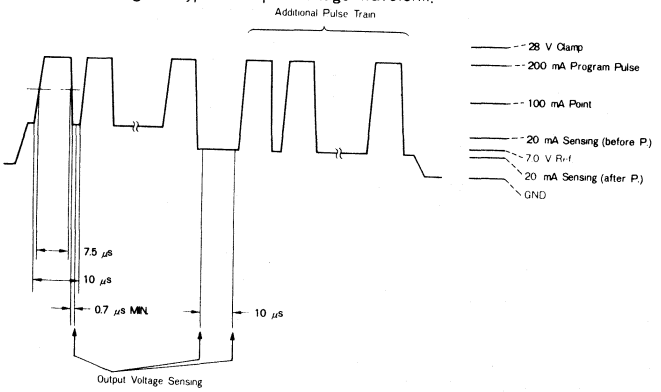
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB424C and μPB424D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

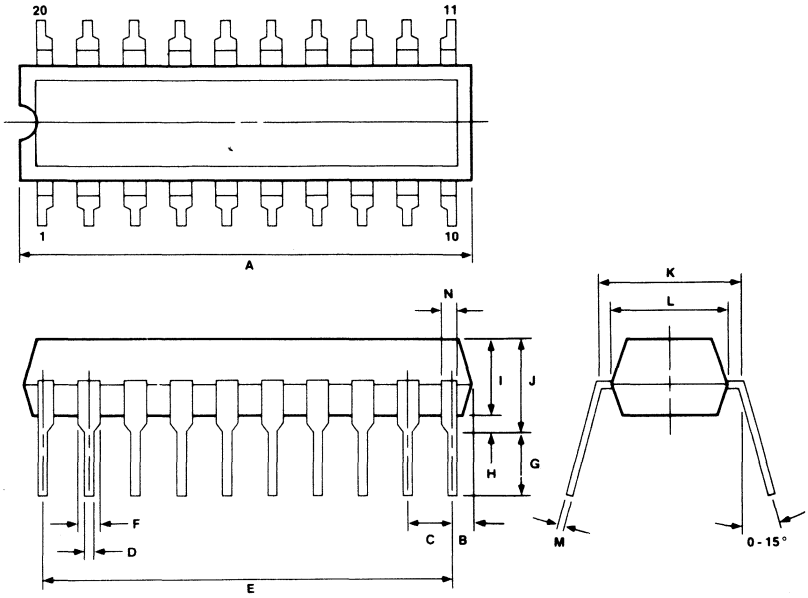
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

20PIN Plastic DIP

Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.1 min
G	3.5 ± .30
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	.9 min



4096 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

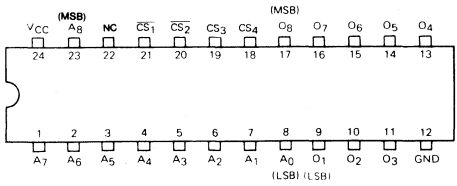
Description

The μPB405C, μPB405D, μPB425C and μ425D are high speed, electrically programmable, fully decoded 4096 bit TTL read only memories. On-chip address decoding, four chip select inputs and open-collector / three-state outputs allow easy expansion of memory capability. The μPB405C, μPB405D, μPB425C and μPB425D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 512 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read acces time : 40 ns MAX. (μPB405-2, μPB425-2)
- Medium power consumption : 500 mW TYP.
- Four chip select inputs for memory expansion
- Open-Collector outputs (μPB405C, μPB405D) / Three-state outputs (μPB425C, μPB425D)
- Cerdip 24-Lead Dual In-Line Package (μPB405D, μPB425D)
- Plastic 24-Lead Dual In-Line Package (μPB405C, μPB425C)
- Fast programming time : 200 μs/bit TYP.
- Compability with : Signetics' 82S140/141, Harris' HPROM HM-7640/7641 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

A0 - A8	: Address Inputs
O1 - O8	: Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	: Chip Select Inputs
NC	: No Connection
VCC	: Power Supply (+5V)
GND	: Ground

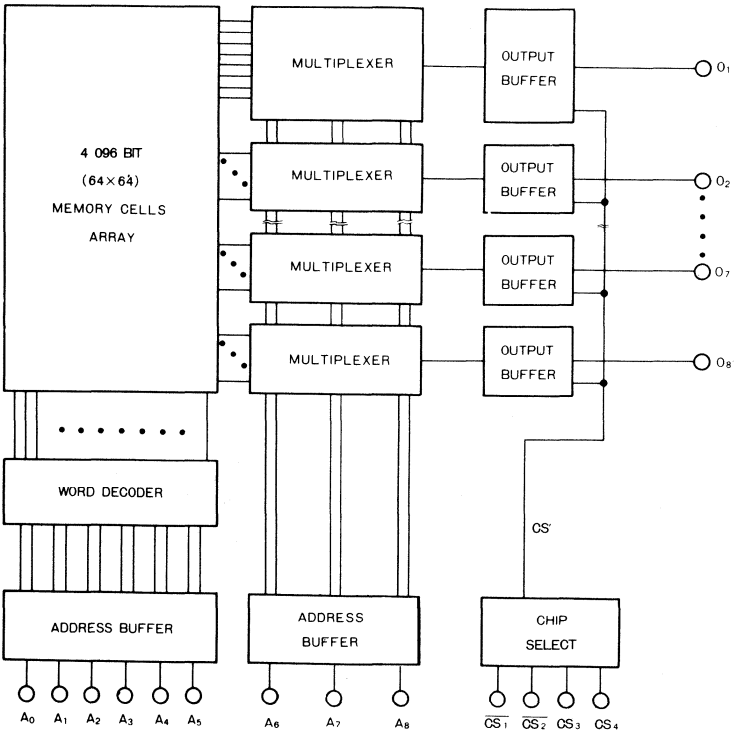
Operation

First we define an internal Chip Select logic by four Chip Select inputs:
$CS' = \overline{CS}_1 + \overline{CS}_2 + \overline{CS}_3 \cdot \overline{CS}_4$
That is, CS' is a logical zero (low) if and only if $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$, While CS' is a logical one (high) in all the other cases.

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the nine address inputs in TTL levels.
The four Chip Select inputs must be set so thatCS' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, the four Chip Select inputs must be set so that CS' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Select inputs are set so that CS' becomes a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature (Cerdip Package)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic Package)	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
	Input High Voltage	V_{IH}	2.0			V		
	Input Low Voltage	V_{IL}			0.85	V		
	Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
	Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
	Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
	Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
	Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
	Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
	Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded.	V_{CC}=5.5 V
*	Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
*	Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

*Note : Applicable to μPB425C, μPB425D

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	μPB405C-2, μPB425C-2 μPB405D-2, μPB425D-2		μPB405C-1, μPB425C-1 μPB405D-1, μPB425D-1		μPB405C, μPB425C μPB405D, μPB425D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		40		50		60	ns
Chip Select Access Time	t_{ACS}		30		30		40	ns
Chip Select Disable Time	t_{DCS}		30		30		40	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

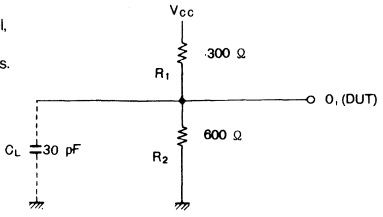


Fig. 1

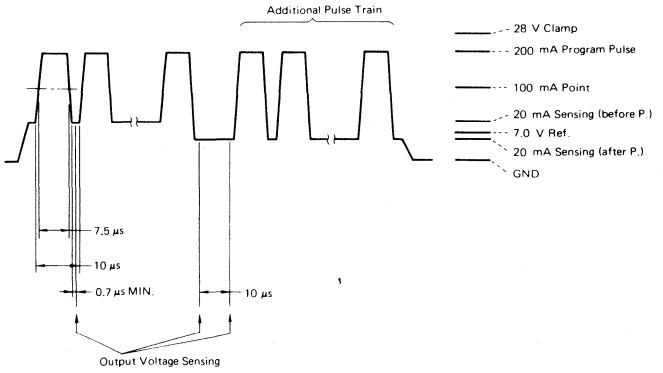
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB405C, μPB405D, μPB425C and μPB425D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

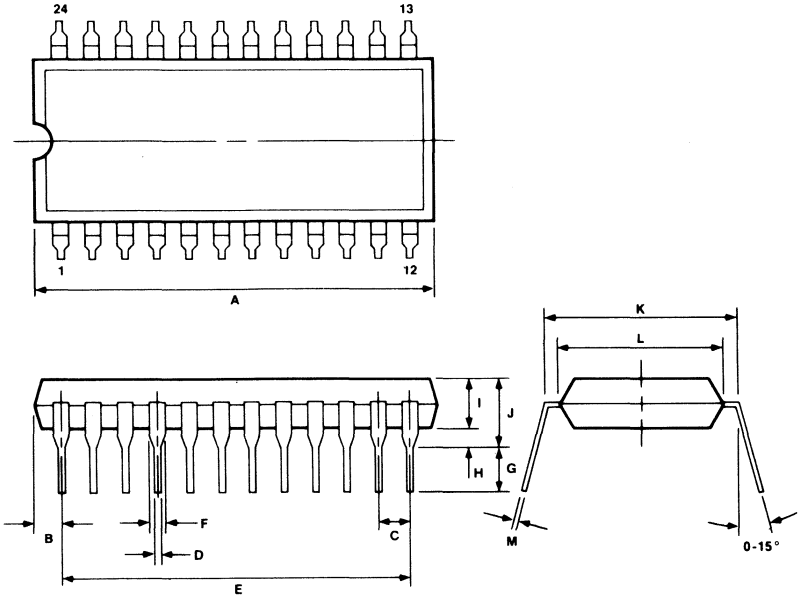
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

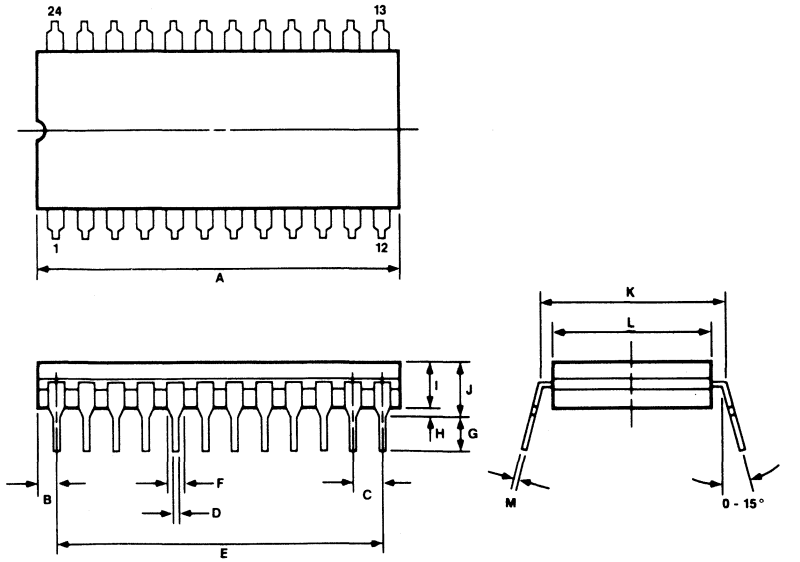
24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



8192 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

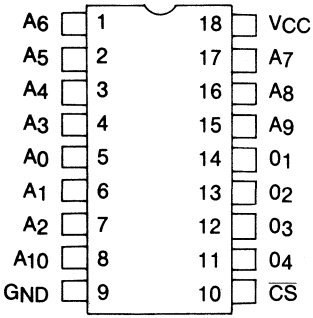
Description

The μPB427C and μPB427D are high speed, electrically programmable, fully decoded 8192 bit TTL read only memories. On-chip address decoding, chip select input and three-state outputs allow easy expansion of memory capacity. μPB427C and μPB427D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 2048 WORDS x 4 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 45 ns MAX. (μPB427-1)
- Medium power consumption : 500 mW TYP.
- A chip select input for memory expansion
- Three-state outputs
- Plastic 18-Lead Dual In-Line Package (μPB427C)
- Cerdip 18-Lead Dual In-Line Package (μPB427D)
- Fast programming time : 200 μs/bit TYP.
- Replaceabel with : MMI's 63S841, Harris' HM7685 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

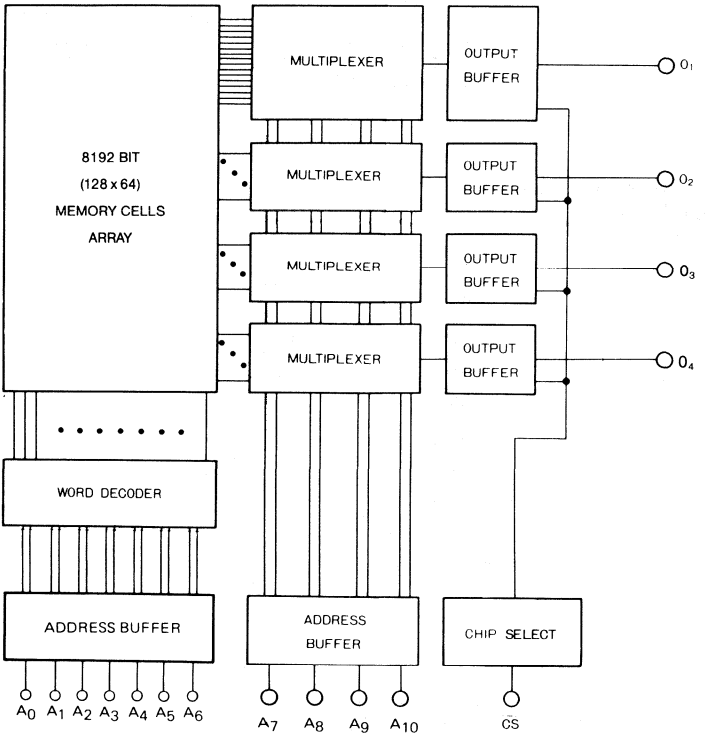
A_0 to A_{10}	: Address Inputs
O_1 to O_4	: Data Outputs
$\overline{CS}$	: Chip Select Input
V_{CC}	: Power Supply (+5V)
GND	: Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Select input $\overline{CS}$ must be a logical one in order to disable the outputs. Second, the desired word is selected by the eleven address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, the Chip Select input must be a logical zero. The outputs then correspond to the data programmed in the selected words. When the Chip Select input is a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	V_{CC}	−0.5 to +7.0	V
INPUT VOLTAGE	V_I	−0.5 to +5.5	V
OUTPUT VOLTAGE	V_O	−0.5 to +5.5	V
OUTPUT CURRENT	I_O	50	mA
OPERATING TEMPERATURE	T_{opt}	−25 to +75	°C
STORAGE TEMPERATURE			
CERDIP PACKAGE	T_{stg}	−65 to +150	°C
PLASTIC PACKAGE	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0,5	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		90	140	mA	All Inputs Grounded	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O=0 V	

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75°C)

Characteristic	Symbol	μPB427C-1 μPB427D-1		μPB427C μPB427D		Unit
		min.	max.	min.	max.	
Address Access Time	t_{AA}		45		55	ns
Chip Select Access Time	t_{ACS}		25		30	ns
Chip Select Disable Time	t_{DCS}		25		30	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

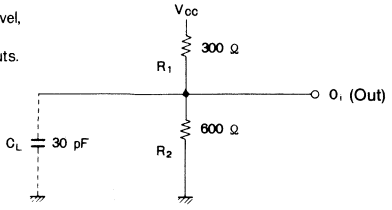


Fig. 1

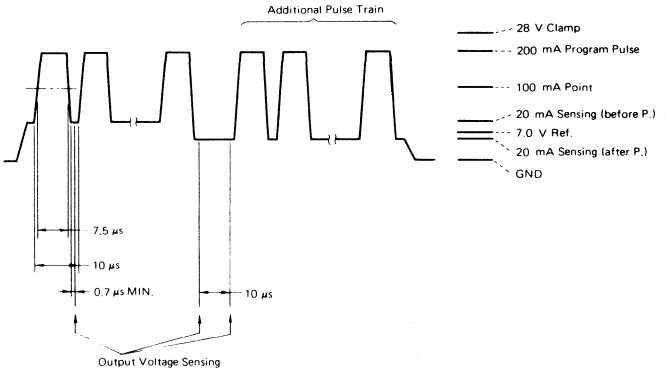
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB427C and μPB427D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

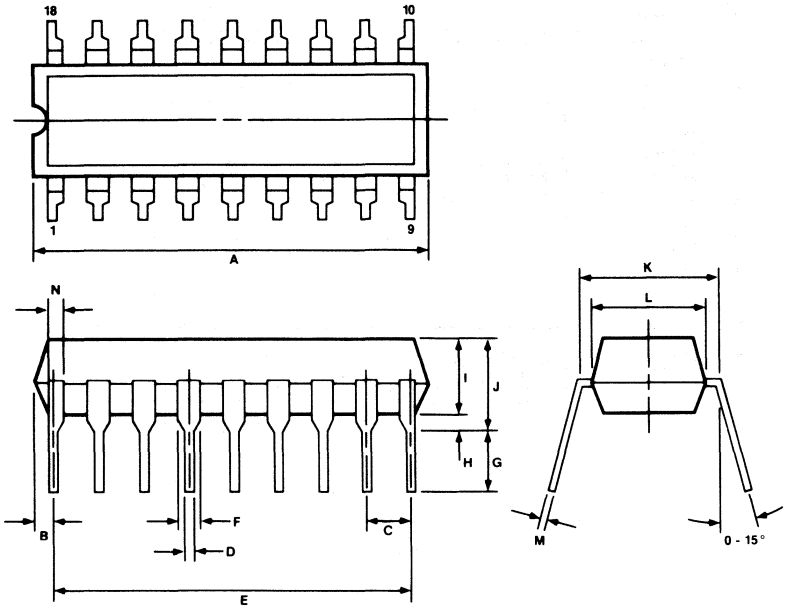
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

18PIN Plastic DIP

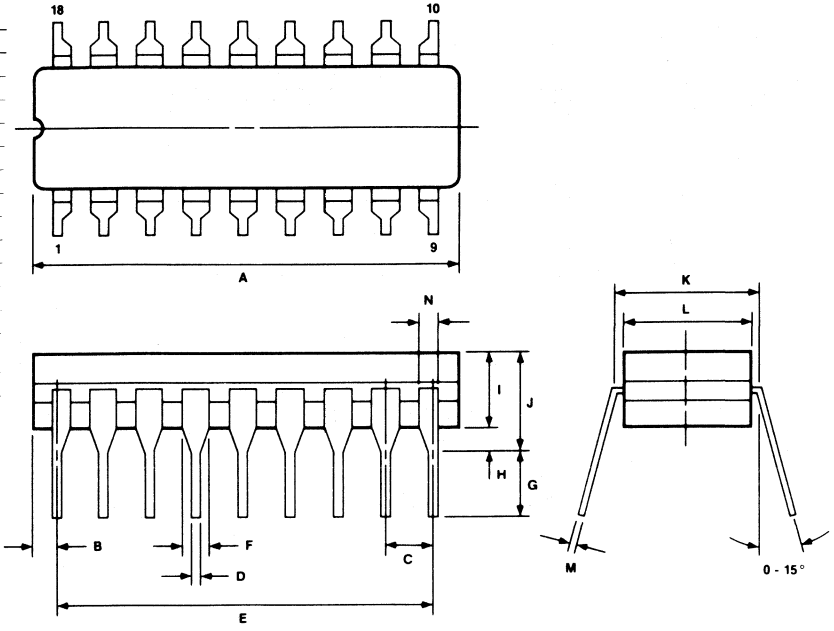
Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	20.32
F	1.2 min
G	3.5 ± .3
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	1.0 min



Package Dimension

18PIN Cerdip

Item	Millimeters
A	22.86 max
B	1.27 max
C	2.54 [TP]
D	.46 ± .05
E	20.32
F	1.42 min
G	3.5 ± .3
H	.51 min
I	3.95
J	5.08 max
K	7.62 [TP]
L	6.60
M	.25 ± .05
N	.89 min



8192 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

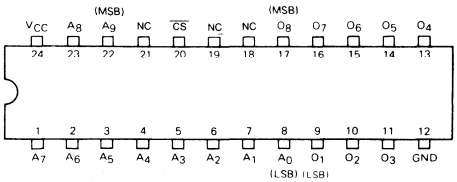
Description

The μPB417C and μPB417D are high speed, electrically programmable, fully decoded 8192 bit TTL read only memories. On-chip address decoding, chip select input and three-state outputs allow easy expansion of memory capacity. μPB417C and μPB417D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 1024 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 50 ns MAX. (μPB417-1)
- Medium power consumption : 500 mW TYP.
- A chip select input for memory expansion
- Three-state outputs
- Plastic 24-Lead Dual In-Line Package (μPB417C)
- Cerdip 24-Lead Dual In-Line Package (μPB417D)
- Fast programming time : 200 μs/bit TYP.
- Replaceable with : Signetics' 82S2708, Harris' HM7608 and equivalent devices (as a ROM)

Connection Diagram (Top View)



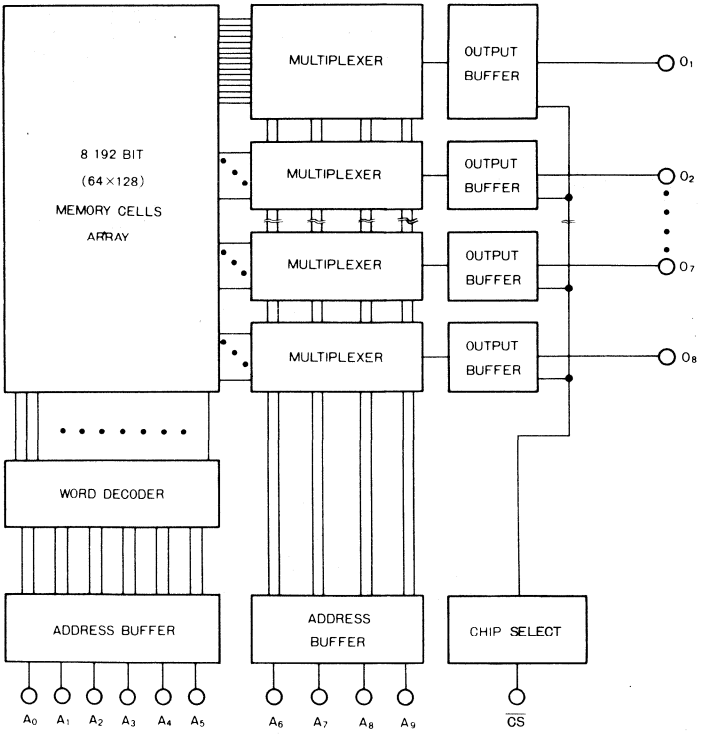
Pin names
$A_0 - A_9$: Address Inputs
$O_1 - O_8$: Data Outputs
$\overline{CS}$: Chip Select Input
NC : No Connection
V_{CC} : Power Supply (+5V)
GND : Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Select input $\overline{CS}$ must be a logical one in order to disable the outputs. Second, the desired word is selected by the ten address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, the Chip Select input must be a logical zero. The outputs then correspond to the data programmed in the selected words. When the Chip Select input is a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	V_{CC}	−0.5 to +7.0	V
INPUT VOLTAGE	V_I	−0.5 to +5.5	V
OUTPUT VOLTAGE	V_O	−0.5 to +5.5	V
OUTPUT CURRENT	I_O	50	mA
OPERATING TEMPERATURE	T_{opt}	−25 to +75	°C
STORAGE TEMPERATURE			
CERDIP PACKAGE	T_{stg}	−65 to +150	°C
PLASTIC PACKAGE	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	20		70	mA	V_O=0 V	

CAPACITANCE (V_{CC}=5 V, f=1 MHz, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN}=2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT}=2.5 V

A.C. CHARACTERISTICS (V_{CC}=4.5 to 5.5 V, T_a=0 to +75 °C)

CHARACTERISTIC	SYMBOL	μPB417C-1 μPB417D-1		μPB417C μPB417D		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		50		60	ns
Chip Select Access Time	t_{ACS}		30		40	ns
Chip Select Disable Time	t_{DCS}		30		40	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

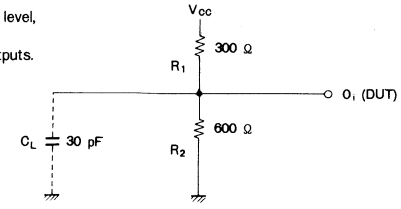


Fig. 1

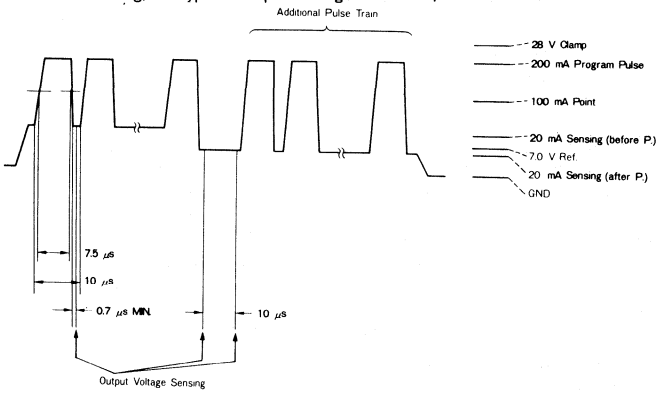
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB417C and μPB417D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

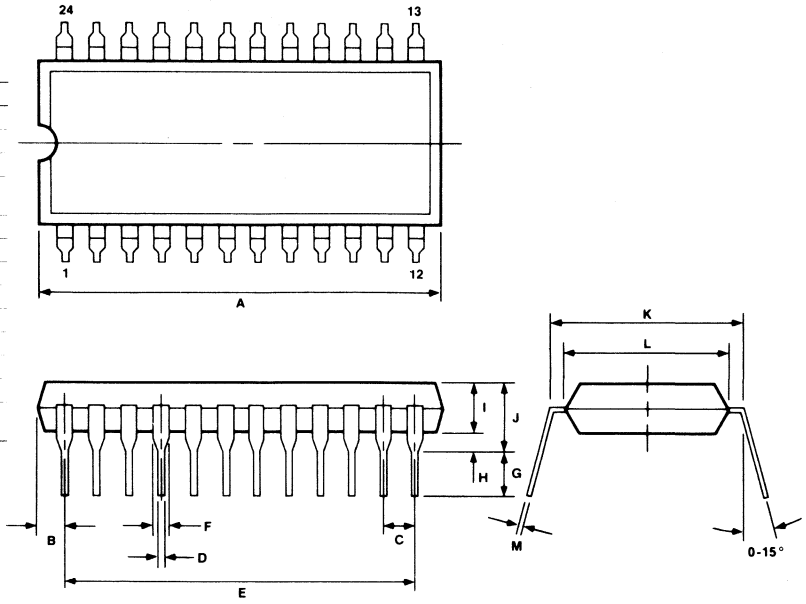
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

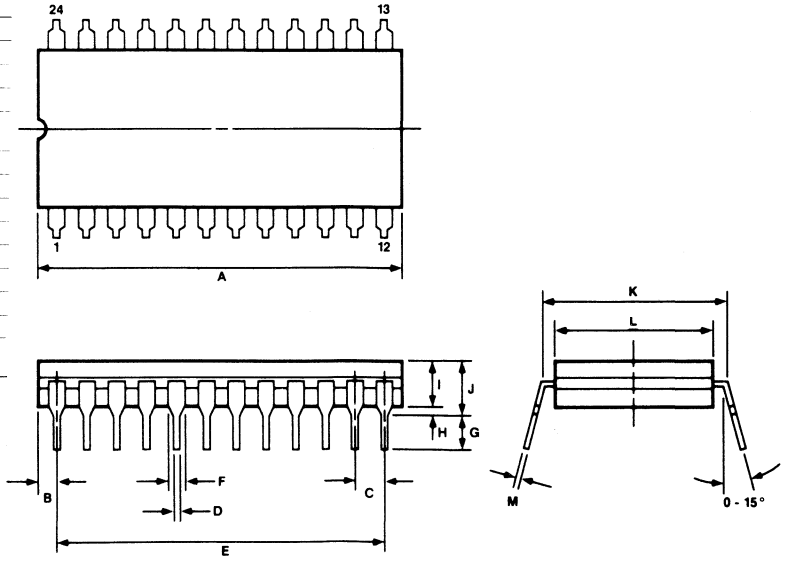
24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



8192 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

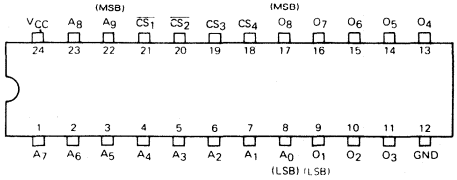
Description

The μPB408C, μPB408D, μPB428C and μPB428D are high speed, electrically programmable, fully decoded 8192 bit TTL read only memories. On-chip address decoding, four chip select inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB408C, μPB408D, μPB428C and μ428D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 1024 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 50 ns MAX. (μPB408-1, μPB428-1)
- Medium power consumption : 500 mW TYP.
- Four chip select inputs for memory expansion
- Open-Collector outputs (μPB408C, μ408D)/Three-state outputs (μPB428C, μPB428D)
- Cerdip 24-Lead Dual In-Line Package (μPB408D, μPB428D)
- Plastic 24-Lead Dual In-Line Package (μPB408C, μPB428C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : Signetics' 82S180/181, Harris' HM 7680/7681 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

$A_0 - A_9$	: Address Inputs
$O_1 - O_8$	: Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	: Chip Select Inputs
V_{CC}	: Power Supply (+5V)
GND	: Ground

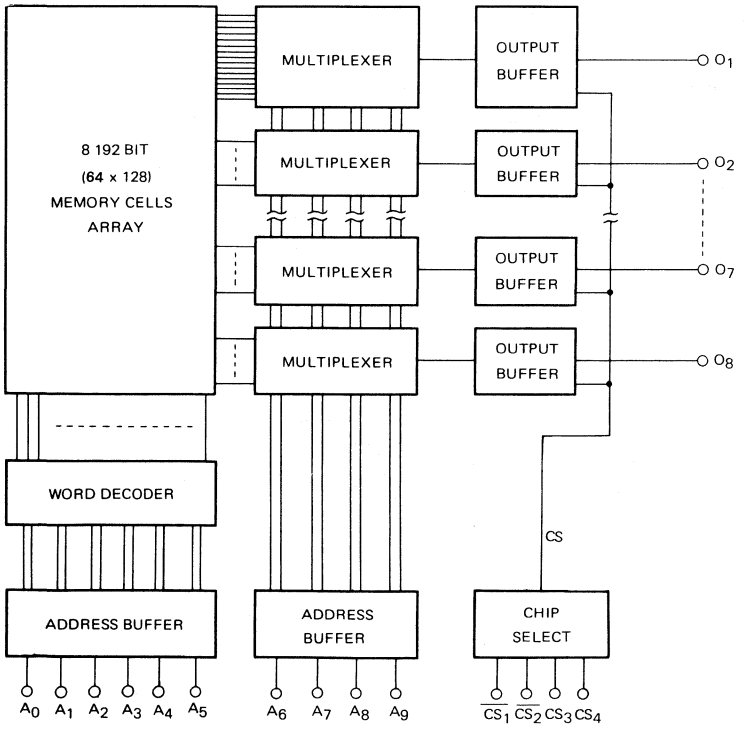
Operation

First we define an internal Chip Select logic by four Chip Select inputs:
$CS' = \overline{CS_1} + \overline{CS_2} + \overline{CS_3} \cdot \overline{CS_4}$
That is, CS' is a logical zero (low) if and only if $\overline{CS_1} = \overline{CS_2} = 0$ and $CS_3 = CS_4 = 1$. While CS' is a logical one (high) in all the other cases.

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. The four Chip Select inputs must be set so that CS' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, The four Chip Select inputs must be set so that CS' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Select inputs are set so that CS' becomes a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded.	V_{CC}=5.5 V
* Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
* Output Short Circuit Current	$-I_{SC}$	20		70	mA	V_O=0 V	

* Note: Applicable to μPB428C and μPB428D.

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	μPB408C-1, μPB428C-1 μPB408D-1, μPB428D-1		μPB408C, μPB428C μPB408D, μPB428D		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		50		60	ns
Chip Select Access Time	t_{ACS}		30		40	ns
Chip Select Disable Time	t_{DCS}		30		40	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

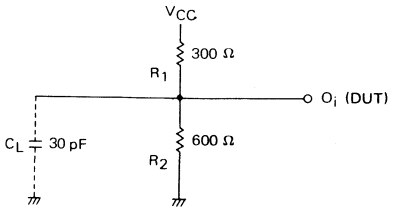


Fig. 1

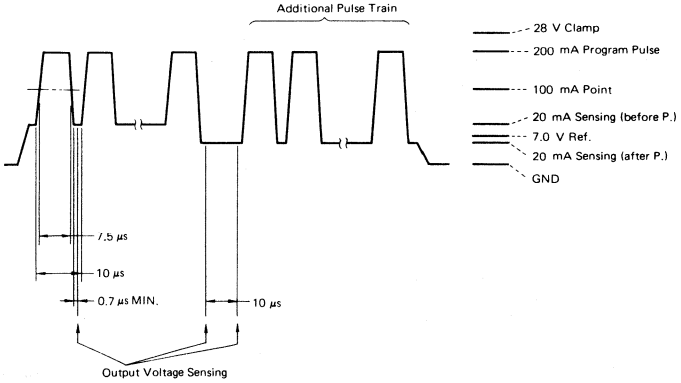
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB408C, μPB408D, μPB428C and μPB428D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

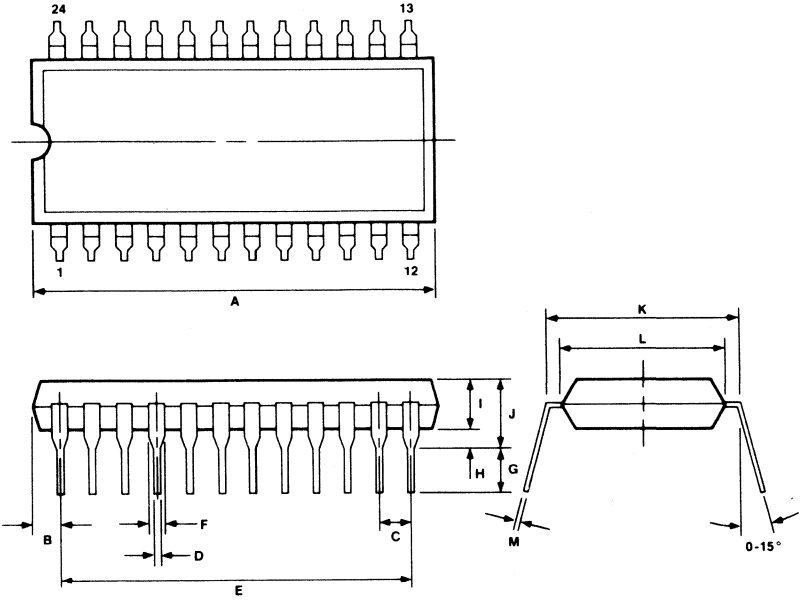
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

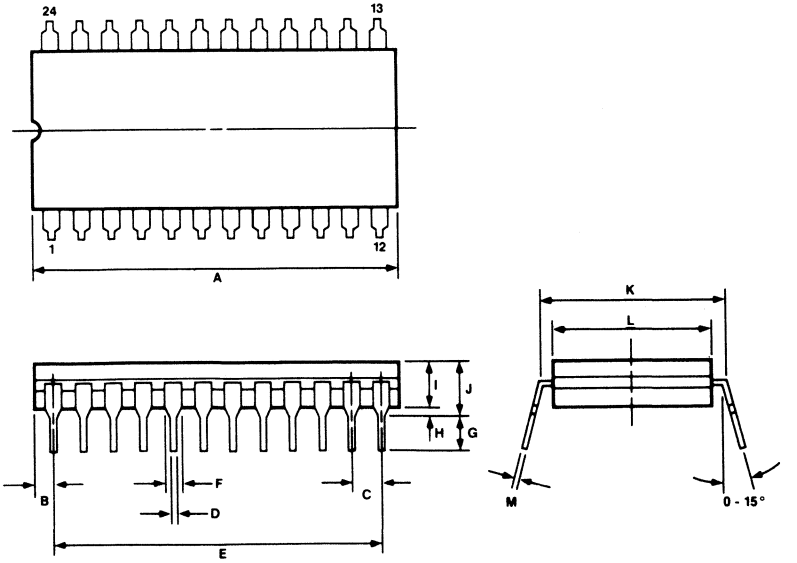
24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



16384 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

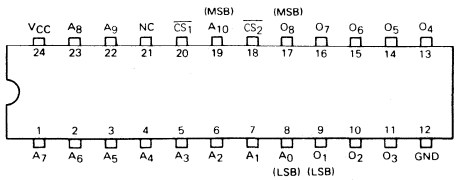
Description

The μPB419C and μPB419D are high speed, electrically programmable, fully decoded 16384 bit TTL read only memories. On-chip address decoding, two chip select inputs and three-state outputs allow easy expansion of memory capacity. The μPB419C and μPB419D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 2048 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 50 ns MAX. (μPB419-2)
- Medium power consumption : 500 mW TYP.
- Two chip select inputs for memory expansion
- Three-state outputs
- Cerdip 24-Lead Dual In-Line Package (μPB419D)
- Plastic 24-Lead Dual In-Line Package (μPB419C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : Intel's 2716 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

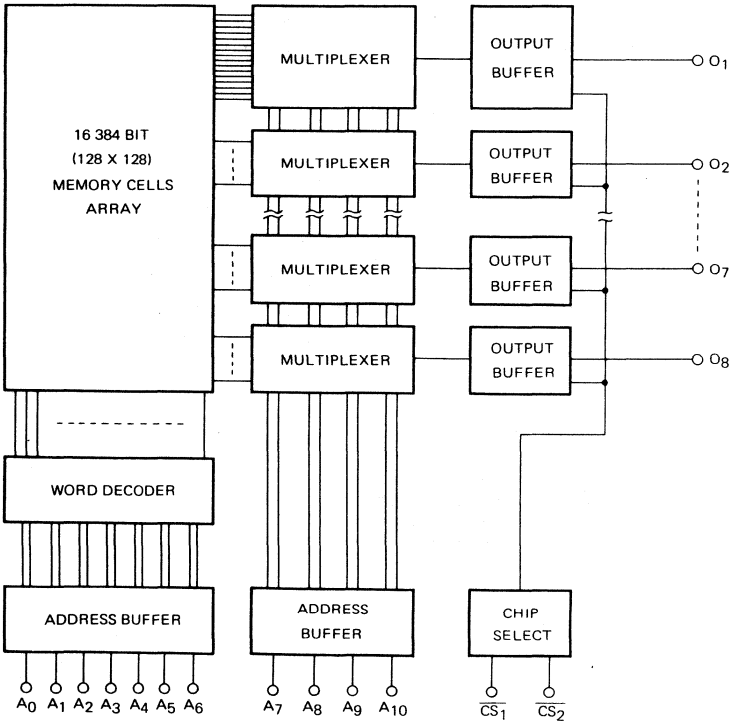
$A_0 - A_{10}$	: Address Inputs
$O_1 - O_8$	: Data Outputs
$\overline{CS}_1, \overline{CS}_2$	: Chip Select Inputs
NC	: No Connection
V_{CC}	: Power Supply (+5V)
GND	: Ground

Operation

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the eleven address inputs in TTL levels. Either or both of the two Chip Select inputs $\overline{CS}_1$ and $\overline{CS}_2$ should be at a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, Both of the two Chip Select inputs must be held at a logical zero. The outputs then correspond to the data programmed in the selected words. When either or both of the two Chip Select inputs are at a logical one, all the outputs will be floating.

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Input High Voltage	V_{IH}	2.0			V		
Input Low Voltage	V_{IL}			0.85	V		
Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded	V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
Output Short Circuit Current	$-I_{SC}$	20		70	mA	V_O=0 V	

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to +75 °C)

CHARACTERISTIC	SYMBOL	μPB419C-2 μPB419D-2		μPB419C-1 μPB419D-1		μPB419C μPB419D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		50		60		70	ns
Chip Select Access Time	t_{ACS}		30		40		50	ns
Chip Select Disable Time	t_{DCS}		30		40		50	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

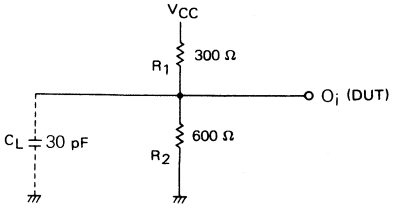


Fig. 1

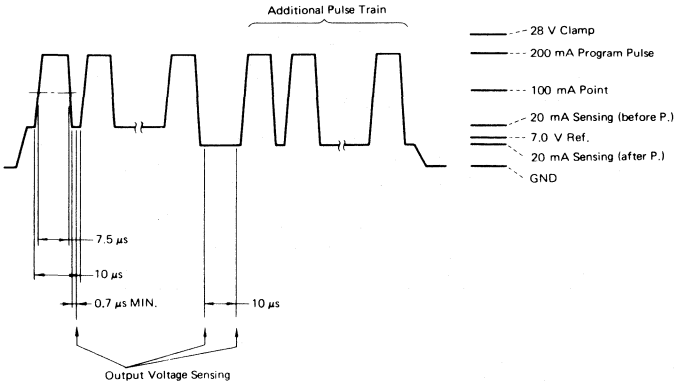
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB419C and μPB419D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

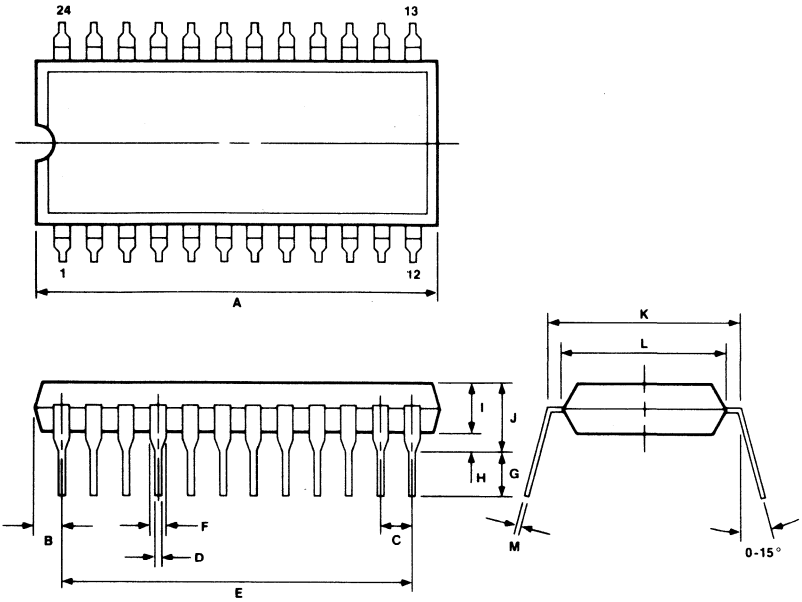
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

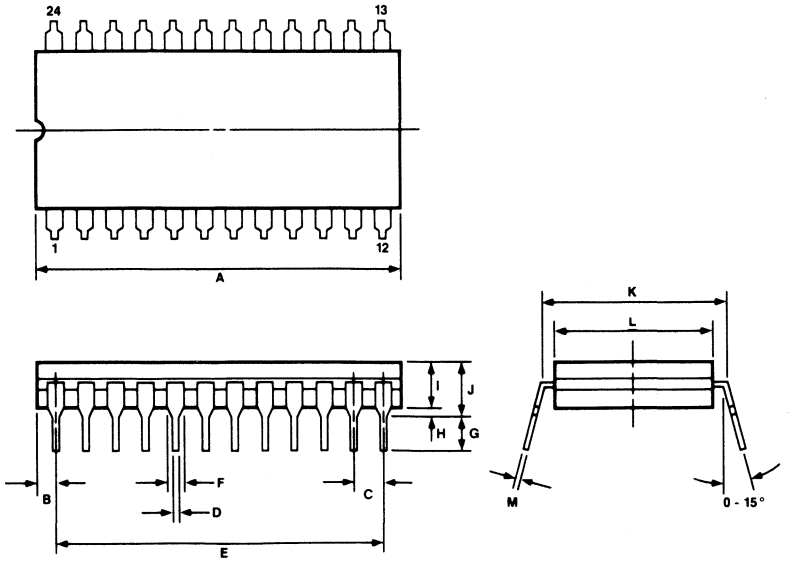
24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



16384 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

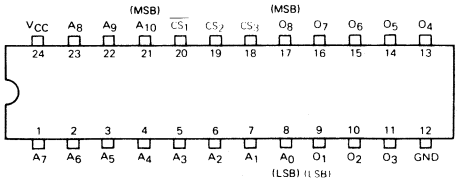
Description

The μPB409C, μPB409D, μPB429C and μPB429D are high speed, electrically programmable, fully decoded 16384 bit TTL read only memories. On-chip address decoding, three chip select inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB409C, μPB409D, μPB429C and μPB29D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 2048 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 45 ns MAX. (μPB409-3, μPB429-3)
- Medium power consumption : 500 mW TYP.
- Three chip select inputs for memory expansion
- Open-Collector outputs (μPB409C, μPB409D) / Three-state outputs (μPB429C, μPB429D)
- Cerdip 24-Lead Dual In-Line Package (μPB409D, 429D)
- Plastic 24-Lead Dual In-Line Package (μPB409C, 429C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : Signetics' 82S190/191, Harris' HM76160/76171 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

$A_0 - A_{10}$	: Address Inputs
$O_1 - O_8$	: Data Outputs
$\overline{CS_1}$, CS_2, CS_3	: Chip Select Inputs
V_{CC}	: Power Supply (+5V)
GND	: Ground

Operation

First we define an internal Chip Select logic by three Chip Select inputs:

$CS' = \overline{CS_1} + CS_2 \cdot CS_3$

That is, CS' is a logical zero (low) if and only if $\overline{CS_1} = 0$ and $CS_2 = CS_3 = 1$, While CS' is a logical one (high) in all the other cases.

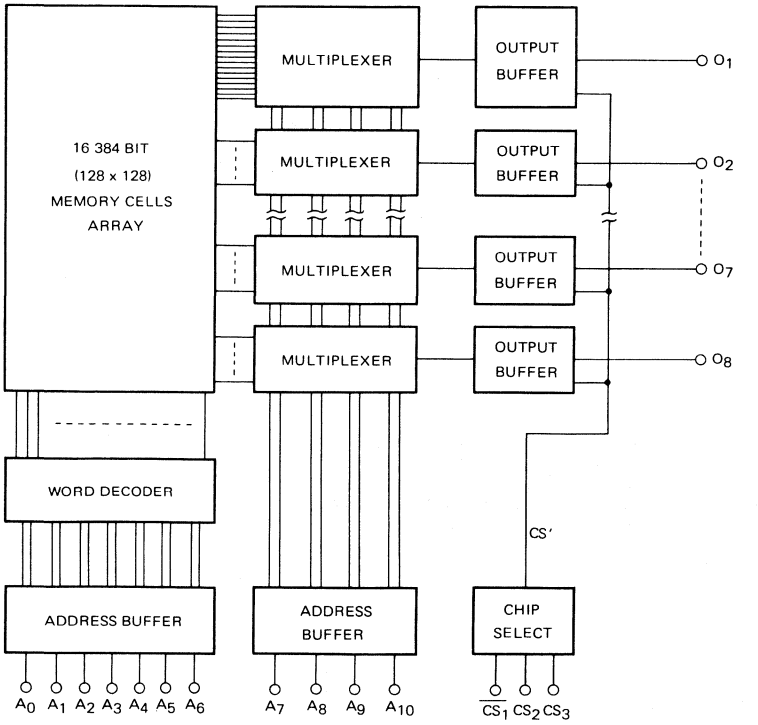
1. Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the eleven address inputs in TTL levels. The three Chip Select inputs must be set so that CS' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading

To read the memory, The three Chip Select inputs must be set so that CS' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the three Chip Select inputs are set so that CS' becomes a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to +75 °C)

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
	Input High Voltage	V_{IH}	2.0			V		
	Input Low Voltage	V_{IL}			0.85	V		
	Input High Current	I_{IH}			40	μA	V_I=5.5 V	V_{CC}=5.5 V
	Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V	V_{CC}=5.5 V
	Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA	V_{CC}=4.5 V
	Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V	V_{CC}=5.5 V
	Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V	V_{CC}=5.5 V
	Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA	V_{CC}=4.5 V
	Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded	V_{CC}=5.5 V
*	Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA	V_{CC}=4.5 V
*	Output Short Circuit Current	$-I_{SC}$	20		70	mA	V_O=0 V	

* Note: Applicable to μPB429C and μPB429D.

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to +75 °C)

CHARACTERISTIC	SYMBOL	μPB409C-3, μPB429C-3 μPB409D-3, μPB429D-3		μPB409C-2, μPB429C-2 μPB409D-2, μPB429D-2		μPB409C-1, μPB429C-1 μPB409D-1, μPB429D-1		μPB409C, μPB429C μPB409D, μPB429D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		45		50		60		70	ns
Chip Select Access Time	t_{ACS}		30		30		40		50	ns
Chip Select Disable Time	t_{DCS}		30		30		40		50	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

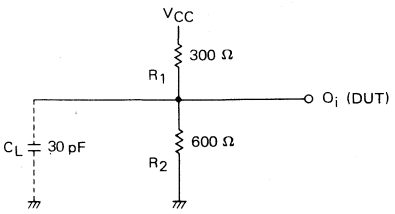


Fig. 1

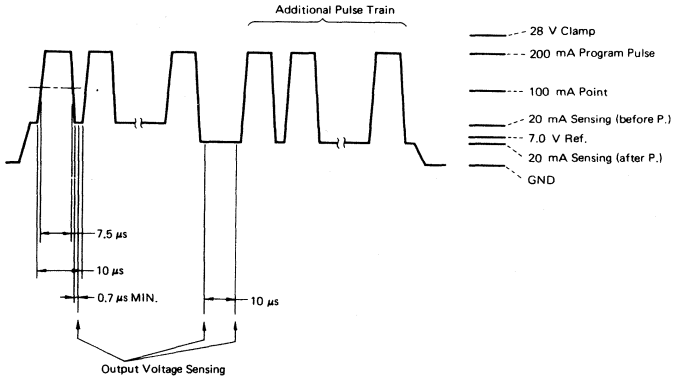
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB409C, μPB409D, μPB429C and μPB429D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

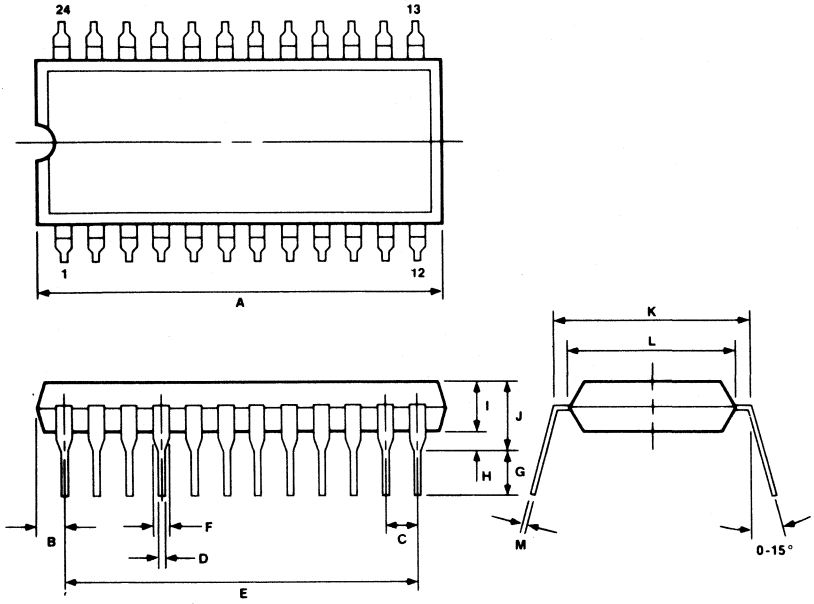
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

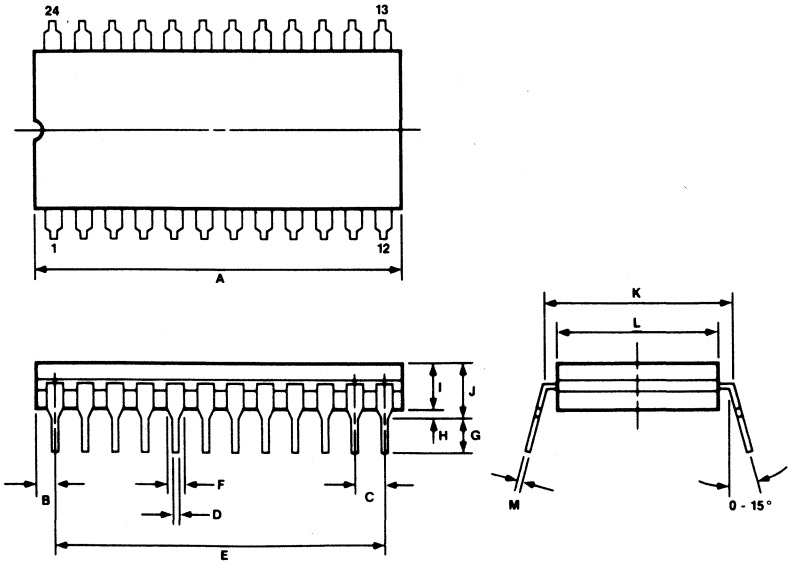
24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	$.25^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05



FPLA

9216 BIT FPLA (FIELD PROGRAMMABLE LOGIC ARRAY)

Description

The μPB450BC and μPB450BD are high speed 9216-bits Field Programmable Logic Array. It has 24 input – 16 output lines, 72 product term lines, input 2 bit decoders, and 16 bit feed back register.
The interconnection of internal AND–OR arrays are electrically performed by the reliable blown junction method which is widely applied to NEC's bipolar PROM series.

Features

- Input terminals: 24
- Output terminals with latch: 16
- Product terms (AND terms): 72
- J-K flip-flop feed back loops: 16
- 2-bit decoder inputs
- AND–array elements: 80 x 72
- OR–array elements: 72 x 48
- Scan path (Shift register mode) capability of J-K flip-flops
- A Chip–Enable capability of 16 outputs
- Input/Output TTL compability (Three-state outputs)
- Single power supply (V_{CC}=5 V)
- Supply current: 200 mA MAX.
- Fast propagation delay t_{PIO} from inputs to outputs:

μPB450BC, μPB450BD	70 ns TYP.
μPB450BC-1, μPB450BD-1	50 ns TYP.

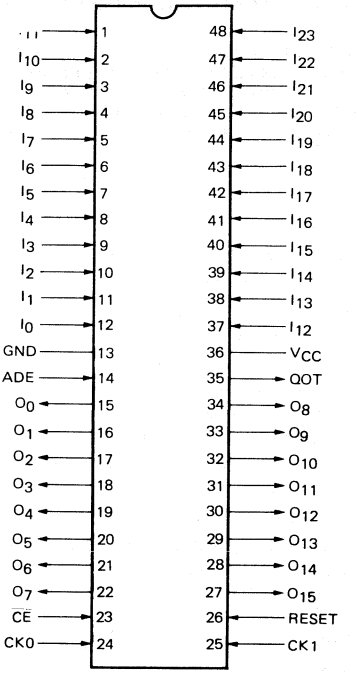
- Plastic 48-Lead Dual In-Line Package (μPB450BC, μPB450BC-1)
- Ceramic 48-Lead Dual In-Line Package (μPB450BD, μPB450BD-1)

MODE SELECTION

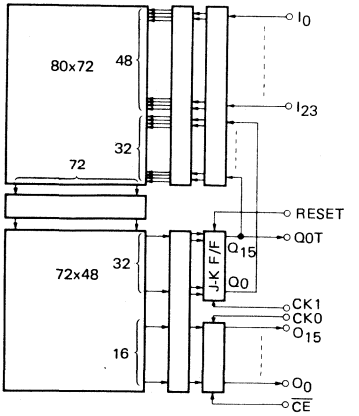
MODE	0	1	2
ADE	L	H	H
$\overline{CE}$	X	L	H

X=H or L

Pin Configuration



MODE 0 BLOCK DIAGRAM



PIN NAMES

I_0~I_{23}	Inputs
O_0~O_{15}	Outputs
ADE	Mode control
QOT	Shift Register Output (Mode 2)
$\overline{CE}$	Output and Mode Control
CK0	Output latch Control
CK1	Feed back register Clock
RESET	Feed back register reset
V_{CC}	Power Supply (+5 V)
GND	Ground

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	±20	mA
Power Dissipation	P_D	1.5	W
Operating Temperature	T_{opt}	0 to +75	°C
Storage Temperature (PLASTIC)	T_{stg}	−55 to +125	°C
Storage Temperature (CERAMIC)	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Operating Temperature	T_a	0		65	°C

D.C. CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a= 0 to +75 °C*)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_O = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_O = 10 mA
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Input High Current	I_{IH}			40	μA	V_I = 2.4 V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4 V
Output High Leakage I	I_{OFFH}			40	μA	V_O = 2.4 V
Output Low Leakage I	$-I_{OFFL}$			40	μA	V_O = 0.4 V
Output Short Circuit Current	$-I_{OS}$	6		30	mA	V_O = 0 V
Power Supply Current	I_{CC}			250	mA	

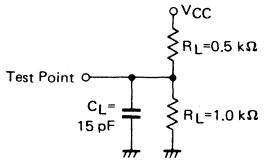
- MODE 0

A.C. CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a=0 to+75 °C*)

CHARACTERISTIC	SYMBOL	μPB450BC μPB450BD			μPB450BC-1 μPB450BD-1			UNIT	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Propagation Delay Times	t_{PIO}	20	70	100	20	50	70	ns	I→O, JK
	t_{PCIQ}	15		60	15		40	ns	CK1↓→Q
	t_{PRQ}			50			50	ns	RESET↓→Q : L
	t_{DCE}			70			50	ns	$\overline{CE}$↑→O: Hi-Z
	t_{ACE}			70			50	ns	$\overline{CE}$↓→O: active
	t_{HCOO}	15		70	15		50	ns	CK0↑→O: unlatched
Cycle Time	t_{CYC}	140			100			ns	Note 1
Pulse Width	t_{WCOH}	50			40			ns	CK0 = H
	t_{WCIL}	30			20			ns	CK1 = L
	t_{WCIH}	100			70			ns	CK1 = H
	t_{WRL}	50			30			ns	RESET = L
Input Set up Time for CK0	t_{SIC0}	100			70			ns	I→CK0↓
Input Hold Time for CK0	t_{HIC0}	0			0			ns	I←CK0↓
Input Set up Time for CK1	t_{SIC1}	80			60			ns	I→CK1↓
Input Hold Time for CK1	t_{HIC1}	15			15			ns	I←CK1↓
CK1 Hold Time for RESET	t_{HCIR}	50			50			ns	CK↓←RESET↑
CK0 Set up Time for CK1	t_{CIC0}			15			15	ns	CK1↓→CK0↓

Note 1. t_{CYC} min. = t_{SIC1} min. + t_{PCIQ} max.

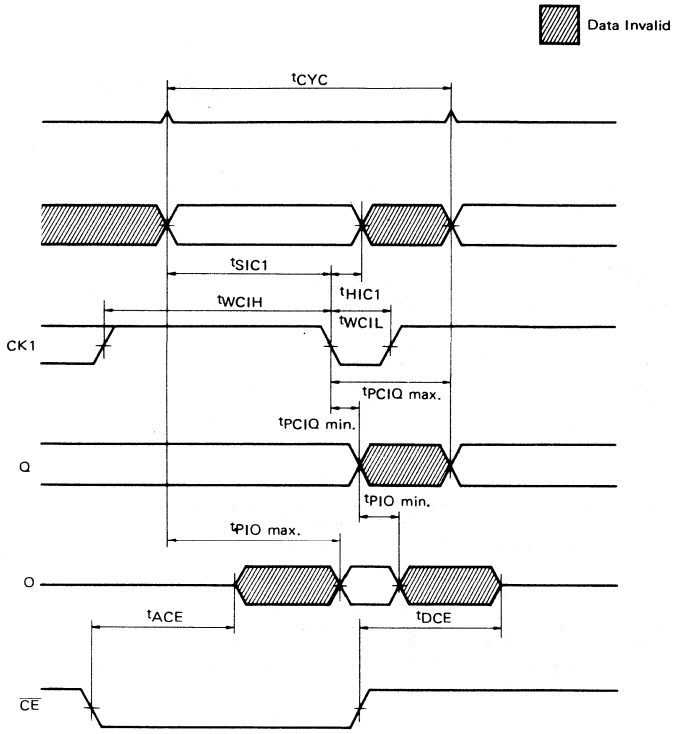
A.C. CHARACTERISTICS TEST LOAD



* In the flowing air larger than 2 m/s.
Under the still air condition, the allowable ambient temperature range is 0 to +65 °C.

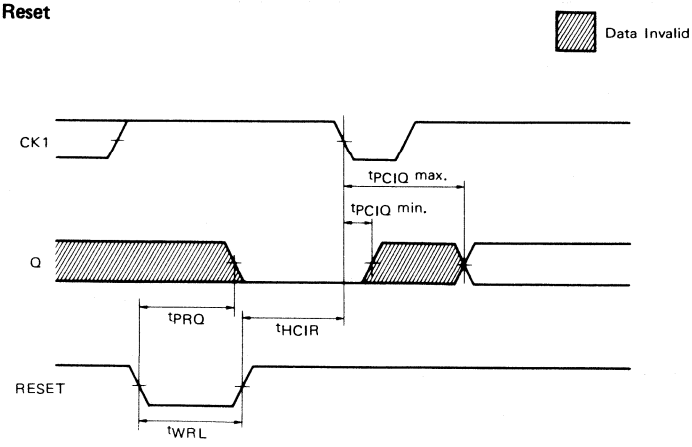
- **MODE 0**

  Output Thru Mode (CK 0 = H)



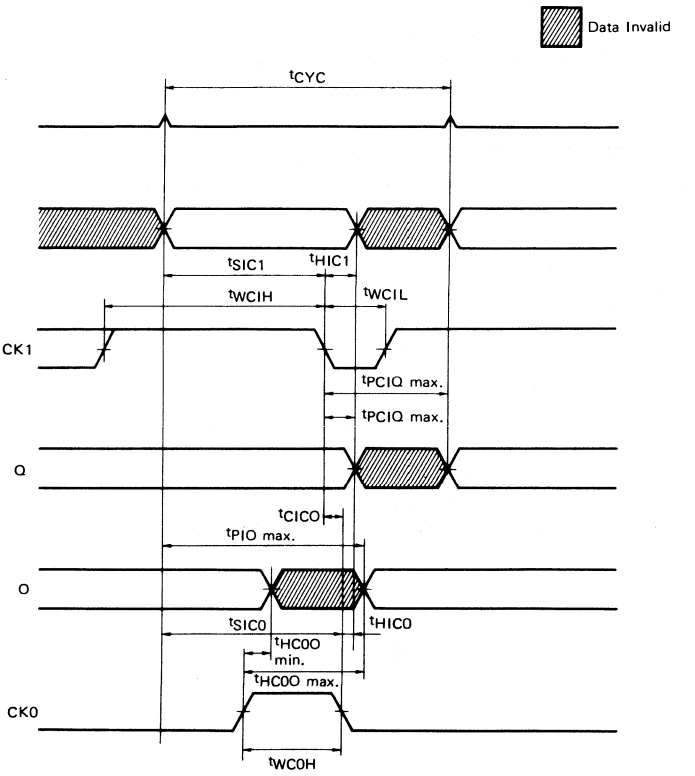
- **MODE 0**

  JK F/F Reset



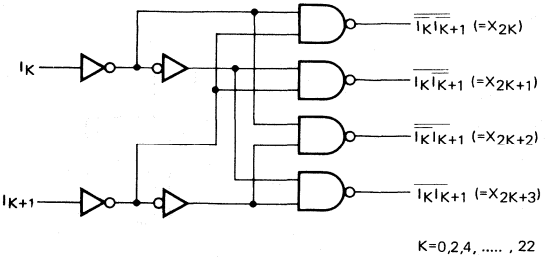
- **MODE 0**

Output Latch Mode

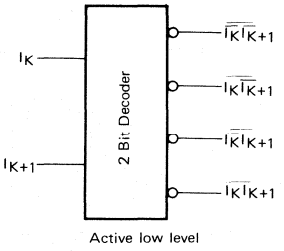


FUNCTION BLOCK DETAILS

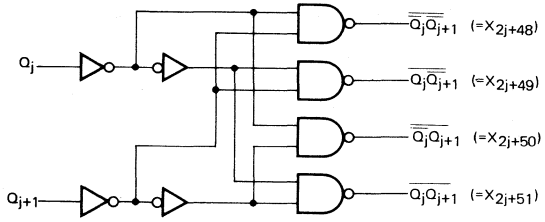
Input Buffer and 2-bit Decoder



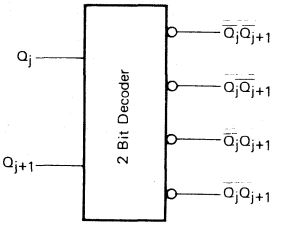
K=0,2,4, ... , 22



Active low level

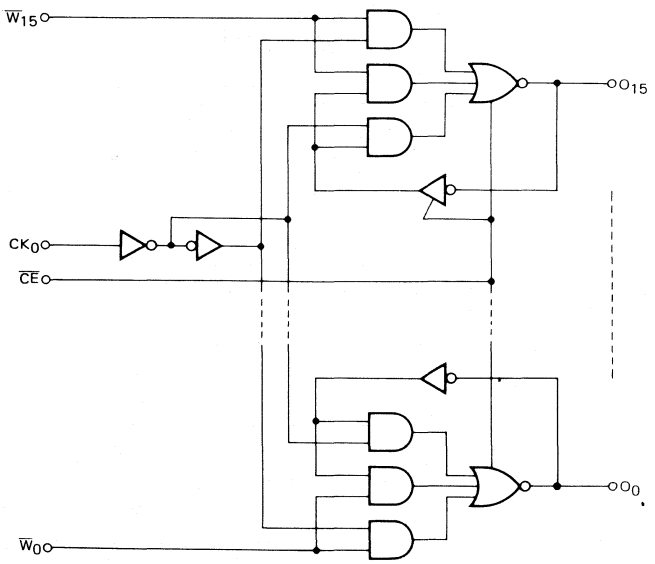


J=0,2,4, ... , 14

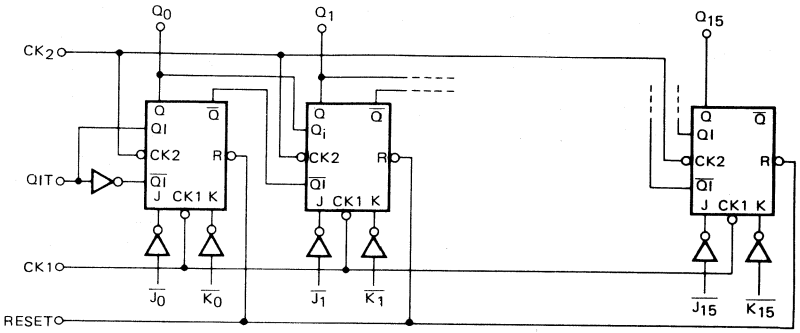


Active low level

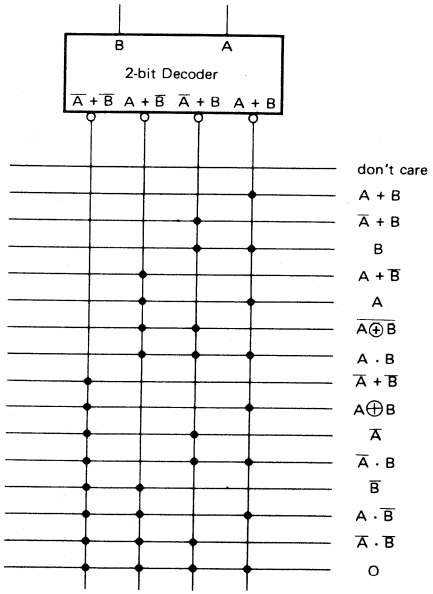
Output Latches



J-K Flip-Flops

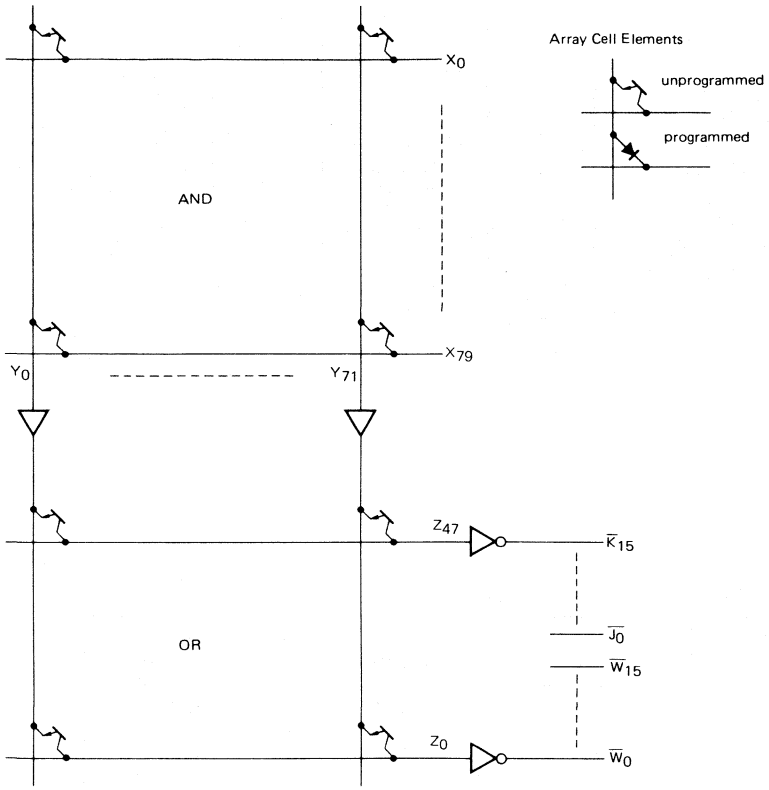


16 Two-Input Functions Using 2-bit Decoder

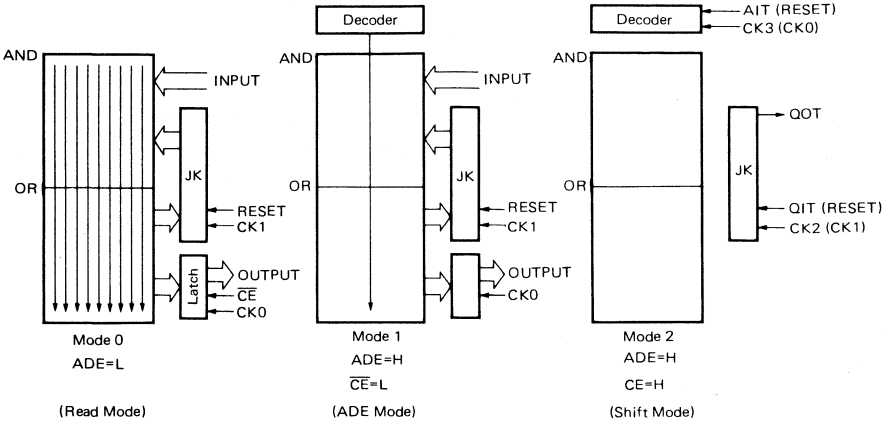


Note: "●" shows programmed point (Diode state).

Array Cell and Output Buffer



MODE SELECT AND OPERATION



CONTROL SIGNAL INTERNAL CONNECTION

Mode / Control Pin	0 Read Mode	1 ADE Mode	2 Shift Mode
CK0	CK0	CK0	CK3
CK1	CK1	CK1	CK2
RESET	RESET	RESET	QIT/AIT
QOT	*	*	QOT

* : don't care

TRUTH TABLE

Latched Output (i=0 to 15)

Mode	ADE	$\overline{CE}$	CK0	Oi	Function
0	L L L	L L H	H ↓ X	Wi Oi Hi–Z	thru, latch } select de-select
1	H H	L L	H ↓	Wi Oi	thru, latch } select
2	H	H	X	Hi–Z	de-select

J-K F/F (j=0~15) CK0=H or L (don't care)

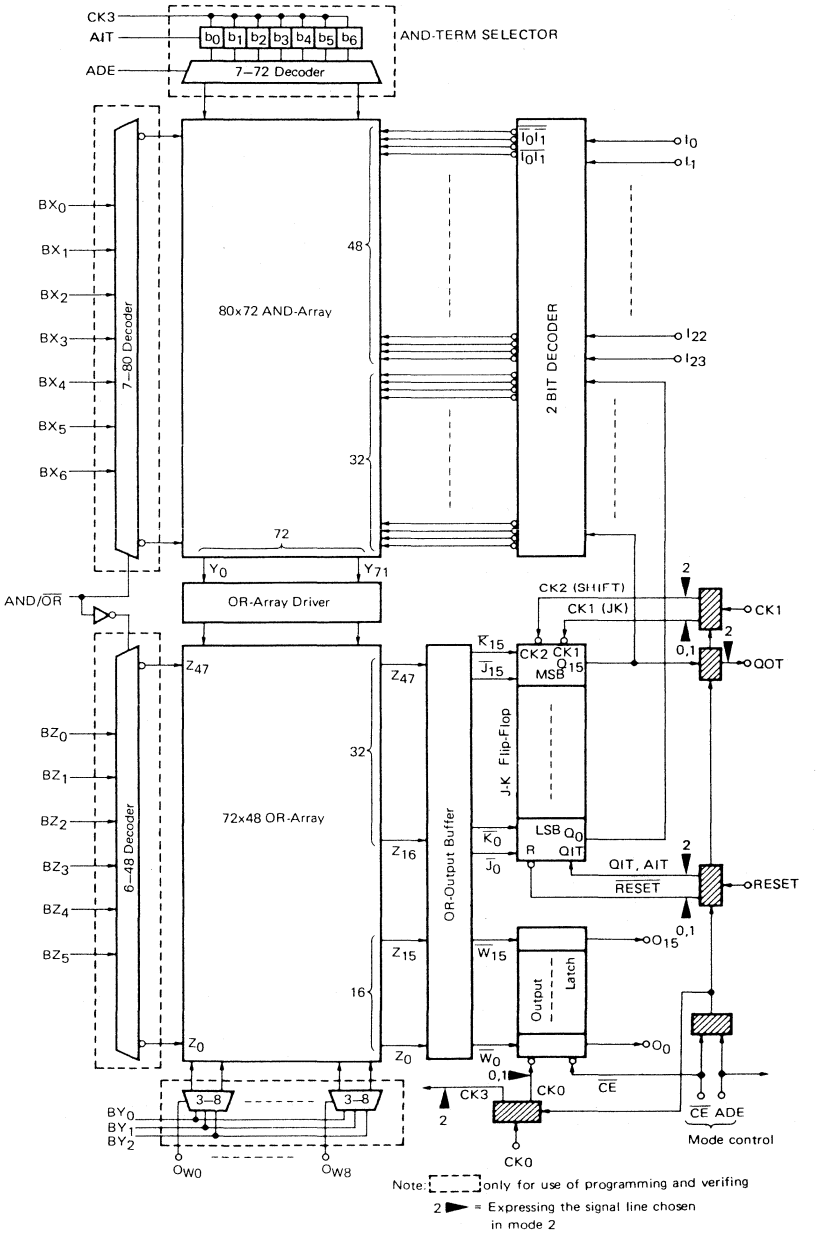
Mode	ADE	$\overline{CE}$	CK1 / $\overline{CK2}$	RESET / $\overline{QIT}$	QOT	Q_j	Function
0	L L	X X	H X	H L	X X	Q'_j L	hold, reset } static
	L	X	↓	H	X	J-K Operation	J-K Mode
1	H H	L L	H X	H L	X X	Q'_j L	hold, reset } static
	H	L	↓	H	X	J-K Operation	J-K Mode
2	H H	H H	H ↓	X L/H	$=Q_{15}$ X	Q'_j Q'_{j-1}	hold, shift } S.R. Mode

AND-TERM Selector (n=0 to 6, i=0 to 71)

Mode	ADE	$\overline{CE}$	CK3	AIT	b_n	Y_i
0	L	X	X	X	X	H : all select
1	H	L	X	X	b'n (hold)	H : i = selected by b_0 to b_6 L : i = deselected by b_0 to b_6
2	H H	H H	H ↓	X H/L	b'n (hold) b'_{n-1}	H : i = selected by b_0 to b_6 L : i = deselected by b_0 to b_6 b_n : data transfer (b'_{n-1} = AIT)

Note. H: High level, L: Low level, X: H or L

BLOCK DIAGRAM (Full Mode)

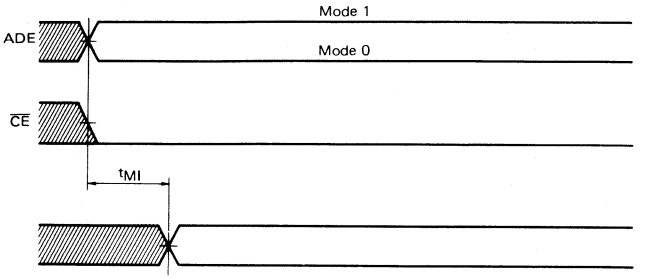


MODE 1, 2 and Mode Selection
A.C. CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a=0 to+75 °C*)

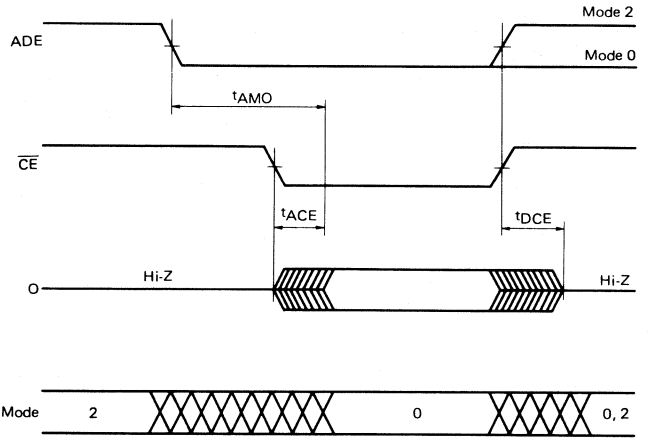
CHARACTERISTIC	SYMBOL	μPB450BD/μPB450BD-1			UNIT	CONDITIONS
		MIN.	TYP.	MAX.		
Clock Pulse Width	t_{WC2L}	100			ns	CK2=L
	t_{WC2H}	200			ns	CK2=H
	t_{WC3L}	100			ns	CK3=L
	t_{WC3H}	200			ns	CK3=H
Mode Set up Time for Input	t_{MI}	200			ns	Mode Set →I
Mode Set up Time for CK2	t_{MC2}	200			ns	Mode Set →CK2 ↓
Mode Set up Time for CK3	t_{MC3}	200			ns	Mode Set →CK3 ↓
CK2 Set up Time for Mode Set	t_{SC2M}	200			ns	CK2 ↑→Mode Set
CK3 Set up Time for Mode Set	t_{SC3M}	200			ns	CK3 ↑→Mode Set
QIT Set up Time for Mode Set	t_{SQM}	200			ns	QIT ↑→Mode Set
QIT Hold Time for Mode Set	t_{HQM}	100			ns	QIT ↓←Mode Set
AIT Set up Time for Mode Set	t_{SAM}	200			ns	AIT ↑→Mode Set
AIT Hold Time for Mode Set	t_{HAM}	100			ns	AIT ↓←Mode Set
QIT Set up Time for CK2	t_{SQC2}	100			ns	QIT →CK2 ↓
QIT Hold Time for CK2	t_{HQC2}	100			ns	QIT ← CK2 ↓
AIT Set up Time for CK3	t_{SAC3}	100			ns	AIT →CK3 ↓
AIT Hold Time for CK3	t_{HAC3}	100			ns	AIT ← CK3 ↓
Propagation Delay Time	t_{PMQ}			200	ns	$\frac{\overline{ADE}\uparrow}{\overline{CE}\uparrow}$ →QOT
	t_{PC2Q}			100	ns	CK2 ↓→QOT
	t_{AMO}			400	ns	ADE ↓→O: adive

• MODE SELECTION

Mode 0, 1, 2→Mode 0, 1 (Input)

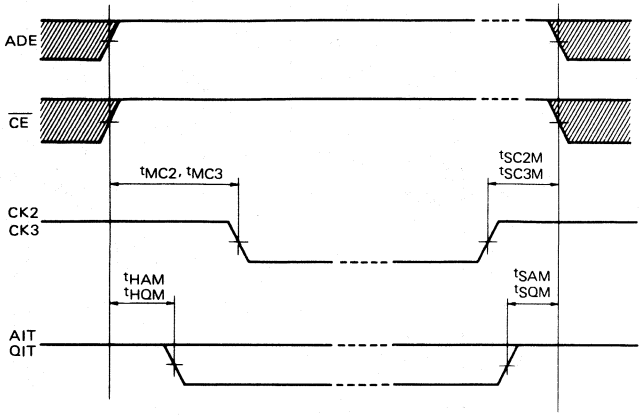


Mode 0↔2 (Output Condition)



• MODE SELECTION

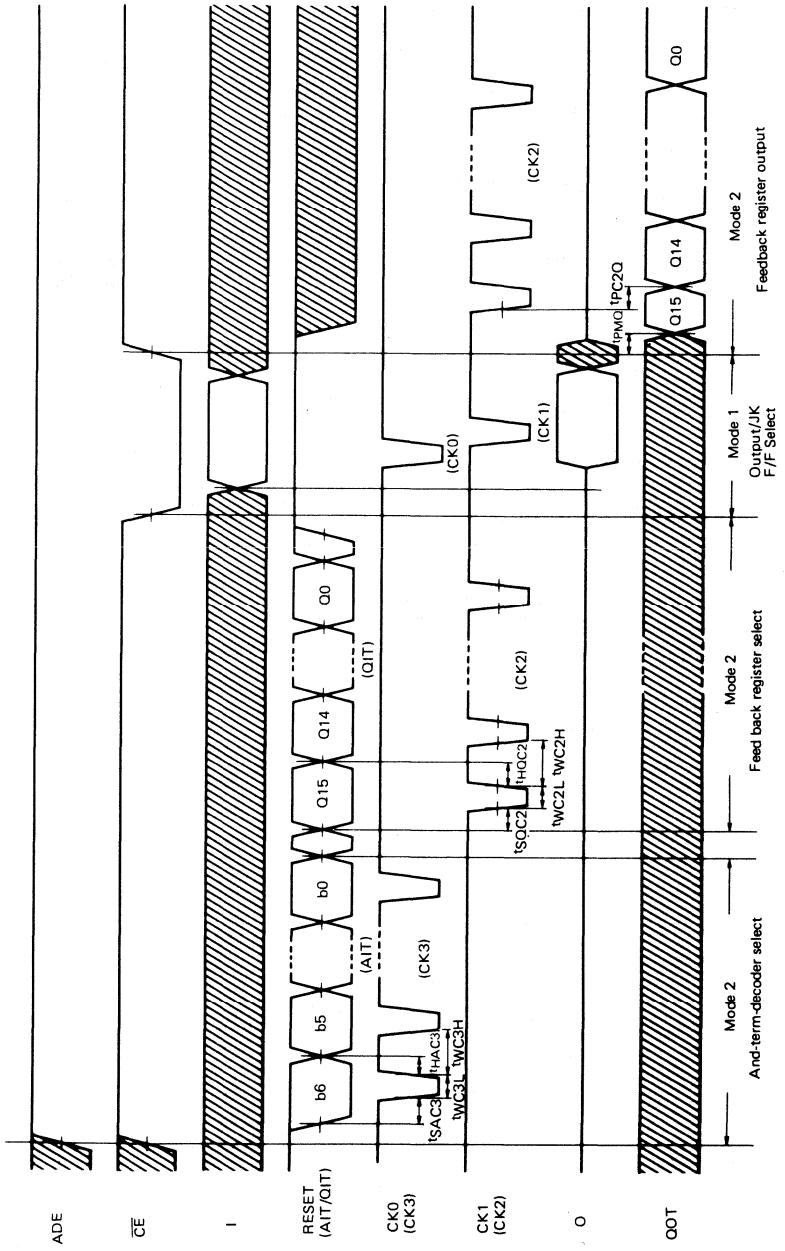
Mode 0, 1⟷Mode 2



Note: Set the CK0 (CK3), CK1 (CK2) and RESET (AIT/QIT) inputs to "H" level when changing mode.

- MODE 1, 2

Verify



Programming (Writing) Operation

This information is prepared for performing the programming (writing) of 9,216-bit FPLA properly by the specified "writer" or the equivalents.
The first step of the programming is to confirm the logic levels of the selected bit locations for blank-check by sensing operation. This is also important to avoid the unexpected reprogramming of the arrays.
The sensing operation is accomplished by forcing a 20 mA constant DC current into the selected bit location through the output terminals and compare the terminal voltage to the reference voltage which is large enough to force the sensing current.
If the terminal voltages are larger than the reference voltage, the selected bit locations are confirmed to be "0" (blank or unprogrammed) levels.
The next step is the programming by forcing 200 mA current into the selected bit locations to flash the junctions.
The specified pulse width of the forcing current is 7.5 μs.
This operation is required by few times until the logic level is altered from "0" level to "1" level.
The accomplishment of the programming operation is assured when the sensing voltage turned to be lower than the reference voltage.

PIN ASSIGN TABLE

PROGRAMMING	MAIN	PIN NUMBER		MAIN	PROGRAMMING
	I_{11}	1	48	I_{23}	V_{CCP}
	I_{10}	2	47	I_{22}	TTL low level
	I_9	3	46	I_{21}	TTL low level
	I_8	4	45	I_{20}	
BX_4 (BZ_4)	I_7	5	44	I_{19}	
BX_3 (BZ_3)	I_6	6	43	I_{18}	
BX_2 (BZ_2)	I_5	7	42	I_{17}	
BX_1 (BZ_1)	I_4	8	41	I_{16}	BX_5 (BZ_5)
BX_0 (BZ_0)	I_3	9	40	I_{15}	BX_6
BY_0	I_2	10	39	I_{14}	AND/$\overline{OR}$
BY_1	I_1	11	38	I_{13}	
BY_2	I_0	12	37	I_{12}	
GND	GND	13	36	V_{CC}	GND
	ADE	14	35	QOT	Open
	O_0	15	34	O_8	
	O_1	16	33	O_9	
	O_2	17	32	O_{10}	
O_{W0}	O_3	18	31	O_{11}	
O_{W1}	O_4	19	30	O_{12}	O_{W8}
O_{W2}	O_5	20	29	O_{13}	O_{W7}
O_{W3}	O_6	21	28	O_{14}	O_{W6}
O_{W4}	O_7	22	27	O_{15}	O_{W5}
	$\overline{CE}$	23	26	RESET	
	CK0	24	25	CK1	

Programming Procedures

To keep the reliability of the FPLA chips against the thermal damage in programming operation, the recommendable procedures and conditions are as follows.

1. Set the power supply and pin connection. (See Table 1)
2. Select a cell to be programmed by setting input signals pairs BX, BY or BZ, BY.
3. Sense the selected cell by forcing a 20 mA DC current to confirm that the cell is unprogrammed.
4. Program the cell by forcing a 200 mA current pulse having a pulse-width of 7.5 μs and check the cell is programmed by sensing operation.
5. If the cell is not programmed repeat the procedure 4 and 5 until it is performed within 1000 pulses.
6. If the cell programmed, force 4 additional pulses to make sure the programming.
7. Repeat the above procedure to the other selected cells.

Only one programming current pulse is allowed to force at the same time to avoid excessive heat up of the FPLA chip.

PROGRAMMING SPECIFICATION

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Ambient Temperature	Ta	20	25	30	°C	
Programming Pulse						
Current Amplitude	I_{PRG}	190	200	210	mA	
Clamp Voltage	V_{PRG}	27.5	28.0	28.0	V	
Ramp Rate				70	V/μs	15 V point/150 Ω load
(Both in Rise and in Fall)						
Pulse Width	t_{PW}	7.2	7.5	7.8	μs	
Duty Cycle		70			%	
Sense Current						
Current Amplitude	I_S	19.5	20.0	20.5	mA	
Clamp Voltage	V_S	27.5	28.0	28.0	V	15 V point/150 Ω load
Ramp Rate				70	V/μs	
(Both in Rise and in Fall)						
Maximum Sensed Voltage	V_{REF}	7.9	8.0	8.1	V	OR–array sense
for programmed "1"		8.9	9.0	9.1	V	AND–array sense
Address Set Up Time	t_{SD}	10			μs	
Address Hold Time	t_{HD}	10			μs	
Delay from trailing edge of programming pulse before sensing output voltage	t_{SR}	700			ns	
Programming Circuit Power Supply Voltage	V_{CCP}					See Fig. 1
Programming Circuit Power Supply Current	I_{CCP}			150	mA	
Input High Level	V_{IH}	2.0		0.8	V	
Input Low Level	V_{IL}				V	

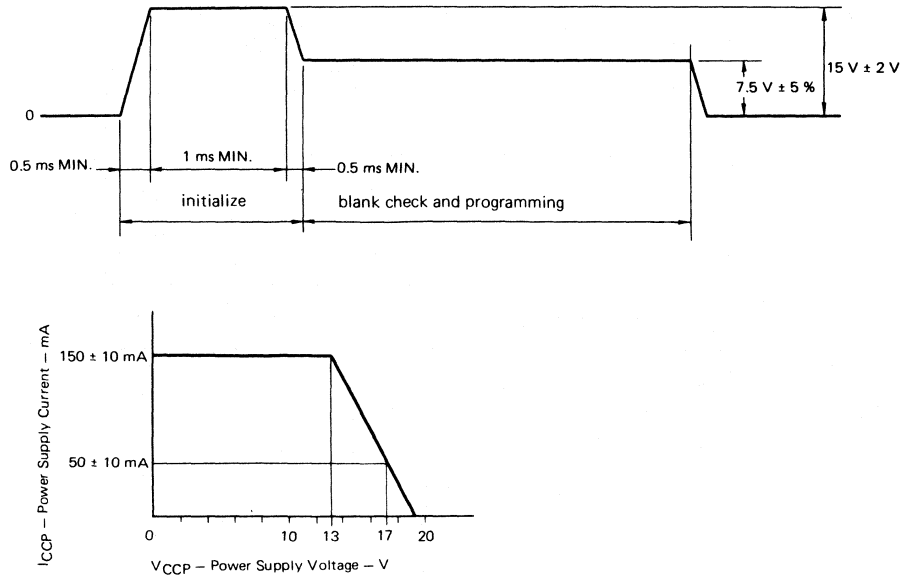


Fig. 1 Power Supply Voltage Wave Forms and Current Supply Ability

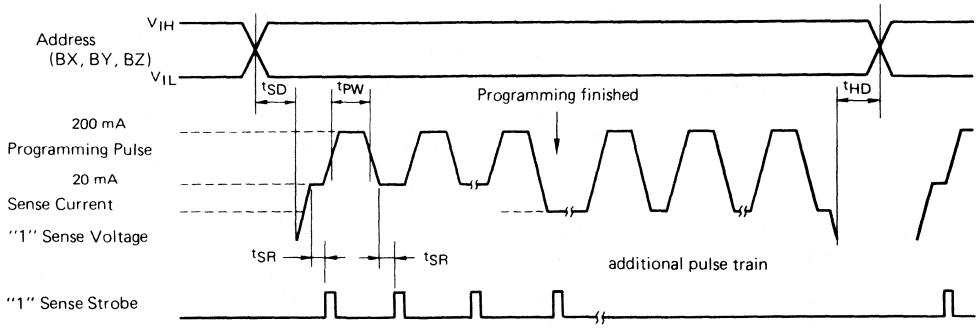


Fig. 2 Programming Wave Forms

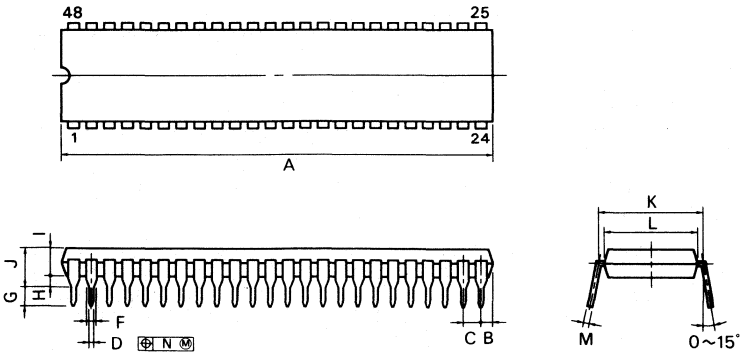
Table 1. Programming and Verifing Sequence Table

MNEMONIC / SUB-MNEMONIC		DATA INPUT																				DATA OUTPUT		CONTROL PIN						POWER	
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	$O_0 \sim O_{15}$		ADE	$\overline{CE}$	CK0 CK0 CK3	CK1 CK1 CK2	RESET RESET QIT AIT	Q0T	V_{CC}	GND
		BY_2	BY_1	BY_0	BX_0 (BZ_0)	BX_1 (BZ_1)	BX_2 (BZ_2)	BX_3 (BZ_3)	BX_4 (BZ_4)							AND BX_6 $\overline{OR}$		BX_5 (BZ_5)				V_{CCP}		$O_{W0} \sim O_{W8}$									
PROGRAM	AND-PROGRAM	BY_2	BY_1	BY_0	BX_0	BX_1	BX_2	BX_4	BX_4							0	BX_6	BX_5				0	0	3		p.p.~p.p	x	x	x	x	x			G	G
	OR-PROGRAM	BY_2	BY_1	BY_0	BZ_0	BZ_1	BZ_2	BZ_3	BZ_4							1		BZ_5				0	0	3		p.p.~p.p.	x	x	x	x				G	G
VERIFY	RANDOM PATH CHECK	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1 (16)	0/1	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	x	x	0	0	1	1	x	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	22	I_{23}	M~M	M~M	0	0	1	1	x	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	M~M	M~M	0	0	1	1	x	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	x	x	0	x	1	1 (16)	0/1	M	+5 V	G
	AND TERM WISE CHECK	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1 (7)	1	0/1	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	x	x	1	1	1	1 (16)	0/1	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	M~M	1	1	0	1	1	x	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	x	x	1	0	1	1	x	x	+5 V	G
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	I_{22}	I_{23}	x	x	1	1	1	1 (16)	0/1	M	+5 V	G
	Notes.	X: irrelevant																			3: High Power Supply for Programming.		M: Measurement P.P.: Program Pulses for Pragramming				1: Clock triggered 1 (7): Clock triggered 7 times.						

Package Dimensions

48 PIN Plastic DIP (600 mil)

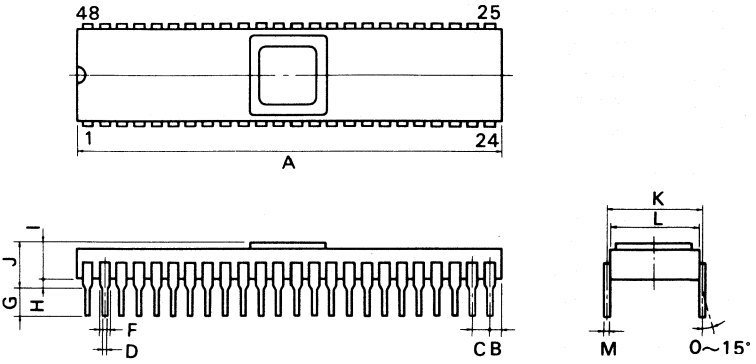
ITEM	MILLIMETERS
A	63.50 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{\pm 0.10}$
F	1.1 MIN.
G	$3.6^{\pm 0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.8
M	$0.25^{+0.10}_{-0.05}$
N	0.25



48 PIN Ceramic DIP (600 mil)

μPB450BD

ITEM	MILLIMETERS
A	63.50 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.46^{+0.05}$
F	0.92 MIN.
G	$3.5^{\pm 0.3}$
H	1.0 MIN.
I	2.74
J	4.57 MAX.
K	15.24 (T.P.)
L	14.93
M	$0.25^{+0.05}$
N	0.25



Static MOS RAMs

Description

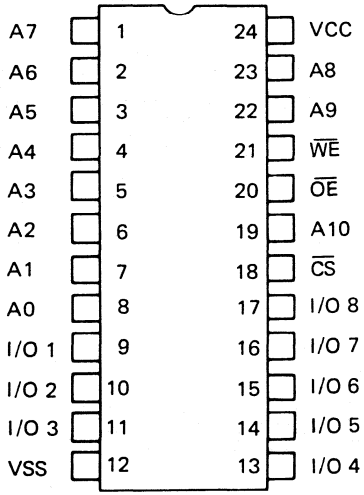
2048 x 8 Bit Static NMOS RAM

The μPD4016 is 16,384 bit static Random Access memory device organized as 2048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with nonclocked static memories.
The μPD4016 has a three-state output and offers a stand-by mode with an attendant 75 % savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in a standard 24-pin dual-in-line package and is plug-compatible with 16K EPROMS.

Features

- 2K x 8 Organization
- Single + 5V Supply (± 10 % tolerances)
- Fully Static Operation (no clocks, no refresh)
- 24 pin 600 mil Package Configuration (μPD4016C)
- 24 pin 300 mil Plastic Package is available (μPD4016CX)
- Plug-in compatible with 16K 5V EPROMs (μPD4016C)
- Equal Access and Cycle Times
- Three-State Outputs
- $\overline{OE}$ eliminates need for external Bus Buffers
- Common I/O Capability
- All Inputs and Outputs fully TTL compatible
- Scaled MOS technology
- Automatic Power Down
- Power dissipation — 60mA max. (Active), 15mA max. (Standby)
- Fast Access Time — 120 ns/150 ns/200 ns/250 ns max.

Pin Configuration



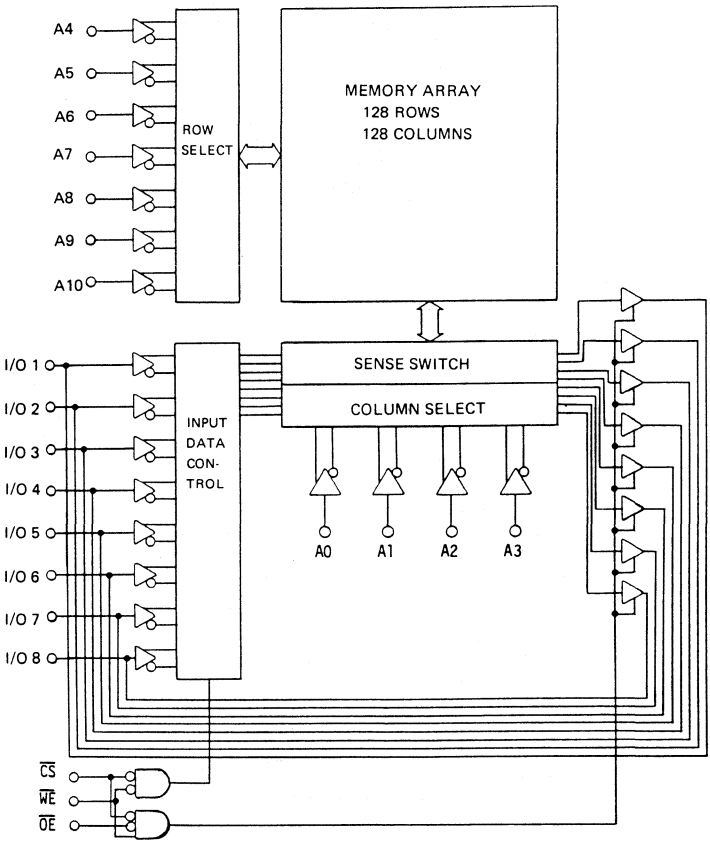
Pin Names

A0 - A10	:	Address Inputs
$\overline{WE}$	:	Write Enable
$\overline{CS}$	:	Chip Select
$\overline{OE}$	:	Output Enable
I/O1 - I/O8	:	Data Input/Output
VCC	:	Power (+ 5V)
VSS	:	Ground

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	Dout	Active
L	H	L	Write	Din	Active
L	L	L	Write	Din	Active

Block Diagram



Absolute Maximum Ratings

Temperature under bias	0°C to + 70°C
Storage temperature	− 55°C to 125°C
Voltage on any pin with respect to Ground	-0.5 V to 7 V
D.C. Output Current	20mA
Power Dissipation	1 W

Comment: Stresses above those listed under »Absolute Maximum Ratings« may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affact device reliability.

D.C. and Operating Characteristics

(Ta = 0°C to 70°C, V_{CC} = 5V±10%) unless otherwise noted.

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current			10	μA	VCC = Max.; VIN = GND to VCC
I_{LO}	Output Leakage Current			10	μA	VCC = Max.; $\overline{CS}$ = VIH; VOUT = GND to VCC
I_{CC}	Operating Current			60	mA	VCC = Max. $\overline{CS}$ = VIL; Outputs Open
I_{SB}	Standby Current			15	mA	VCC = Min. to Max.; $\overline{CS}$ = VIH
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4	V	IOL = 4 mA
V_{OH}	Output High Voltage	2.4			V	IOH = −1mA
I_{OS}	Output Short Circuit Current		70		mA	VOUT = GND to VCC

Capacitance

(Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
CIN	Input Capacitance			5	pF	VIN = OV
CI/O	I/O Capacitance			7	pF	VI/O = OV

Note: This parameter is sampled and not 100% tested.

A.C. TEST CONDITIONS

Input Pulse Levels	0.8 V to 2.2 V
Input Rise and Fall Times	10 nsec
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load	See Figure 1

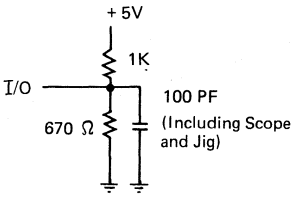


Figure 1

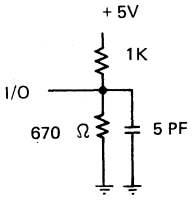


Figure 2

A.C. CHARACTERISTICS

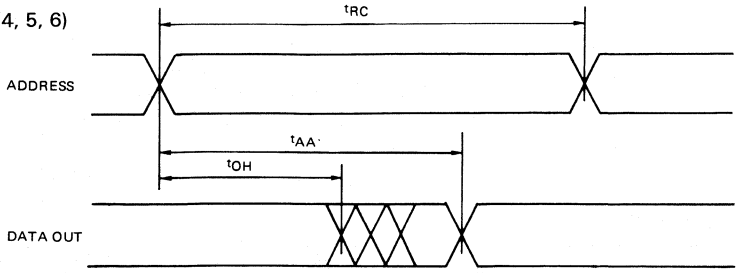
(T_a = 0 to 70°C, V_{CC} = 5 V ± 10 % unless otherwise noted.)

READ CYCLE

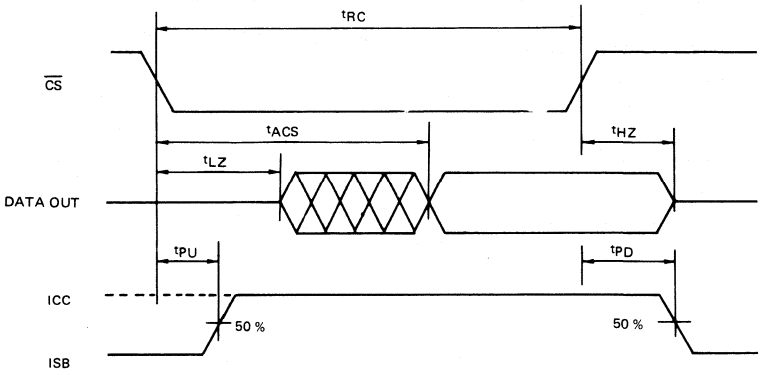
Symbol	Parameter	4016C-5		4016C-3		4016C-2		4016C-1		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	120		150		200		250		nsec	1
t_{AA}	Address Access Time		120		150		200		250	nsec	
t_{ACS}	Chip Select Access Time		120		150		200		250	nsec	2
t_{OH}	Output Hold from Address Change	10		10		10		10		nsec	
t_{LZ}	Chip selection to Output in Low Z	10		10		10		10		nsec	3,7
t_{HZ}	Chip Deselection to Output in High Z		45		50		60		80	nsec	3,7
t_{OE}	Output Enable to Output valid		50		70		90		110	nsec	
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		nsec	3,7
t_{OHZ}	Output Disable to Output in High Z		45		50		60		80	nsec	3,7
t_{PU}	Chip Selection to Power up Time	0		0		0		0		nsec	7
t_{PD}	Chip Deselection to Power down Time		60		70		90		110	nsec	7

WAVE FORMS

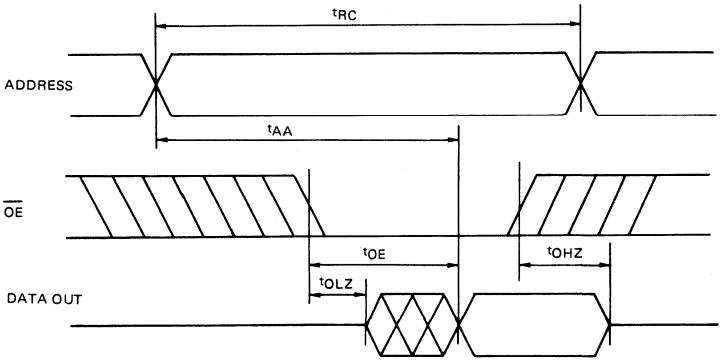
READ CYCLE No. 1 (Note 4, 5, 6)



READ CYCLE No. 2 (Note 2, 4, 6)



READ CYCLE No. 3 (Note 4, 5)



NOTES:

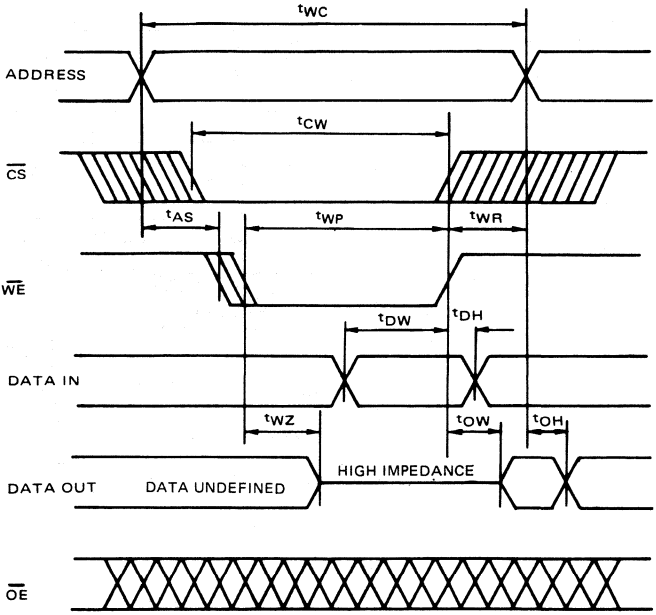
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. $\overline{OE} = V_{IL}$.
7. This parameter is sampled and not 100 % tested.

WRITE CYCLE

Symbol	Parameter	4016C-5		4016C-3		4016C-2		4016C-1		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	120		150		200		250		nsec	
t_{CW}	Chip Selection to End of Write	90		120		160		200		nsec	
t_{AW}	Address Valid to End of Write	80		90		120		150		nsec	
t_{AS}	Address Setup Time	0		0		0		0		nsec	
t_{WP}	Write Pulse Width	70		80		100		130		nsec	1
t_{WR}	Write Recovery Time	10		10		10		10		nsec	
t_{DW}	Date Valid to End of Write	45		50		60		80		nsec	
t_{DH}	Data Hold Time	0		0		0		0		nsec	
t_{WZ}	Write Enable to Output in High Z		45		50		60		80	nsec	2,3
t_{OW}	Output Active from End of Write	10		10		10		10		nsec	2,3

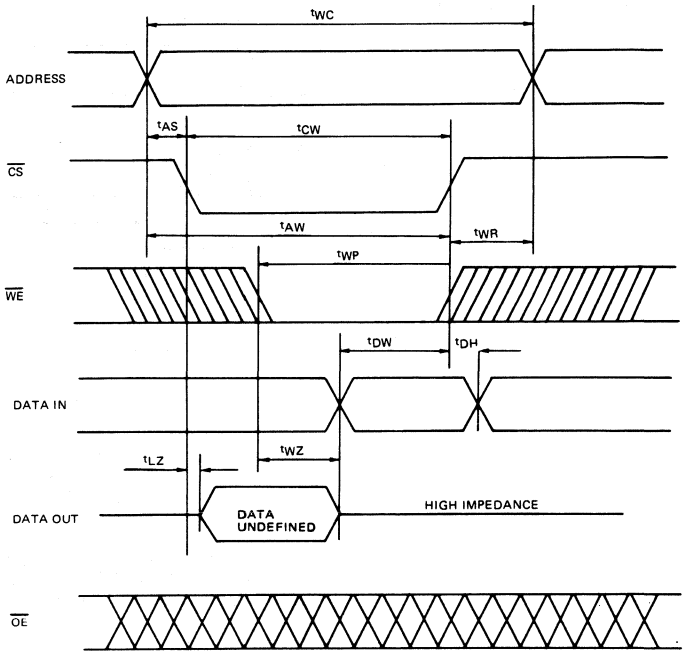
WAVE FORMS

Write Cycle No. 1 ($\overline{WE}$ controlled)



WAVE FORMS

WRITE CYCLE No. 2
($\overline{CS}$ controlled)

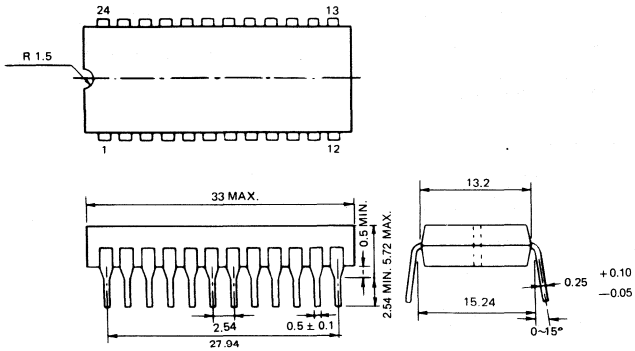


NOTES:

1. If $\overline{CS}$ and $\overline{OE}$ are both low before write enabled, $t_{WP} = t_{WZ} + t_{DW}$.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Figure 2.
3. This parameter is sampled and not 100 % tested.
4. $\overline{WE}$ must be high during address transitions.
5. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
6. When I/O pins are in a low impedance state, input signals must not be applied to them.

μPD4016C

Package Outline
(Unit: mm)

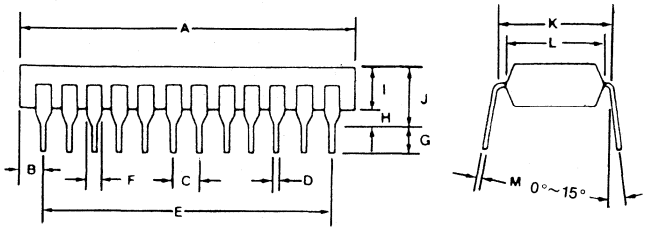


PACKAGE DIMENSIONS

μPD4016CX

Plastic Shrinkdip

Item	Millimeters
A	33 max.
B	1.03
C	2.54
D	0.5±0.1
E	27.94
F	1.5
G	2.54 min.
H	0.5 min.
I	5.22 max.
J	5.72 max.
K	7.62
L	6.4
M	0.25 $^{+0.01}_{-0.05}$



16.384 Bit Static CMOS RAM

Description

The μPD4311C is a high speed, low power, 16.384 words by 1 bit static CMOS RAM fabricated with short channel silicon-gate CMOS process. The μPD4311C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD4311C requires no clock or refreshing to operate.
Two kinds of access time, adress acces time and chip select acces time, are the same and very fast. The grades of access time are 35 ns, 45 ns and 55 ns.
The μPD4311C is fully compatible with μPD2167D. The μPD4311C is packaged in a 20pin plastic Dual In-Line Package (DIP) with the standard 2167 pinout.

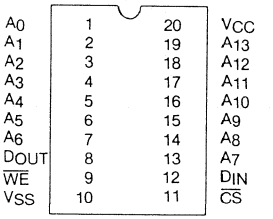
Features

- Single + 5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and the Output
- Separated Data Input and Output
- Three-State Output
- Fast Access Time

μPD4311C-35	35ns MAX
μPD4311C-45	45ns MAX
μPD4311C-55	55ns MAX

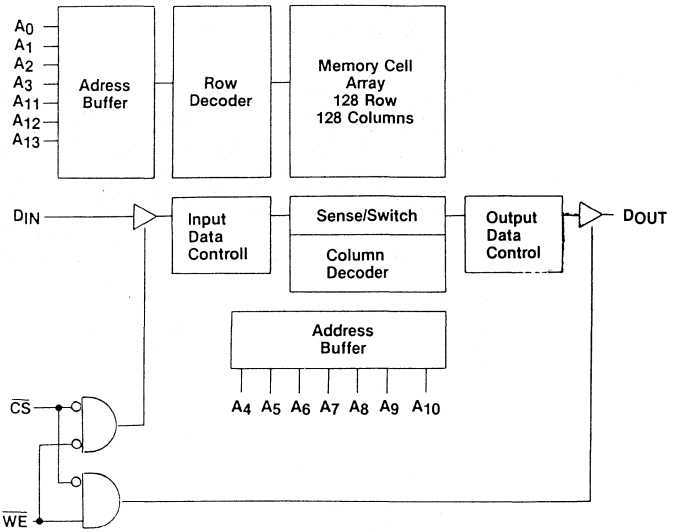
- Low Standby Current 20 mA MAX
- Low Active Current 60mA TYP
- Standard 300mil 20-pin Plastic DIP
- Compatible with μPD2167D

Pin Configuration and Function



A_0 - A_{13}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature μPD4311C Storage Temperature μPD4311D	T_{stg}	−55 to 125 −65 to 150	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0 V MIN. while 20 ns pulse width.

Recommended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
InputHigh Voltage	V_{IH}	2.2		6.0	V

Note (1) V_{IL} = −3.0 V MIN. while 20 ns pulse Width.

Capacitance (Ta = 25 °C f = 1 MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data Output Capacitance	C_{DOUT}	V_{DOUT} = 0V	6	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}, V_{CC} = Max.	−2		2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max.	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0ma		60	80	mA
Stanby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			15	mA
Standby Supply Current	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V, V_{IN} < 0.2V or V_{IN} > V_{CC} −0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA			0.4	mA
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

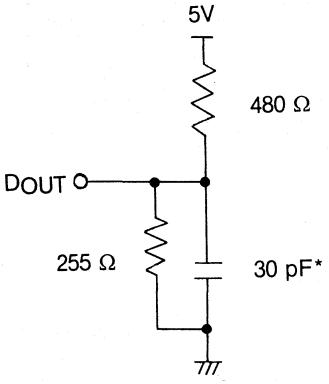


Figure 1 Output Load

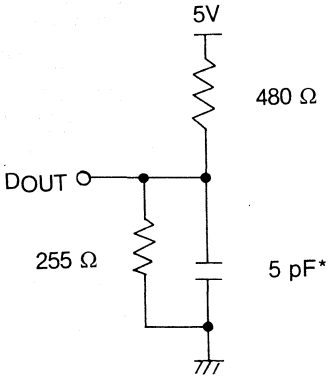


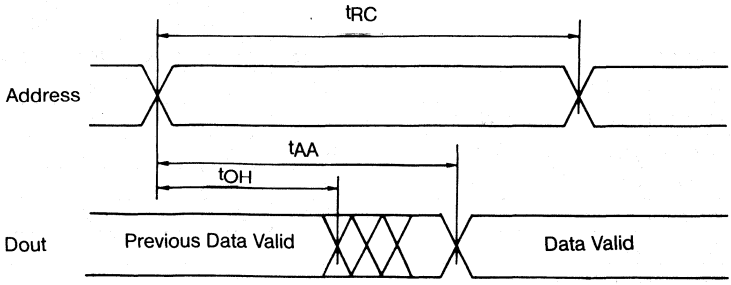
Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

*Including Scope and Jig

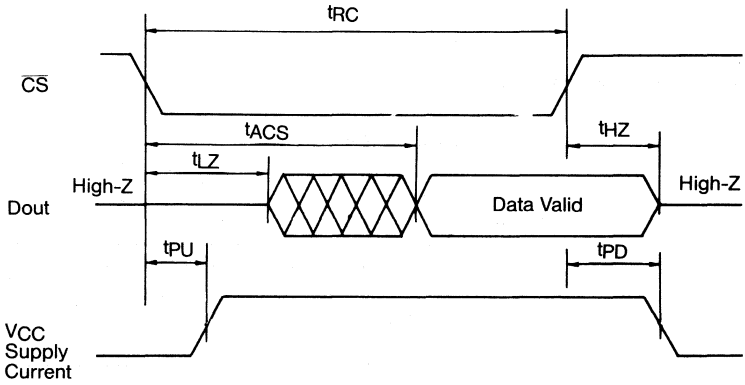
AC Characteristics (T_a = 0 to 70°C V_{CC} = 5 V ±10%)
Read Cycle

Parameter	Symbol	μPD4311C -35		μPD4311C -45		μPD4311C -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	20	0	25	0	30	ns
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Downtime	t_{PD}	0	35	0	40	0	45	ns

Read Cycle No. 1 (Address Access) [4] [5]



Read Cycle No. 2 (Chip Select Access) [4] [6]

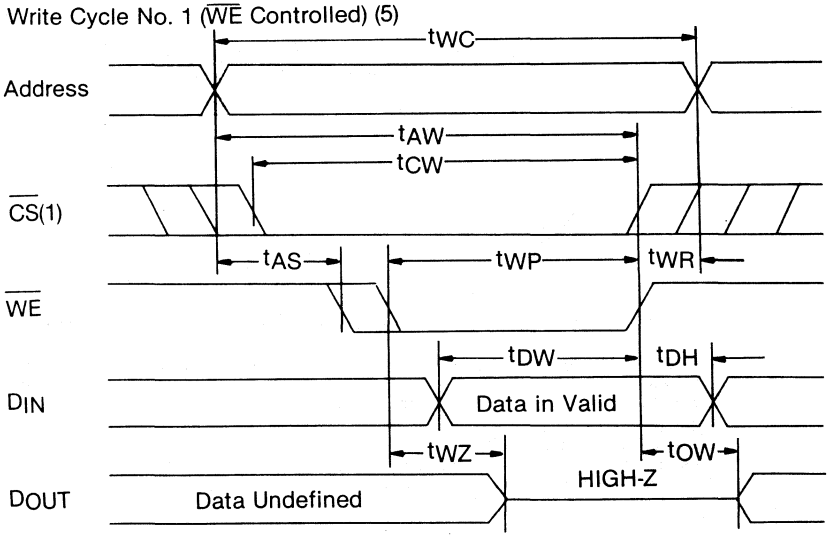


Notes: (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(3) Transition is measured at V_{OL} + 200 mV and V_{OH} -200 mV with specified load in Figure 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continuously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

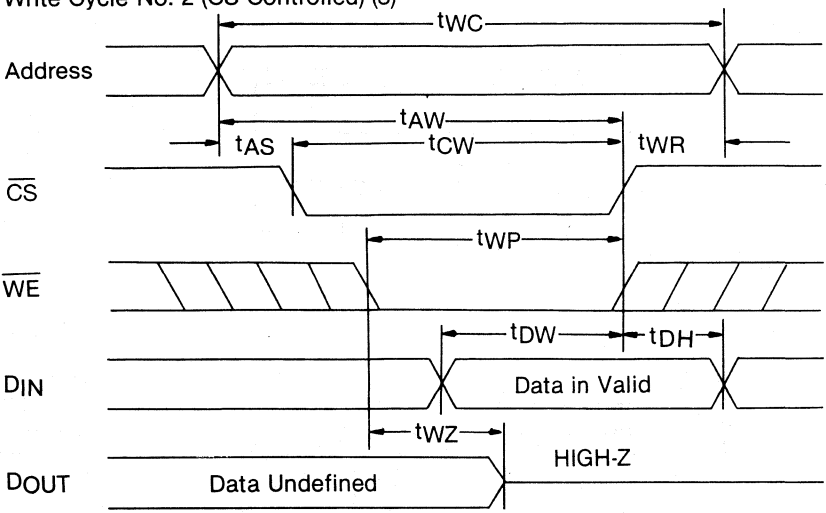
Write Cycle

Parameter	Symbol	μPD4311C —35		μPD4311C —45		μPD4311C —55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	$t_{WC(2)}$	35		45		55		ns
Chip Selection to End of Write	t_{CW}	35		40		45		ns
Access Valid to End of Write	t_{AW}	35		40		45		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	25		30		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	20		25		25		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	$t_{WZ(3)}$	0	20	0	25	0	30	ns
Output Active from End of Write	$t_{OW(4)}$	0		0		0		ns

Write Cycle Wave Forms

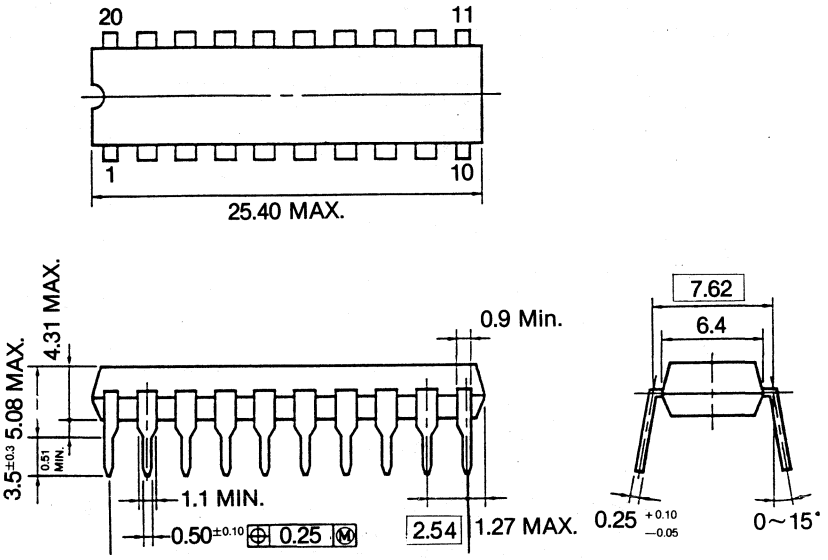


Write Cycle No. 2 ($\overline{CS}$ Controlled) (5)



Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} +200 mV and V_{OH} -200 mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimension of μPD4311C
(20 Pin Plastic Dip)
(Units: mm)



Note: 1. ⊕ 0.25 M: The cernter of each lead can be shifted within the Tolerance of 0.25 mm for both Sides.
2. 2.54 7.62: Figure in [ ] means Typical Figure.

16,384 BIT STATIC CMOS RAM

DESCRIPTION

The μPD4314C is a high speed, low power 4,096 words by 4 bit static CMOS RAM fabricated with short channel silicon-gate CMOS process. The μPD4314C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD4314C requires no clock or refreshing to operate.
Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 35ns, 45ns and 55ns.
The μPD4314C is packaged in a 20-pin plastic Dual In-line Package (DIP) used with the standard JEDEC pin configuration.

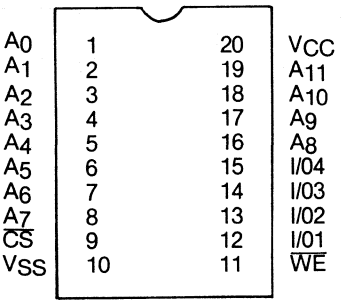
FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or refreshing required
- TTL Compatible — All Inputs and Outputs
- Common I/O Capability
- Three-State Output
- Fast Access Time

μPD4314C-35	35ns MAX
μPD4314C-45	45ns MAX
μPD4314C-55	55ns MAX

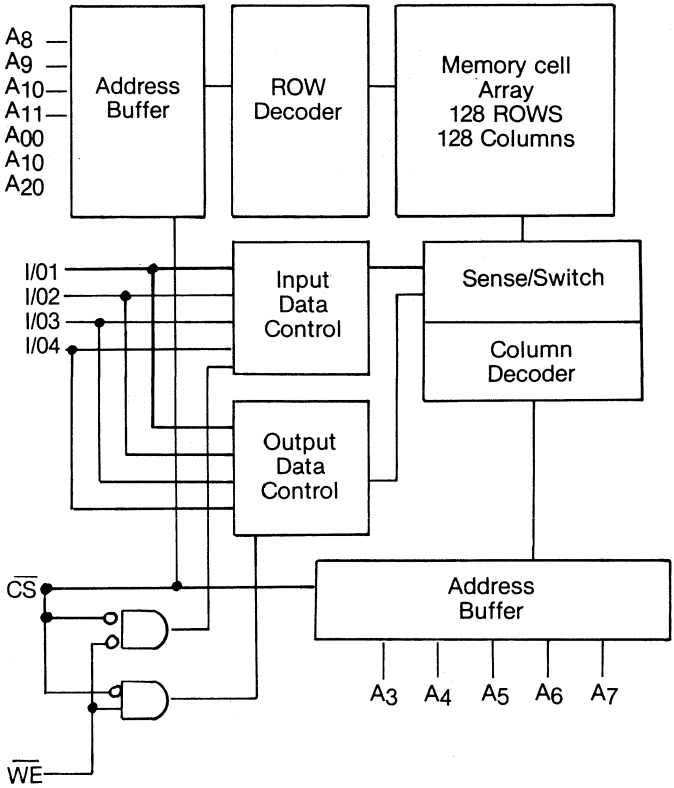
- Low Standby Current 20mA Max.
- Low Active Current 70mA Max.
- Standard 300mil 20-pin Plastic DIP

Pin Configuration and Function



A_0-A_{11}	Address Inputs
I/01-I/04	Data-Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	Dout	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0V MIN. at 20ns pulse width MAX.

Recommended DC Operating Conditions (T_A = 0° to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

Note (1) V_{IL} = −3.0V Min. at 20ns pulse width max.

Capacitance (T_A = 25°C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
I/O Capacitance	C_{DOUT}	V_{DOUT} = 0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics ($T_a = 0°$ to 70°C, $V_{CC} = 5V \pm 20\%$)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim V_{CC}$, V_{CC} = Max.	−2		2	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0 \sim V_{CC}$, $\overline{CS} = V_{IH}$, V_{CC} = Max.	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, I_{DOUT} = 0mA			80	mA
Standby Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			20	mA
	I_{SB1}	$\overline{CS} = V_{CC}$ −0.2V, $V_{IN} < 0.2V$ or $V_{IN} > V_{CC}$			2	mA
Output low Voltage	I_{OL}	I_{OL} = 8.0mA			0.4	V
Output High Voltage	I_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

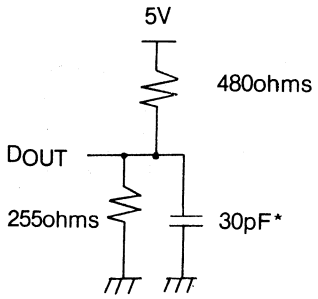


Figure 1 Output Load

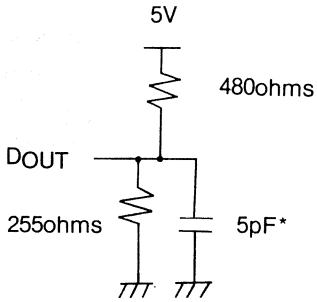


Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

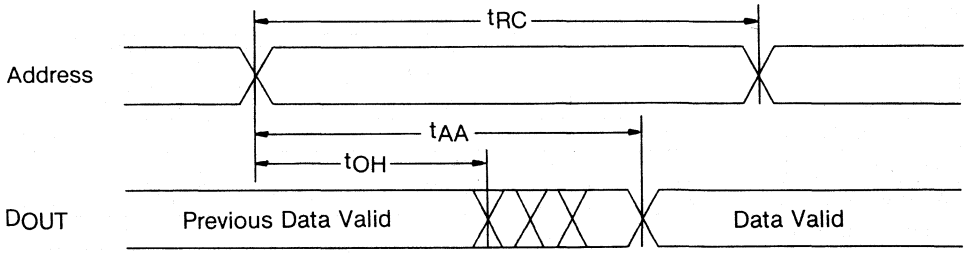
*Including Scope and jig

AC Characteristics (Ta = 0° to 70°C, V_{CC} = 5V±10%)
Read Cycle

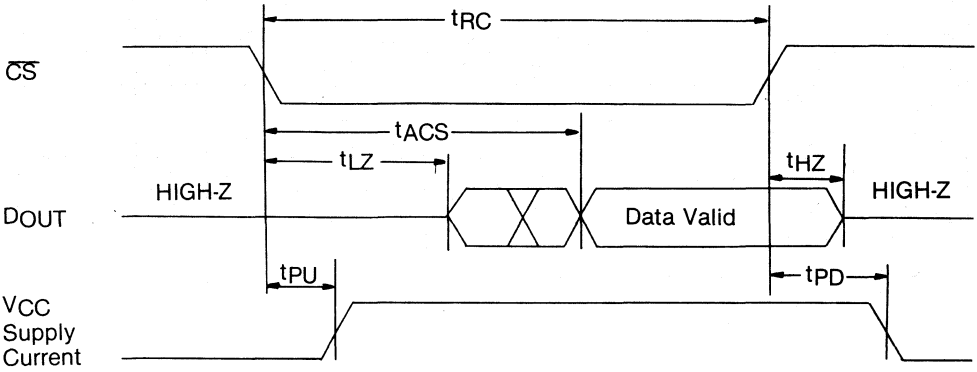
Parameter	Symbol	μPD4314C —35		μPD4314C —45		μPD4314C —55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	20	0	25	0	30	ns
Chip Selection to Power-up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Down Time	t_{PD}	0	35	0	45	0	55	ns

Read Cycle Waveforms

Read Cycle No. 1
(Address Access) (4) (5)



Read Cycle No. 2
Chip Select Access) (4) (6)



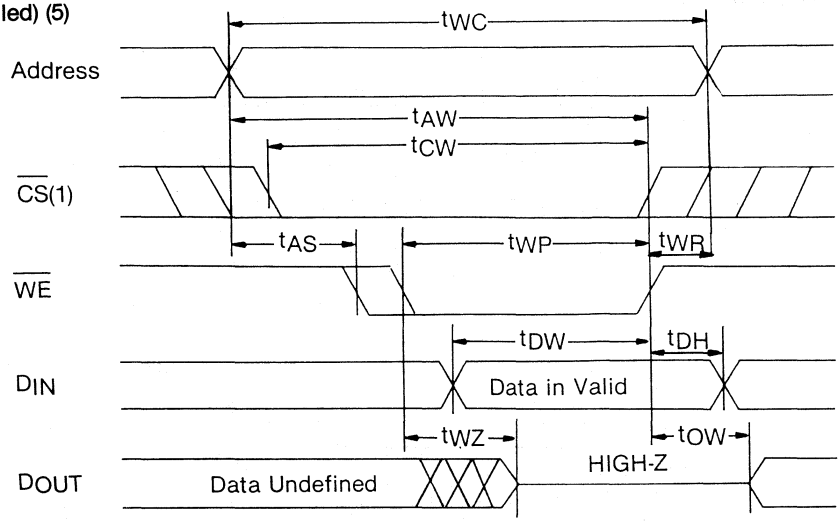
Notes: (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
(3) Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified load in Figure 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continuously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

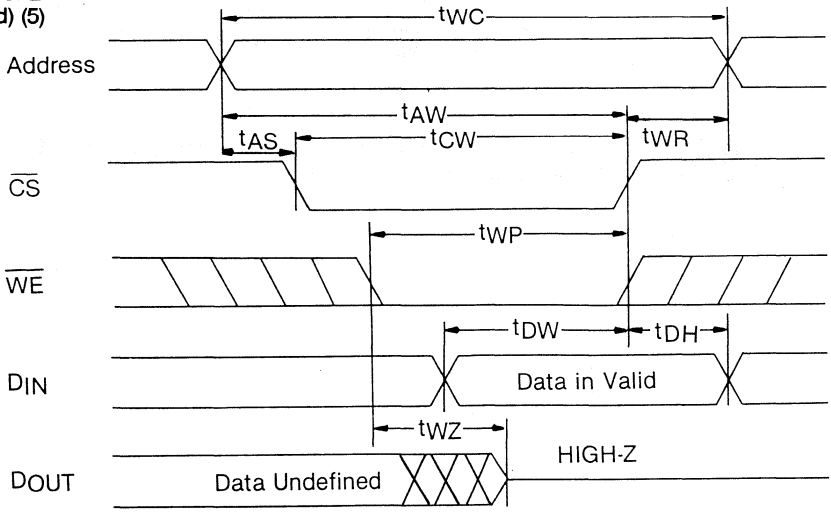
Parameter	Symbol	μPD4314C −35		μ4314C −45		μPD4314C −55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	$t_{WC(2)}$	35		45		55		ns
Chip Selection to End of Write	t_{CW}	35		40		45		ns
Address Valid to End of Write	t_{AW}	35		40		45		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	30		40		50		ns
Write Recovery Time	t_{WR}	5		5		5		ns
Data Valid to End of Write	t_{DW}	20		25		30		ns
Data hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	$t_{WZ(3)}$	0	20	0	25	0	30	ns
Output Active from End of Write	$t_{OW(4)}$	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1
($\overline{WE}$ Controlled) (5)

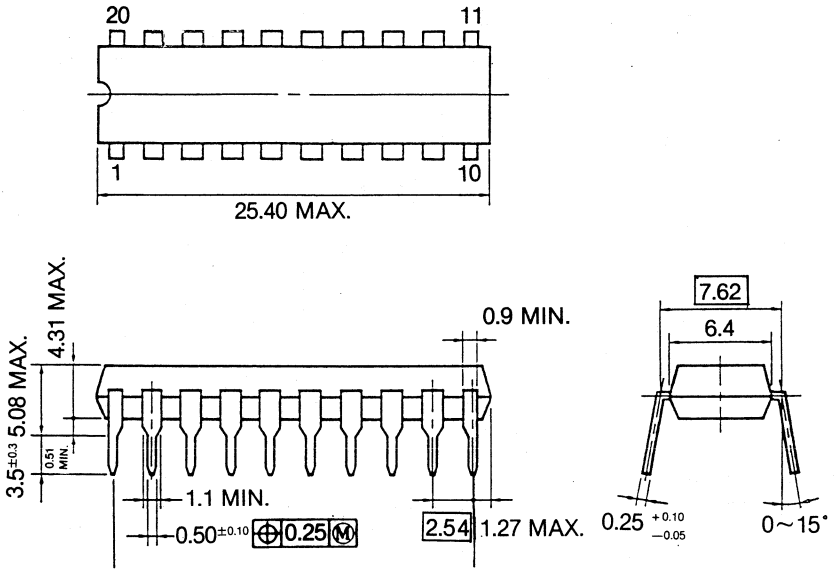


Write Cycle No. 2
($\overline{CS}$ Controlled) (5)



Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH} −200mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimension of 4314C
(20 Pin Plastic DIP)
Units: mm



Note: 1. ⊕ 0.25 M: The cernter of each lead can be shifted within the Tolerance of 0.25 mm for both Sides.
2. 2.54 7.62: Figure in ☐ means Typical Figure.

High Speed 2048 x 8 Bit Static CMOS RAM

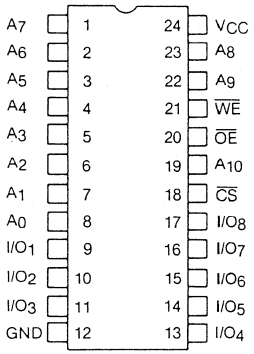
Description

The μPD446C/D/G is a high speed, low power, 2048 words by 8 bits static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD446C/D/G a verly low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CS}$ equals V_{CC} independently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2 volts.
The μPD446C/D is packaged in a standard 24-pin dual-in-line package and plug-in compatible with 16K EPROMs.
The μPD446G is packed in a miniflat package providing high density application.

Features

- Single + 5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and Outputs
- Common I/O Using Three-State Output
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Max Access / Min Cycle Times Down to 150 ns
- Low Power Dissipation - 38 mA Max Active / 10 μA Max Standby
- Data Retention Voltage - 2 V Min
- Operating Temperature Range - —40 to 85 °C
- Standard 24-pin Plastic and Ceramic Packages (μPD446C/D)
- Plug-in Compatible with 16K EPROMs (μPD446C/D)
- L-Version (1.0 μA MAX Standby at 60 °C) for Battery Backup Operation μPD446C/D-L

Pin Configuration and Funktion

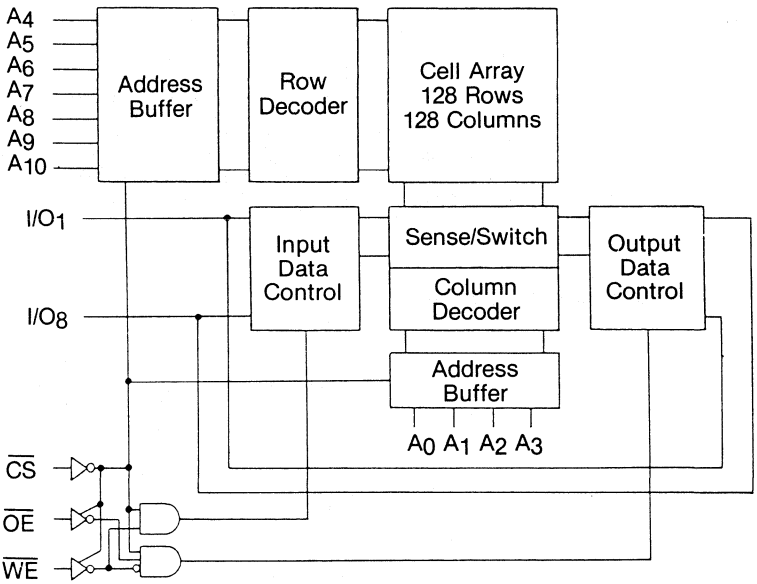


A_0 - A_{10}	Address Input
I/O_1 - I/O_8	Data Input / Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
GND	Ground

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	X	Not Selected	HZ	Standby
L	H	H	Not Selected	HZ	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	DIN	Active

Block Diagram



Absolute Max. Ratings

Supply Voltage	7.0 V
Input or Output Voltage Supplied	−0.3 to V_{CC} + 0.3 V
Storage Temperature Range	−55 to 125 °C
Operating Temperature Range	−40 to 85 °C

Comment: Stress above those listed under »Absolute Maximum Ratings« may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (Ta = —40 to 85 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	—0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	

DC Characteristics (Ta = —40 to 85 °C, V_{CC} = 5V ±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=0\sim V_{CC}$			1	μA
I/O Leakage Current	I_{LO}	$V_{I/O}=0\sim V_{CC}$ $\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$			1	μA
Operating Supply Current	I_{CCA1}	$\overline{CS}=V_{IL}$, $I_{I/O}=0$, Min. Cycle		(1)	(1)	μA
Operating Supply Current	I_{CCA2}	$\overline{CS}=V_{IL}$, $I_{I/O}=0$, DC Current		5	10	μA
Standby Supply Current	I_{CCS}	$\overline{CS}=V_{CC}-0.2V$, $V_{IN}=0\sim V_{CC}$		0.02	(2)	μA
Output Low Voltage	V_{OL}	$I_{OL}=2.0mA$			0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4			V

Notes (1)

μPD446C/D-3/3L	25mA TYP	38mA MAX
μPD446C/D-2/2L	20mA TYP	30mA MAX
μPD446C/D-1/1L	18mA TYP	26mA MAX
μPD446C/D-0/0L	12mA TYP	18mA MAX

Notes (2)

μPD446C/D-3L/2L/1L/0L	Ta = 25 °C	0.2μA MAX
	Ta = 60 °C	1.0μA MAX
	Ta = 85 °C	10μA MAX
μPD446C/D-3/2/1/0	Ta = 25 °C	1.0μA MAX
	Ta = 60 °C	5.0μA MAX
	Ta = 85 °C	10μA MAX

Capactance Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	8	

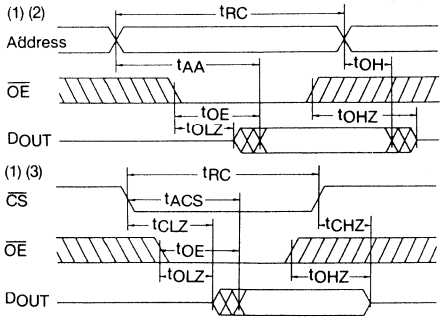
AC Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Pulse Rise and Fall Time	10ns
Timing Reference Levels	1.5V
Output Load	1TTL + 100pF

AC Characteristics (Ta = −40 to 85°C, V_{CC} = 5V±10%)
Read Cycle

		D446C/D-3/-3L D446G-15		D446C/D-2/-2L D446G-20		D446C/D-1/-1L D446G-25		D446C/D-0/-0L D446G-45		
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	t_{RC}	150		200		250		450		ns
Address Access Time	t_{AA}		150		200		250		450	ns
Chip Select Access Time	t_{ACS}		150		200		250		450	ns
Output Enable to Output Valid	t_{OE}		75		100		120		150	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Selection to Output in LZ	t_{CLZ}	10		10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	5		5		5		5		ns
Chip Deselection to Output in HZ	t_{CHZ}		50		60		80		100	ns
Output Disable to Output in HZ	t_{OHZ}		50		60		80		100	ns

READ CYCLE TIMING CHART

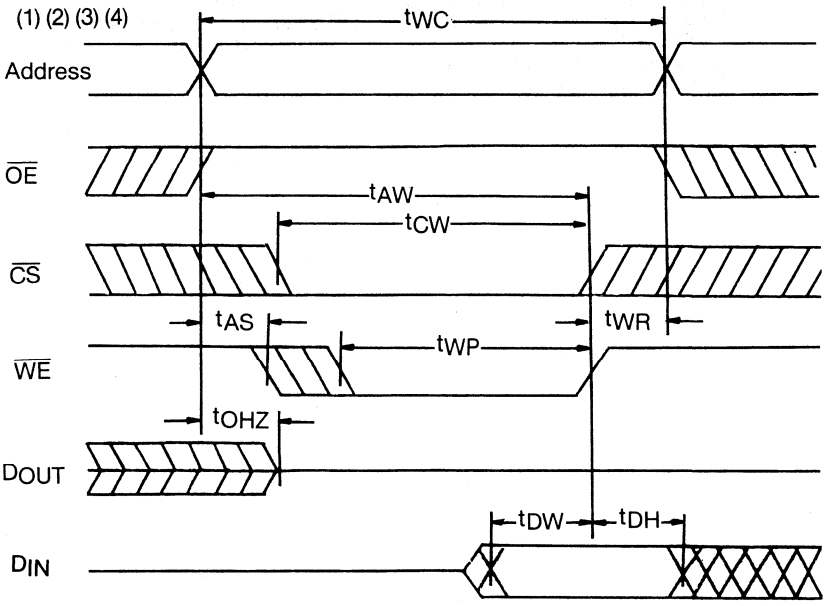


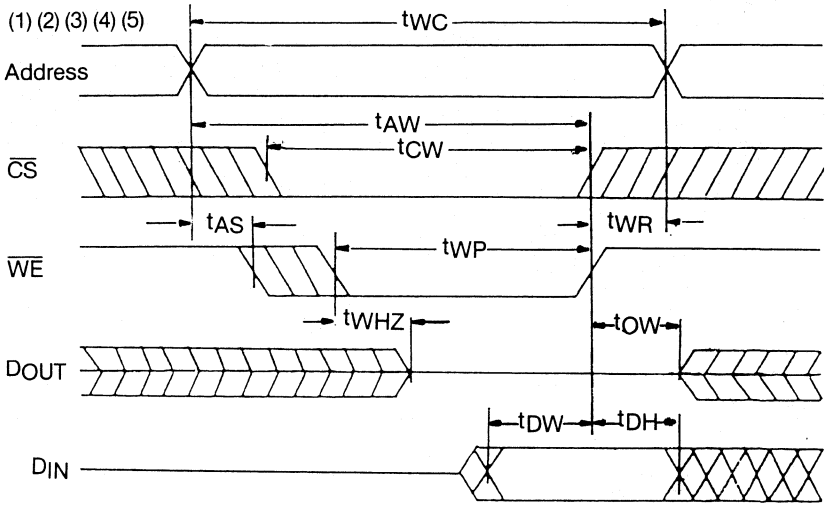
Notes (1) WE is high for read cycles.
(2) Device is continuously selected, $\overline{CS}$ = V_{IL}.
(3) Address valid aprior to or coincident with $\overline{CS}$ transition low.

Write Cycle

Parameter	Symbol	D446C/D-3/-3L D446G-15		D446C/D-2/-2L D446G-20		D446C/D-1/-1L D446G-25		D446C/D-0/-0L D446G-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{RC}	150		200		250		450		ns
Chip Selection to End of Write	t_{CW}	120		150		180		210		ns
Address Valid to End of Write	t_{AW}	120		150		180		210		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		50		60		80		100	ns
Output Active from End of Write	t_{CW}	10		10		10		10		ns

Write Cycle Timing Chart





Notes (1) $\overline{WE}$ must be high during all address transition.
(2) A write occurs during the overlab of a low $\overline{CS}$ ans a low $\overline{WE}$.
(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(4) If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state
(5) $\overline{OE}$ is continuously low.

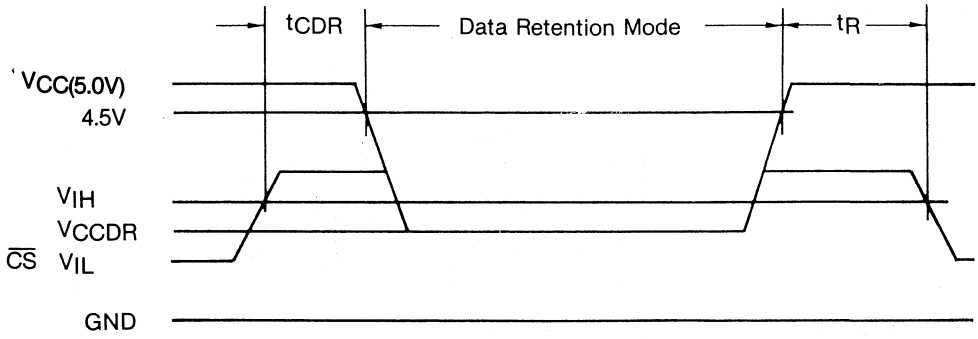
Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
V_{CC} for Data Retention	V_{CCDR}	$V_{IN} = 0 \sim V_{CC}$, $\overline{CS} \geqq V_{CC}-0.2V$	2.0			V
Data Retention Current	I_{CCDR}	$V_{IN}=0 \sim V_{CC}$, $\overline{CS} \geqq V_{CC}-0.2V$, $V_{CC}=3.0V$		0.01	(1)	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

Notes (1)

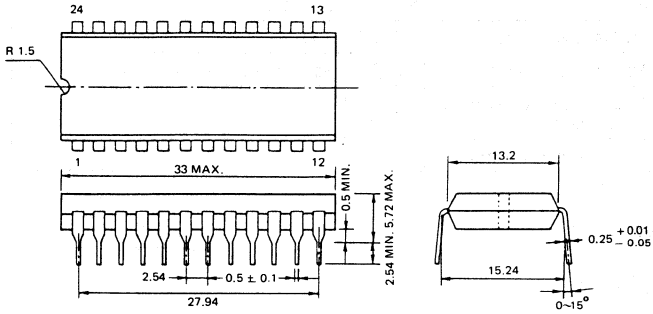
μPD446C/D-3L/2L/1L	Ta = 25 °C	0.2μA Max.
	Ta = 60 °C	1.0μA Max.
	Ta = 85 °C	10μA Max.
μPD446C/D-3/2/1	Ta = 25 °C	1.0μA Max.
	Ta = 60 °C	5.0μA Max.
	Ta = 85 °C	10μA Max.

Low V_{CC} Data Retention Timing Chart

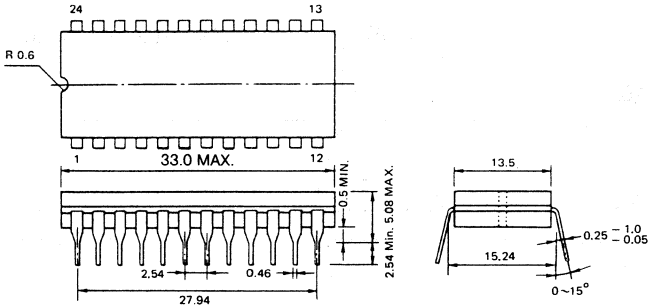


Package Outline

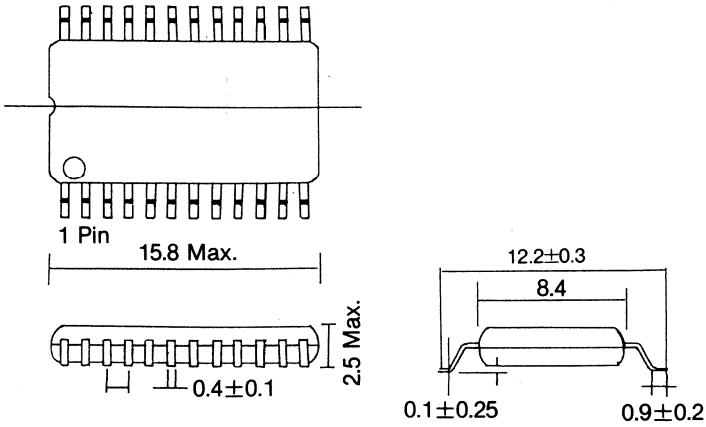
μPD446C Plastic



μPD446D Ceramic



μPD446G Miniflat



High Speed 2048 x 8 Bit Static CMOS RAM

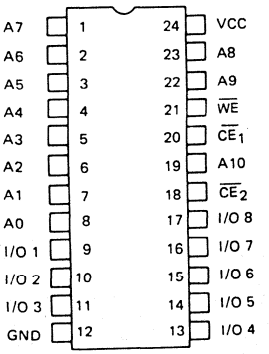
Description

The μPD449C/G is a high speed, low power, 2048 words by 8 bits static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD449C/G a very low oerating power device which requires no clock or refreshing to operate. Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE}_1$ or $\overline{CE}_2$ equals V_{CC} indepently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2 volts.
The μPD449C is packaged in a standard 24-pin dual-in-line package and plug-in compatible with 16K EPROMs.
The μPD449G is packaged in a mini flat package providing high density application.

Features

- Single + 5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and Outputs
- Common I/O Using Three-State Output
- Two Chip Enable Inputs for Battery Backup Application
- Max Access / Min Cycle Times Down to 150 ns
- Low Power Dissipation - 38mA Max Active / 10 μA Max Standby
- Data Retention Voltage - 2V Min
- Operating Temperature Range - —40 to 85 °C
- Standard 24-pin Plastic Package (μPD449C)
- Plug-in Compatible with 16K EPROMs (μPD449C)
- Mini Flat Package for High Density Application (μPD449G)
- L Version (1.0μA MAX Standby at 60 °C) for Battery Backup Operation (μPD449C/G-L)

Pin Configuration and Function

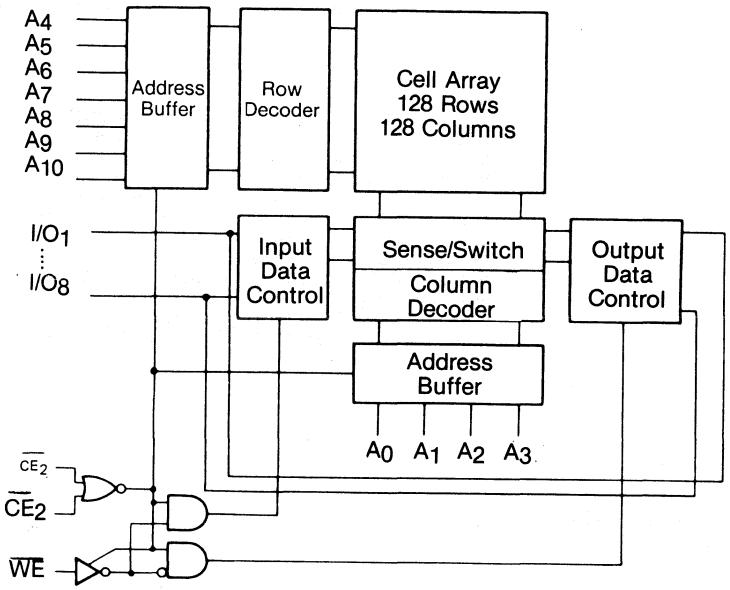


A_0 - A_{10}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Input
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
GND	Ground

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	Output	I_{CC}
X	H	X	Not Selected	HZ	Standby
H	L	X	Not Selected	HZ	Standby
L	L	H	Read	D_{OUT}	Active
L	L	L	Write	D_{IN}	Active

Block Diagram



Absolute Maximum Ratings

Supply Voltage	7.0 V
Input or Output Voltage Supplied	−0.3 to V_{CC} + 0.3 V
Storage Temperature Range	−55 to 125 °C
Operating Temperature Range	−40 to 85 °C

Comment: Stress above those listed under »Absolute Maximum Ratings« may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (Ta = —40 to 85°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	—0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V

DC Characteristics (Ta = —40 to 85°C, V_{CC} = 5V±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN}=0\sim V_{CC}$			1	μA
I/O Leakage Current	I_{LO}	$V_{I/O}=0\sim V_{CC}$ $\overline{CE1}$ or $\overline{CE2}=V_{IH}$ or $\overline{WE}=V_{IL}$			1	μA
Operating Supply Current	I_{CCA1}	$\overline{CE1}$ and $\overline{CE2}=V_{IL}$, $I_{I/O}=0$, Min. Cycle		(1)	(1)	mA
Operating Supply Current	I_{CCA2}	$\overline{CE1}$ and $\overline{CE2}=V_{IL}$, $I_{I/O}=0$, DC Current		5	10	mA
Standby Supply Current	I_{CCS}	$\overline{CE1}$ or $\overline{CE2}\geqq V_{CC}$ -0.2V, $V_{IN}=0\sim V_{CC}$		0.02	(2)	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = —1.0mA	2.4			V

Notes (1)

μPD449C-3/3L	μPD449G-15/15L	25mA TYP	38mA MAX
μPD449C-2/2L	μPD449G-20/20L	20mA TYP	30mA MAX
μPD449C-1/1L	μPD449G-25/25L	18mA TYP	26mA MAX
μPD449C-0/0L	μPD449G-45/45L	12mA TYP	18mA MAX

Notes (2)

μPD449C-3L/2L/1L/0L	μPD449G-15L/20L/25L/45L	Ta = 25°C	0.2μA MAX
		Ta = 60°C	1.0μA MAX
		Ta = 85°C	10μA MAX
μPD449C-3/2/1/0	μPD449G-15/20/25/45	Ta = 25°C	1.0μA MAX
		Ta = 60°C	5.0μA MAX
		Ta = 85°C	10μA MAX

Capacitance Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	8	pF

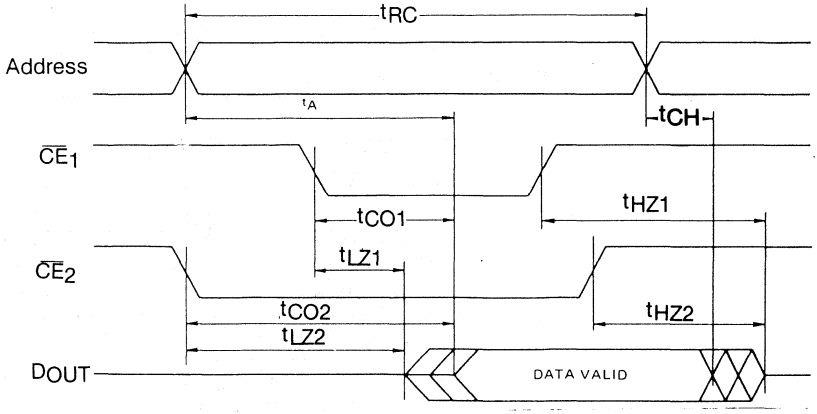
AC Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Pulse Rise and Fall Time	10ns
Timing Reference Levels	1.5V
Output Load	1TTL + 100pF

AC Characteristics (Ta = 40 to 85°C, V_{CC} = 5V±10%)
Read Cycle

Parameter	Symbol	D449C-3 D449G-15		D449C-2 D449G-20		D449C-1 D449G-25		D449C-0 D449G-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150		200		250		450		ns
Access Time	t_A		150		200		250		450	ns
Chip Enable ($\overline{CE1}$) to Output Valid	t_{CO1}		150		200		250		450	ns
Chip Enable ($\overline{CE2}$) to Output Valid	t_{CO2}		150		200		250		450	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Enable ($\overline{CE1}$) to Output in LZ	t_{LZ1}	5		5		5		5		ns
Chip Enable ($\overline{CE2}$) to Output in LZ	t_{LZ2}	10		10		10		10		ns
Chip Enable ($\overline{CE1}$) to Output in HZ	t_{HZ1}		50		60		80		100	ns
Chip Enable ($\overline{CE2}$) to Output in HZ	t_{HZ2}		50		60		80		100	ns

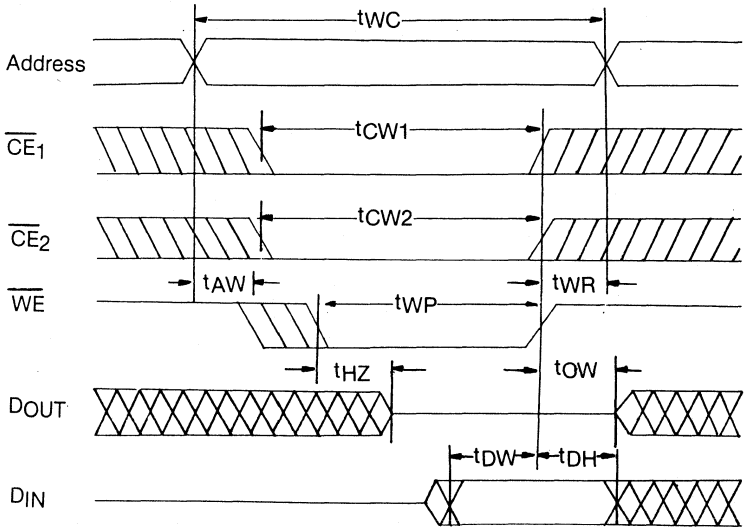
Read Cycle Timing Chart



Write Cycle

Parameter	Symbol	D449C-3 D449G-15		D449C-2 D449G-20		D449C-1 D449G-25		D449C-0 D449G-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{RC}	150		200		250		450		ns
Chip Enable ($\overline{CE1}$) to End of Write	t_{CW1}	120		150		180		210		ns
Chip Enable ($\overline{CE2}$) to End of Write	t_{CW2}	120		150		180		210		ns
Address Set-up Time	t_{AW}	0		0		0		0		ns
Write Pulse Width	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		50		60		80		100	ns
Output Active from End of Write	t_{CW}	10		10		10		10		ns

Write Cycle Timing Chart



Low VCC Data Retention Characteristics (Ta = —40 to 85 °C)

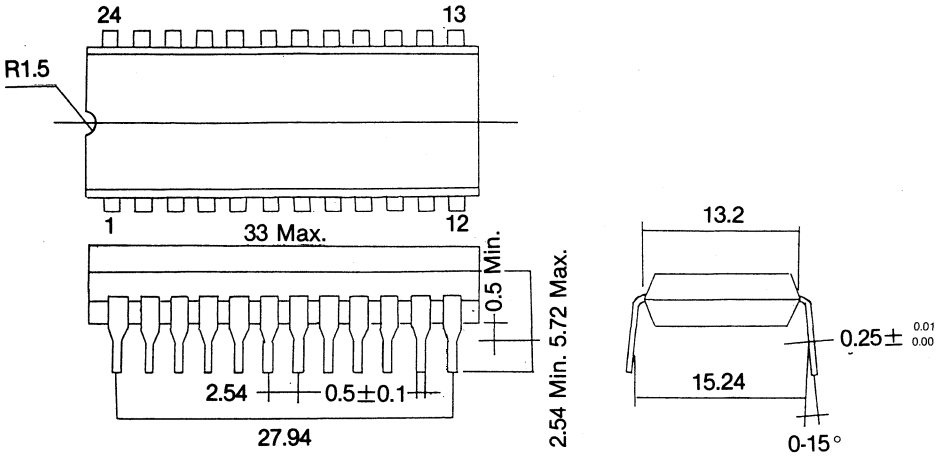
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
VCC for Data Retention	VCCDR	CE1 or CE2 ≧ VCC − 0.2V, VIN = 0 ~ VCC	2.0			V
Data Retention Current	ICCDR	CE1 or CE2 ≧ VCC − 0.2V, VIN = 0 ~ VCC VCC = 3.0V		0.01	(1)	μA
Chip Deselection to Data Retention Mode	tCDR		0			ns
Operation Recovery Time	tR		tRC			ns

Notes (1)

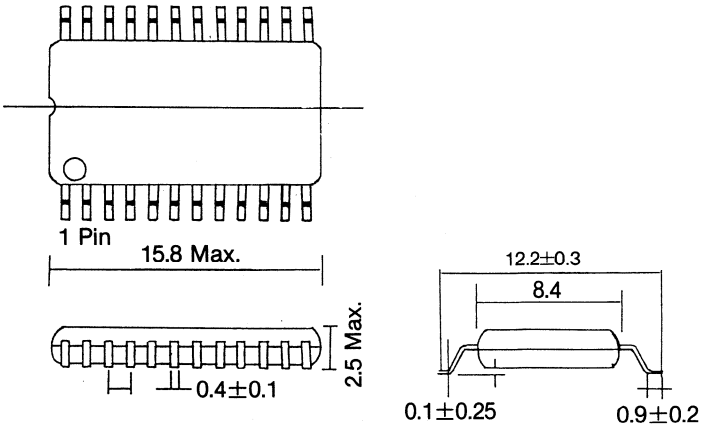
μPD449C-3L/2L/1L/0L	μPD449G-15L/20L/25L/45L	Ta = 25 °C	0.2μA Max.
		Ta = 60 °C	1.0μA Max.
		Ta = 85 °C	10μA Max.
μPD449C-3/2/1/0	μPD449G-15/20/25/45	Ta = 25 °C	1.0μA Max.
		Ta = 60 °C	5.0μA Max.
		Ta = 85 °C	10μA Max.

Package Outline

μPD449C Plastic



μPD449G Mini Flat



High Speed 65,536 BIT Static CMOS RAM

Description

The μPD4361C is a high speed, low power, 65,536 words by 1 bit static CMOS RAM fabricated width short channel silicon-gate CMOS process. The μPD4361C is a low standby power device using n-channel memory cells with polisilicon resistors. Furthermore, an excellent circuitry achieves very high speed and low operating power. The μPD4361C requires no clock or refreshing to operate.
Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 45ns, 55ns and70ns.
Data retention is guaranteed at a power supply voltage as low as 2 volts (μPD4361C-45L/55L/70L)
The μPD4361C is packaged in a 22-pin plastic Dual In-line Package (DIP) used with the standard JEDEC pin configuration.

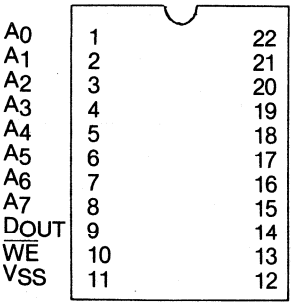
Features

- Single +5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and an Output
- Separated Data Input and Output
- Three-State Output
- Fast Access Time

μPD4361C-45/-45L	45ns Max.
μPD4361C-55/-55L	55ns Max.
μPD4361C-70/-70L	70ns Max.

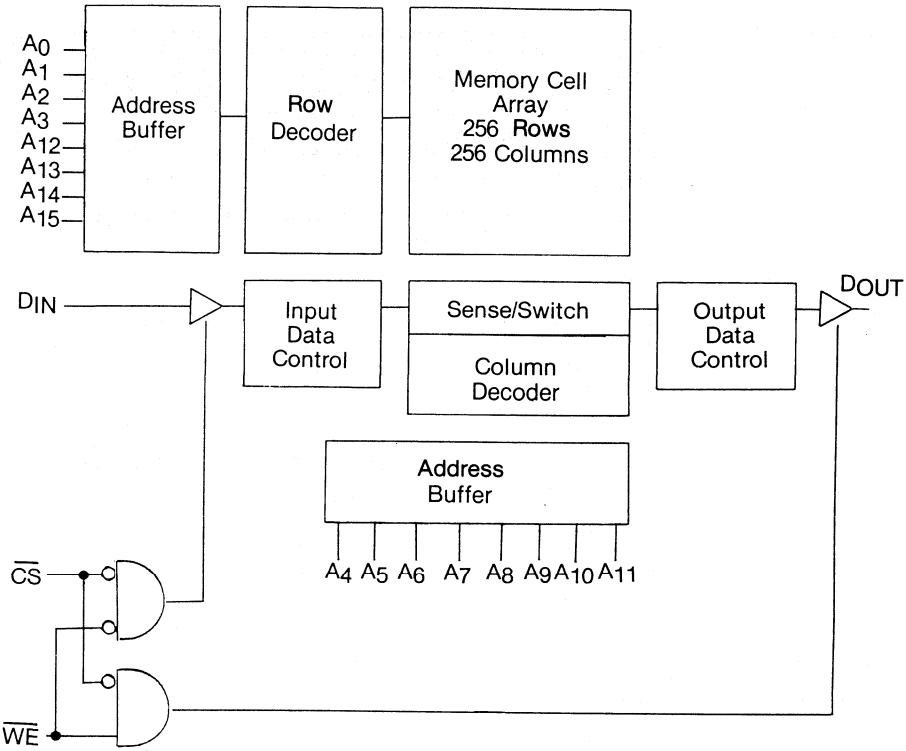
- Low Standby Current 20mA Max.
- Low Active Current 120mA Max.
- 300mil 22-pin Plastic DIP
- Data Retention Voltage -2Vmin. (μPD4361C-45L/55L/70L)
- Same Pin Configuration as JEDEC Standard

Configuration and Function



A_0-A_{15}	Address Inputs
D_{IN}	Data-Input
D_{OUT}	Data-Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Recomended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	*–0.5		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V

* -3.0V min while 20ns pulse width

Capacitance Ta = 25 °C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data-Output Capacitance	C_{DOUT}	V_{DOUT} = 0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0 °C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leake Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	-2		2	μA
Output Leake Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max.	-2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA			120	mA
Standby Supply Current	I_{SB1}	$\overline{CS}$ = V_{CC} – 0.2V $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}$ -0.2V		2	2	V
Output Low Voltage	V_{OL}	I_{OL} = 8,0mA	V		0.4	
Output High Voltage	V_{OH}	I_{OH} = –4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

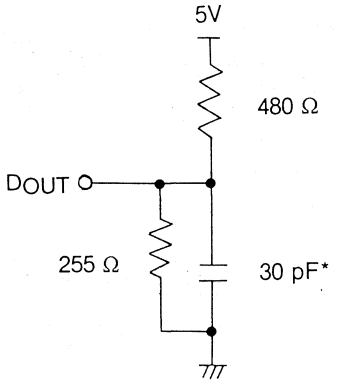


Figure 1 Output Load

*Including Scope and jig

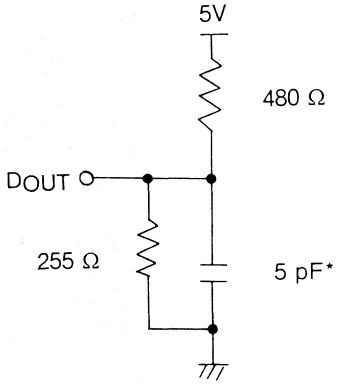


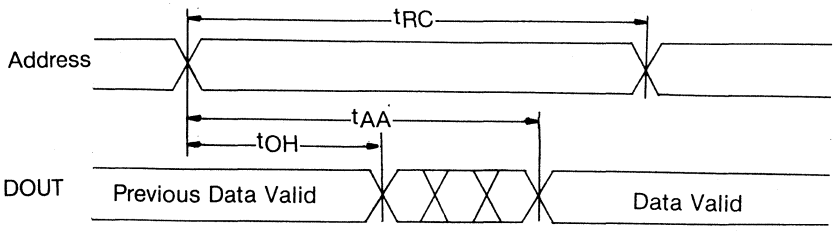
Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

AC Characteristics (Ta = 0 to 70°C V_{CC} = 5V±10%)

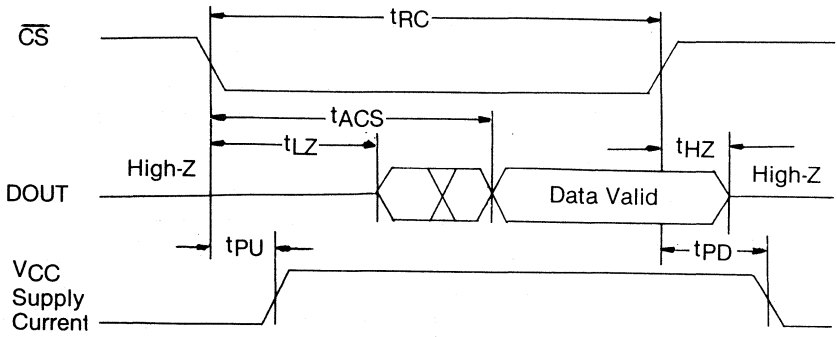
Parameter	Symbol	μPD4361C —45		μPD4361C —55		μ4361C —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC(1)}$	45		55		70		ns
Address Access Time	t_{AA}		45		55		70	ns
Chip Select Access Time	t_{ACS}		45		55		70	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	$t_{LZ(2)}$	5		5		5		ns
Chip Deselection to Output in High Z	$t_{HZ(3)}$	0	25	0	30	0	30	ns
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	40	0	40	ns

Read Cycle Waveforms

Read Cycle No. 1 (Address Access) (4) (5)



Read Cycle No. 2 (Chip Select Access) (4) (6)



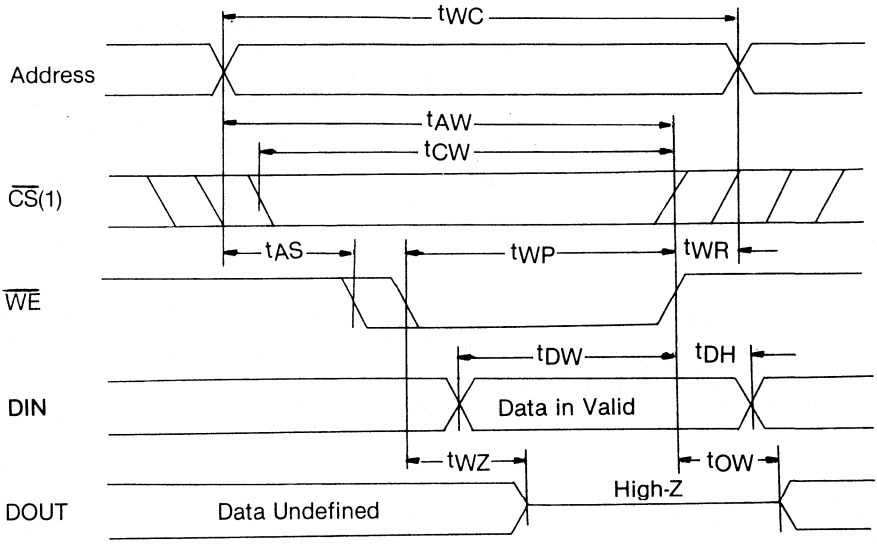
Notes (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200 mV from steady state voltage with specified loading in FIGURE 2.
(3) Transition is measured at V_{OL} + 200mV and V_{OH}-200mV with specified load in FIGURE 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

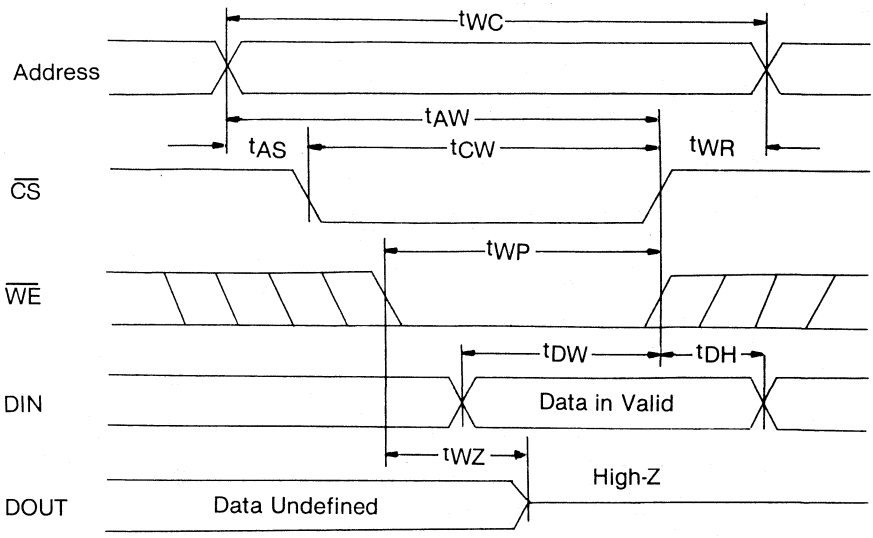
Parameter	Symbol	μPD4361C —45		μPD4361C —55		μPD4361C —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}(2)	45		55		70		ns
Chip Selection to End of Write	t_{CW}	40		50		60		ns
Address Valid to End of Write	t_{AW}	40		50		60		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	25		30		40		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	25		25		30		ns
Data hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	t_{WZ} (3)	0	25	0	25	0	30	ns
Output Active from End of Write	t_{OW} (4)	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1 ($\overline{WE}$ Controlled) (1), (2), (3), (4), (5)



Write Cycle No. 2 ($\overline{CS}$ Controlled) (1), (2), (3), (4), (5)



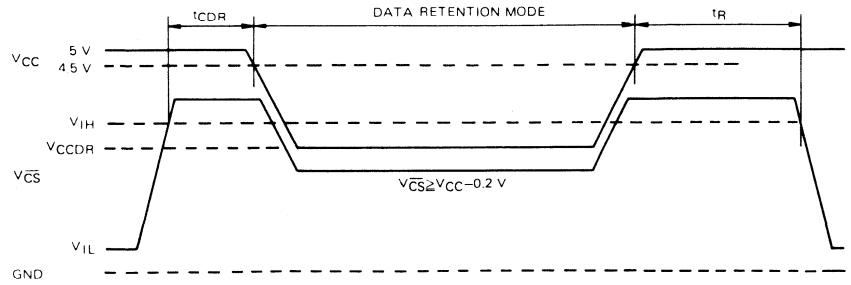
Notes (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH}-200mV with specified loading in FIGURE 2.
(4) Transition is measured ±200mV from steady state voltage with specified loading in FIGURE 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to 70 °C)

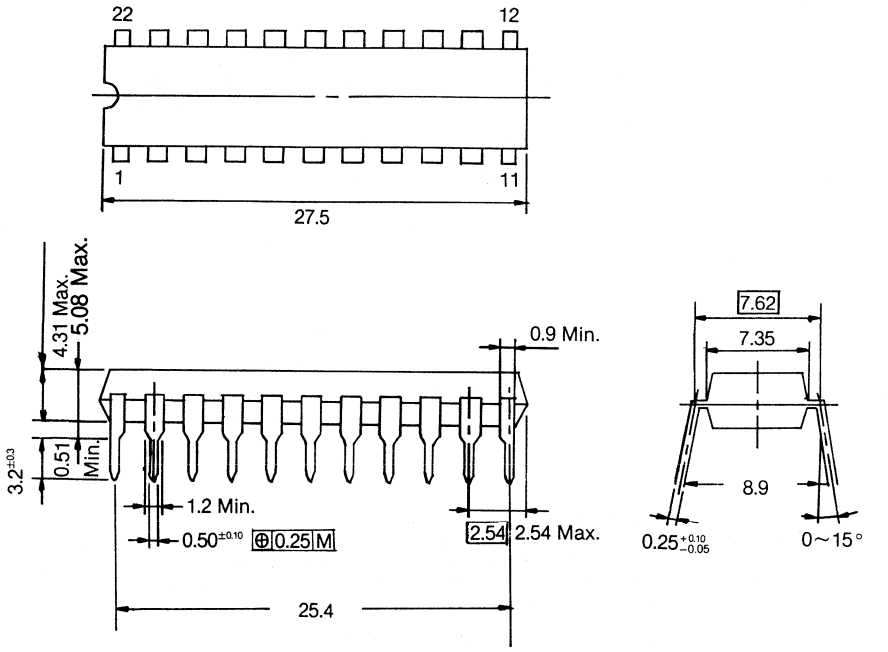
for μPD4361C-45L/-55L/-70L

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR}	2.0		5.5	V	$V_{\overline{CS}} \geq V_{CC}-0.2$ V,
Data Retention Supply Current	I_{CCDR}		1	50*	μA	$V_{IN} \geq V_{CC}-0.2$ V
Chip Deselection to Data Retention Mode	t_{CDR}	0			ns	or 0 V ≤ V_{IN} ≤ 0.2 V
Operation Recovery Time	t_R	t_{RC}			ns	

V_{CC} = 3.0 V



Package Dimension
(Units: mm)



Note: 1. ⊕ 0.25 M: The cernter of each lead can be shifted within the Tolerance of 0.25 mm for both Sides.
2. 2.54 7.62: Figure in [ ] means Typical Figure.

High Speed 65,536 BIT Static CMOS RAM

Description

The μPD4361K is a high speed, low power, 65,536 words by 1 bit static CMOS RAM fabricated with short channel silicon-gate CMOS process. The μPD4361K is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry achieves very high speed and low operating power.
The μPD4361K requires no clock or refreshing to operate.
Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 40ns, 45ns and 55ns.
The μPD4361K is packaged in a 22-pin Leadless Chip Carrier (LCC) used with the standard JEDEC pin configuration.

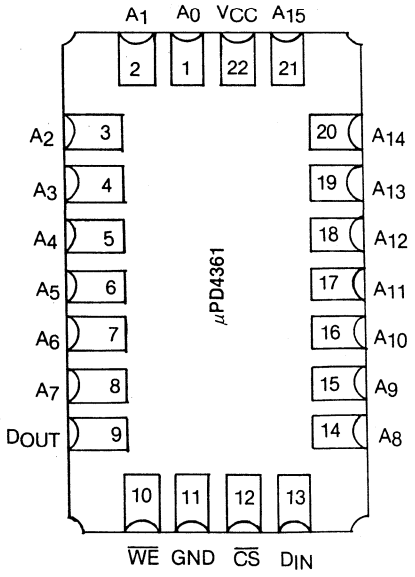
Features

- Single +5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and an Output
- Separated Data Input and Output
- Three-State Output
- Fast Access Time

μPD4361K-40	40ns Max.
μPD4361K-45	45ns Max.
μPD4361K-55	55ns Max.

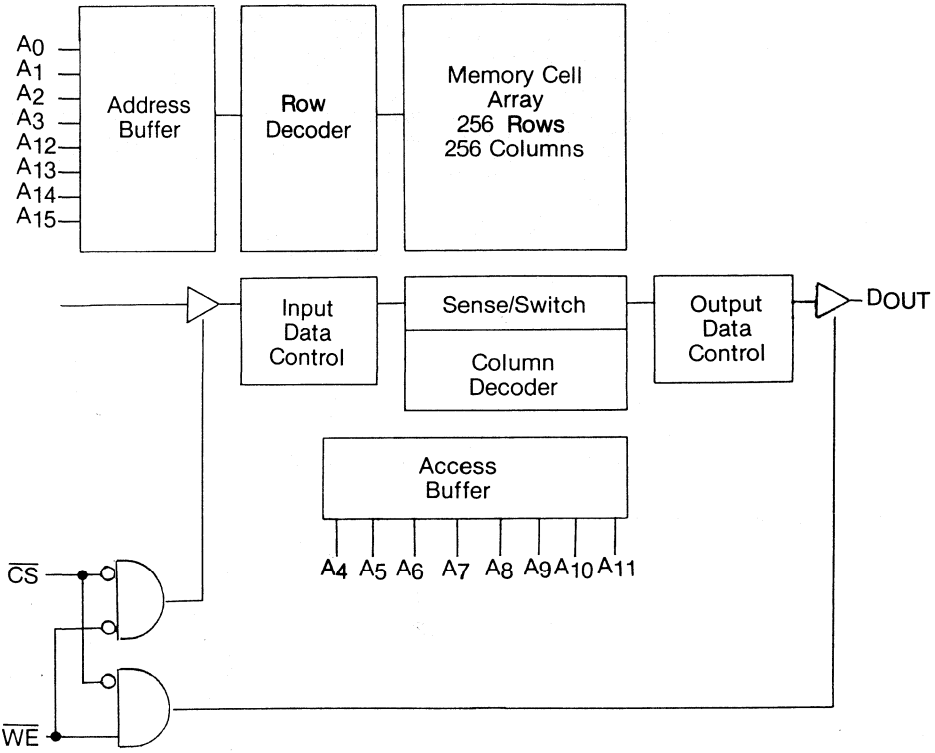
- Low Standby Current 20mA Max.
- Low Active Current 120mA Max.
- 290mil X 490mil 22-pin LCC
- Same Pin Configuration as JEDEC Standard

Configuration and Function



A_0-A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
Operating Temperature	Topr	−10 to 85	°C
Storage Temperature	Tstg	−65 to 150	°C
Power Dissipation	Pd	1.0	W

Recommended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V

Note (1) −3.0V min. while 20ns pulse width

Capacitance Ta = 25 °C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data-Output Capacitance	C_{DOUT}	V_{DOUT}=0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC},			2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{IH}			2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA			120	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V V_{IN} ≤ 0.2V or ≥ V_{CC} −0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	V		0.4	
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

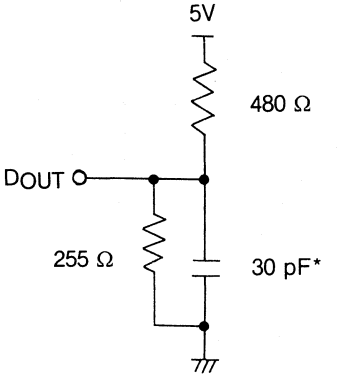


Figure 1 Output Load

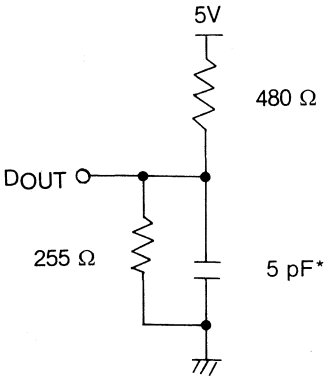


Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

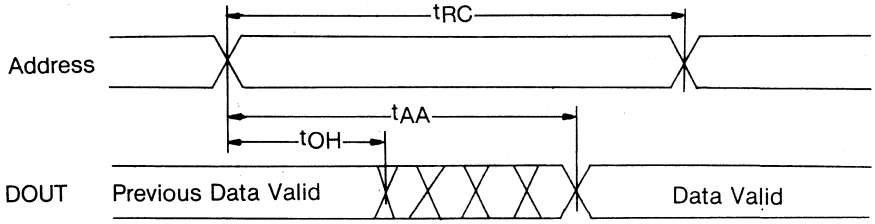
*Including Scope and Jig

AC Characteristics ($T_a = 0$ to 70°C $V_{CC} = 5V \pm 10\%$)

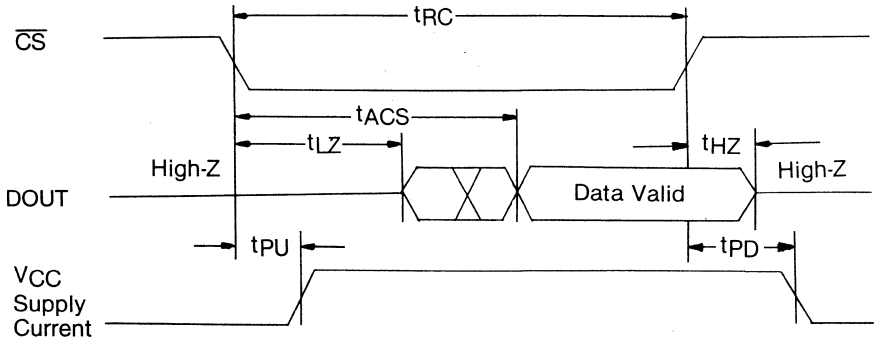
Parameter	Symbol	μPD4361K —40		μPD4361K —45		μ4361K —55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC(1)}$	40		45		55		ns
Address Access Time	t_{AA}		40		45		55	ns
Chip Select Access Time	t_{ACS}		40		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	$t_{LZ(2)}$	5		5		5		ns
Chip Deselection to Output in High Z	$t_{HZ(3)}$	0	22	0	25	0	30	ns
Chip Selection to Power-up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Down Time	t_{PD}	0	27	0	30	0	40	ns

Read Cycle Waveforms

Read Cycle No. 1 (Address Access) (4) (5)



Read Cycle No. 2 (Chip Select Access) (4) (6)



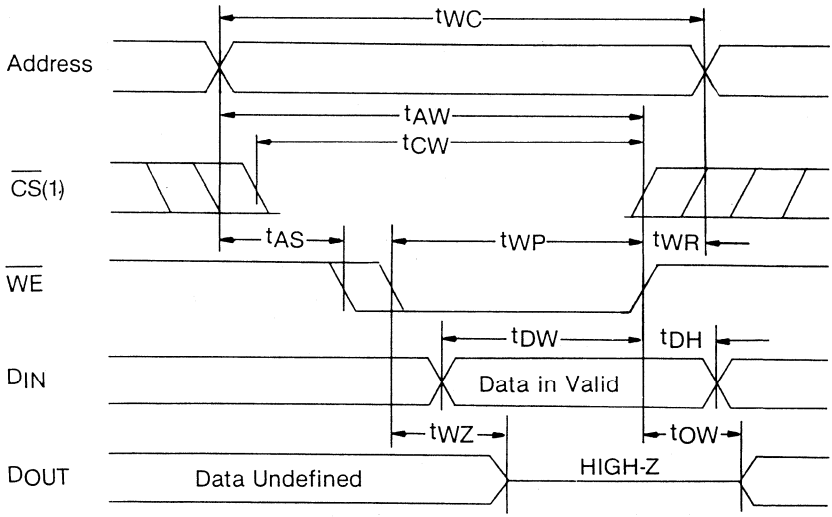
Notes (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200 mV from steady state voltage with specified loading in FIGURE 2.
(3) Transition is measured at V_{OL} + 200mV and V_{OH}-200mV with specified load in FIGURE 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

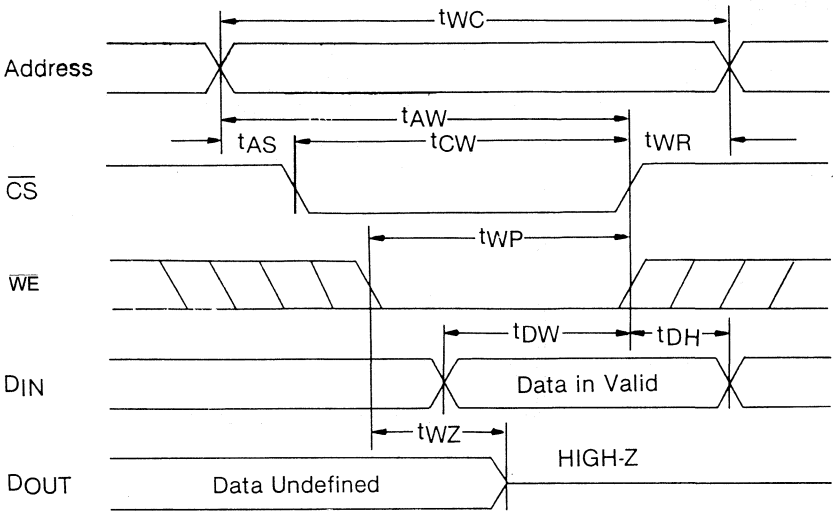
Parameter	Symbol	μPD4361K —40		μPD4361K —45		μPD4361K —55		Unit
		Min.	Max.	Min.	Max,	Min.	Max.	
Write Cycle Time	$t_{WC(2)}$	40		45		55		ns
Chip Selection to End of Write	t_{CW}	37		40		50		ns
Address Valid to End of Write	t_{AW}	37		40		50		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	23		25		30		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	23		25		25		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	$t_{WZ(3)}$	0	22	0	25	0	25	ns
Output Active from End of Write	$t_{CW(4)}$	0		0		0		ns

Write Cycle Waveforms

Write Cycle No.1 ($\overline{WE}$ Controlled) (5)

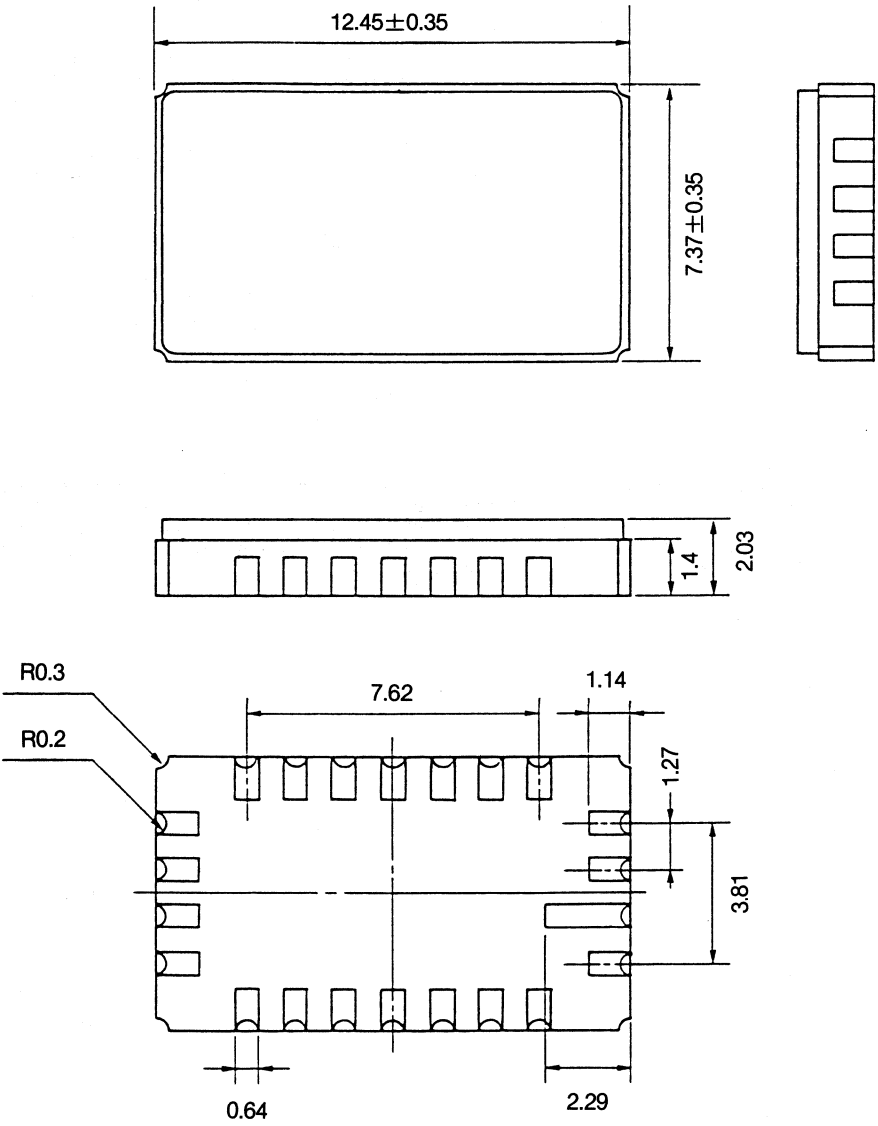


Write Cycle No. 2 ($\overline{CS}$ Controlled) (5)



Notes (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH}-200mV with specified loading in FIGURE 2.
(4) Transition is measured ±200mV from steady state voltage with specified loading in FIGURE 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimension of 4361K
(22 Pads Ceramic LCC)
(Units: mm)



High Speed 65,536 BIT STATIC CMOS RAM

DESCRIPTION

The μPD4362C is a high speed, low power, 16,384 words by 4 bit static CMOS RAM fabricated with short channel silicon-gate CMOS process. The μPD4362C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD4362C requires no clock or refreshing to operate.
Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 45ns, 55ns and 70ns.
The μPD4362C is packaged in a 22-pin plastic Dual In-line Package (DIP) used with the standard JEDEC pin configuration.

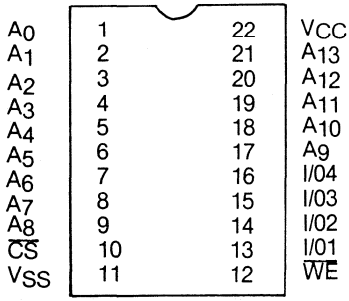
FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or refreshing required
- TTL Compatible — All Inputs and Outputs
- Common I/O Capability
- Three-State Output
- Fast Access Time

μPD4362C-45	45ns MAX
μPD4362C-55	55ns MAX
μPD4362C-70	70ns MAX

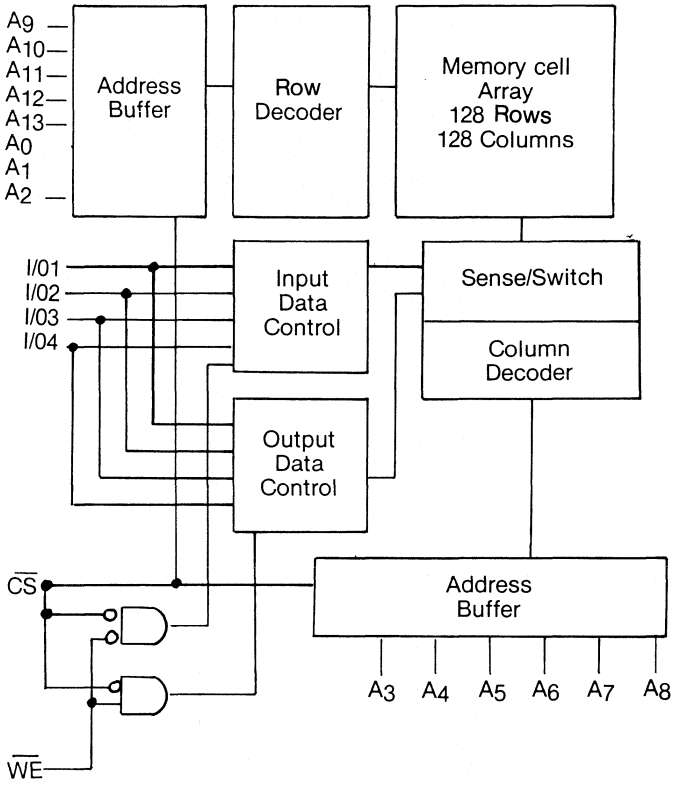
- Low Standby Current 20mA Max.
- Low Active Current 90mA Max.
- Standard 300mil 22-pin Plastic DIP

Pin Configuration and Function



A_0-A_{13}	Address Inputs
I/01-I/04	Data-Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	Dout	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0V min. while 20ns pulse width.

Recommended DC Operating Conditions (T_A = 0° to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

Note (1) V_{IL} = −3.0V Min. while 20ns pulse width.

Capacitance (T_A = 25°C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
I/O Capacitance	C_{DOUT}	V_{DOUT} = 0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (T_a = 0° to 70°C, V_{CC} = 5V±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0~V_{CC},	−2		2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0~V_{CC}, $\overline{CS}$ = V_{IH},	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA			90	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V, V_{IN} ≤ 0.2V or ≥ V_{CC} −0.2V			2	mA
Output low Voltage	V_{OL}	I_{OL} = 8.0mA			0.4	V
Output High Voltage	I_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

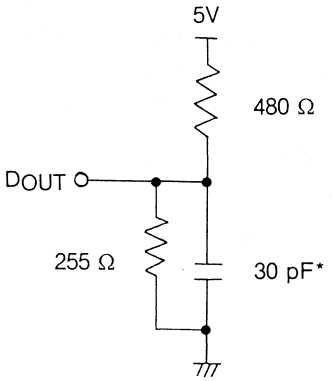


Figure 1 Output Load

*Including Scope and jig

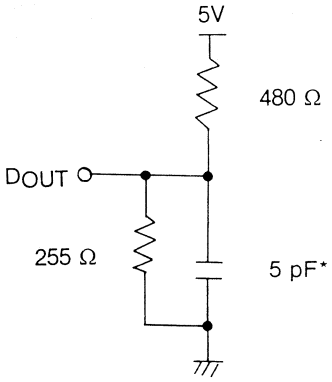


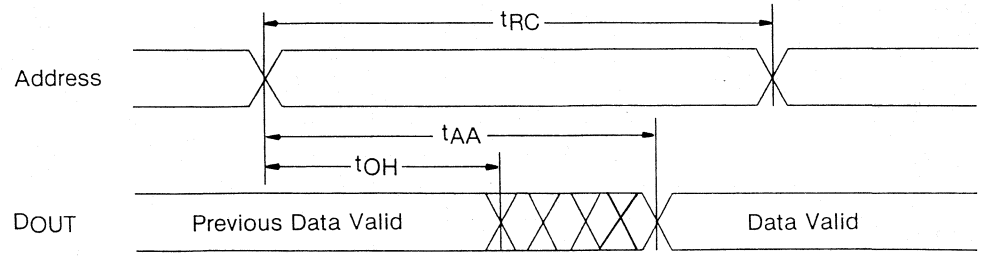
Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

AC Characteristics ($T_a = 0°$ to $70°C$, $V_{CC} = 5V \pm 10\%$)
Read Cycle

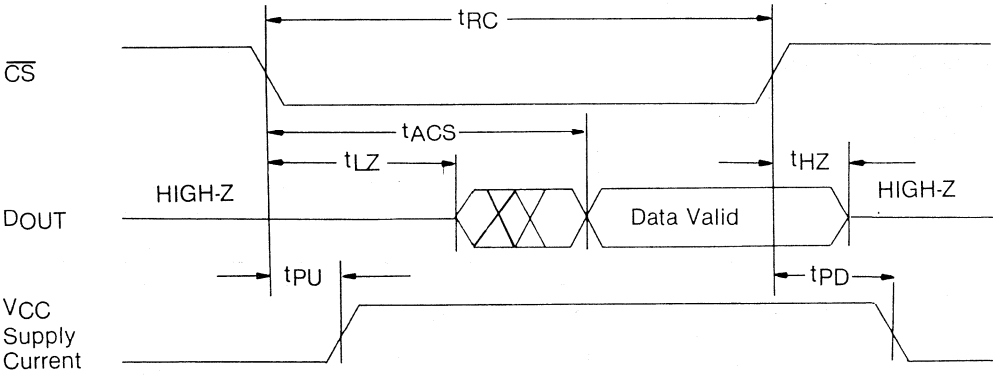
Parameter	Symbol	μPD4362C —45		μPD4624C —55		μPD4624C —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	45		55		70		ns
Address Access Time	t_{AA}		45		55		70	ns
Chip Select Access Time	t_{ACS}		45		55		70	ns
Output hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	25	0	25	0	30	ns
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns
Chip Selection to Power-Down Time	t_{PD}	0	45	0	55	0	55	ns

Read Cycle Waveforms

Read Cycle No. 1
(Address Access) (4) (5)



Read Cycle No. 2
(Chip Select Access) (4) (6)



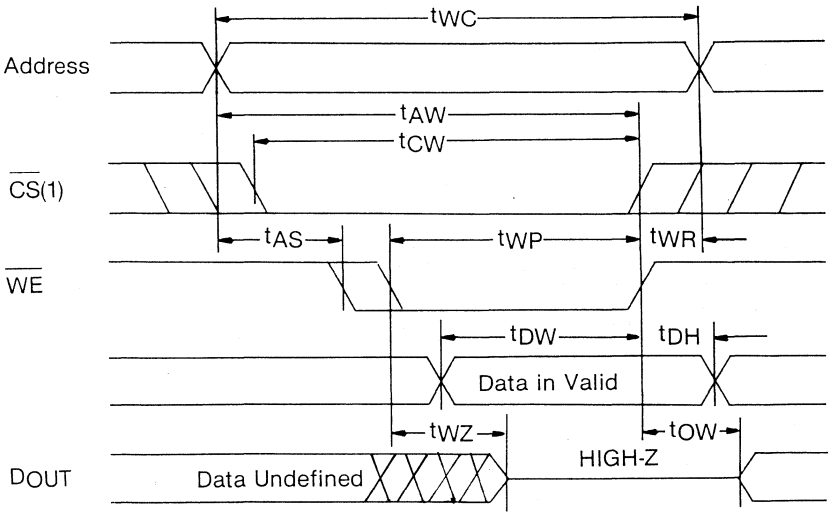
Notes: (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
(3) Transition is measured at V_{OL} + 200mV and V_{OH} −200mV with specified load in Figure 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continuously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

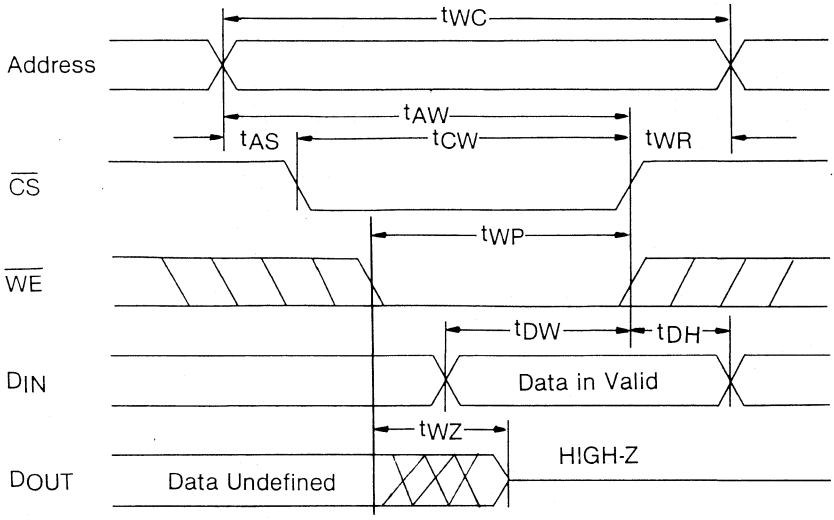
Parameter	Symbol	μPD4362C —45		μ4362C —55		μPD4362C —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}(2)	45		55		70		ns
Chip Selection to end of Write	t_{CW}	40		50		60		ns
Address Valid to end of Write	t_{AW}	40		50		60		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	40		50		60		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to end od Write	t_{DW}	20		25		30		ns
Data hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	t_{WZ}(3)	0	20	0	25	0	30	ns
Output Active from end of Write	t_{OW}(4)	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1
($\overline{WE}$ Controlled) (5)

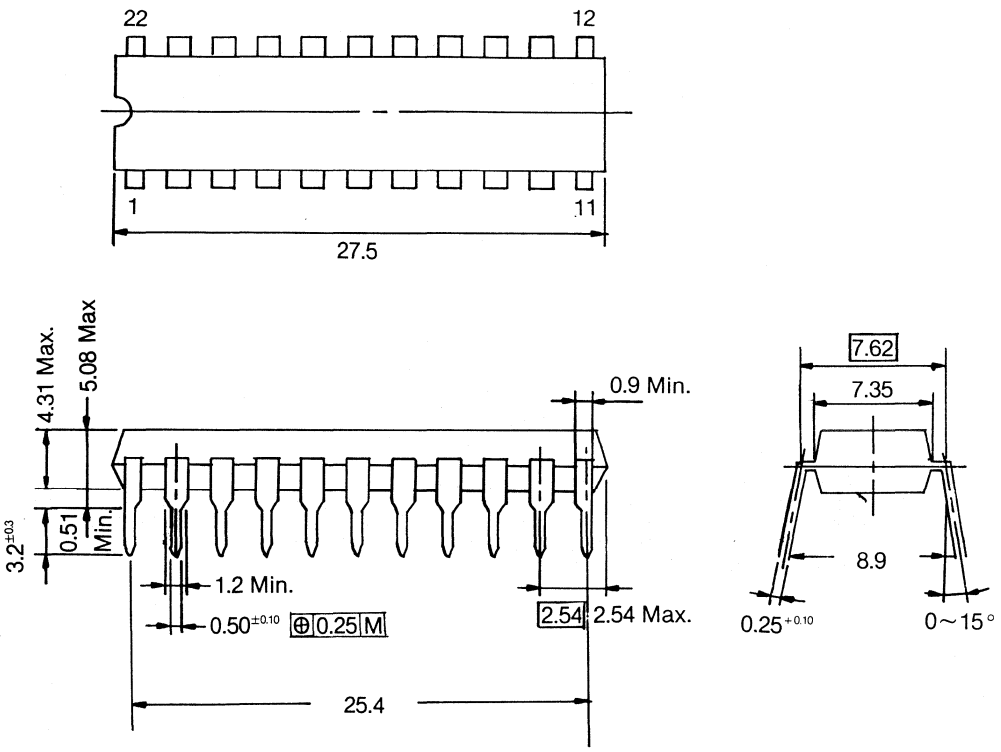


Write Cycle No. 2
($\overline{CS}$ Controlled) (5)



Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH} —200mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimension of 4362C
(22 Pin Plastic DIP)
Units: mm



Note: 1. ⊕ 0.25 M: The cernter of each lead can be shifted within the tolerance of 0.25 mm for both Sides.
2. 2.54 7.62: Figure in [ ] means Typical Figure.

High Speed 65,536 BIT STATIC CMOS RAM *

DESCRIPTION

The μPD4363C is a high speed, low power, 16,384 words by 4 bit static CMOS RAM fabricated with short channel silicon-gate CMOS process. The μPD4363C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD4363C requires no clock or refreshing to operate.
Three kinds of access time, address access time and chip select access time and output enable access time, are very fast. Output enable access time is about half of other access times. And address access time and chip select access time are the same and very fast.
The grades of access time are 45ns, 55ns and 70ns.
The μPD4363C is packaged in a 24-pin plastic Dual In-line Package (DIP) used with the standard JEDEC pin configuration.

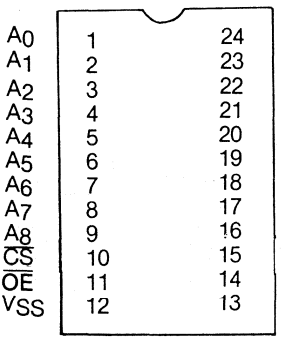
FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or refreshing required
- TTL Compatible — All Inputs and Outputs
- Commom I/O Capabillyti
- $\overline{OE}$ eliminates Need for External Bus Buffers
- Three-State Output
- Fast Access Time

μPD4363C-45	45ns MAX
μPD4363C-55	55ns MAX
μPD4363C-70	70ns MAX

- Low Standby Current 20mA TYP
- Low Active Current 80mA TYP
- Standard 300 mil 24-pin Plastic DIP

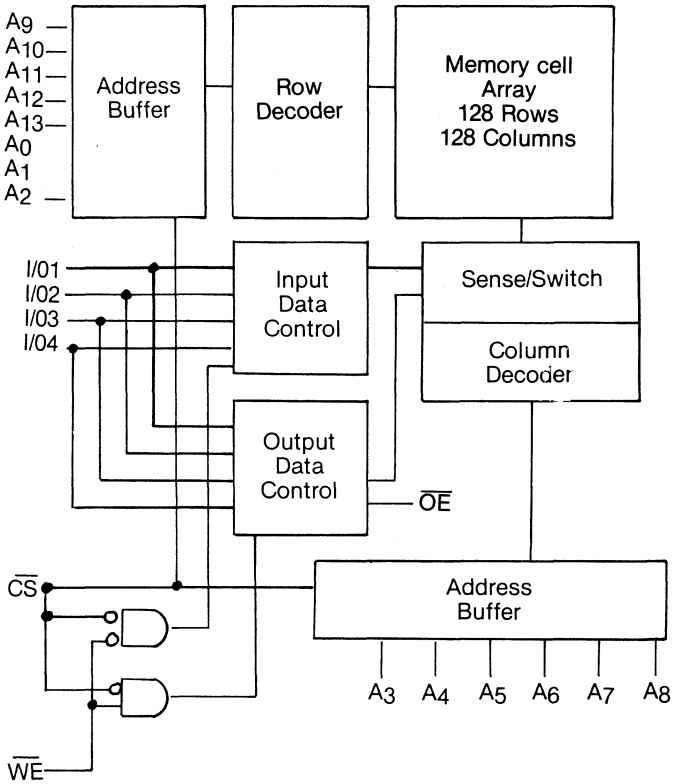
Pin Configuration and Function



A_0-A_{13}	Address Inputs
I/01-I/04	Data-Input/Output
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND

*under development

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	I_{CC}
H	X	X	Not Selected	High Z	Standby
L	H	L	Read	Dout	Active
L	H	H	Read	High Z	Active
L	L	X	Write	DIN	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0V min. while 20ns pulse width.

Recommended DC Operating Conditions (Ta = 0° to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

Note (1) V_{IL} = −3.0V Min. while 20ns pulse width.

Capacitance (TA = 25°C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data-Output Capacitance	C_{DOUT}	V_{DOUT} = 0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0° to 70°C, V_{CC} = 5V±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0~V_{CC},	−2		2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0~V_{CC}, $\overline{CS}$ = V_{IH},	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA			90	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V, V_{IN} < 0.2V or > V_{CC} −0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

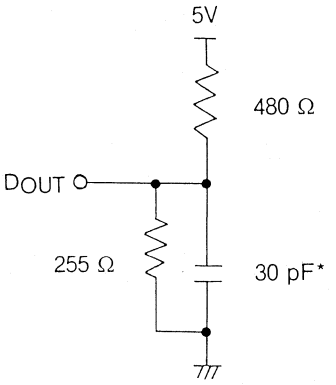


Figure 1 Output Load

*Including Scope and jig

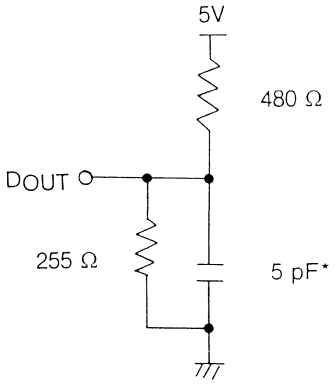


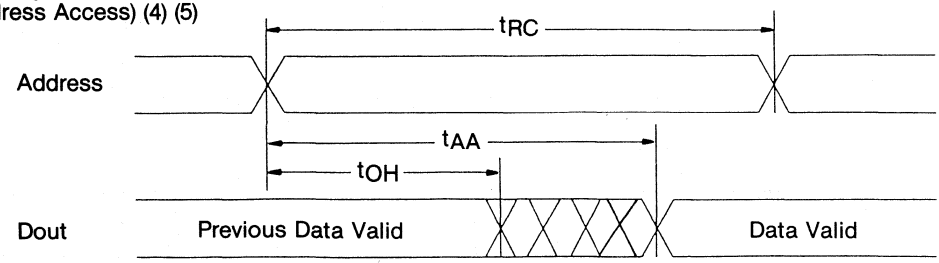
Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

AC Characteristics (Ta = 0° to 70°C, V_{CC} = 5V±10%)
Read Cycle

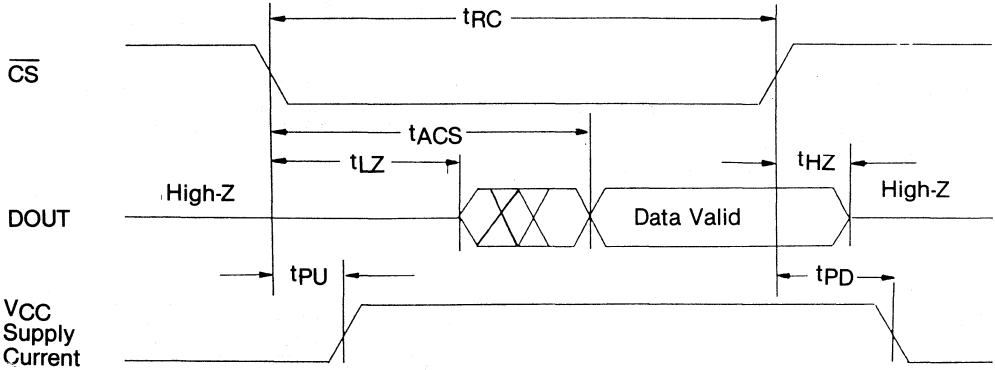
Parameter	Symbol	μPD4363C —45		μPD4363C —55		μPD4363C —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	45		55		70		ns
Address Access Time	t_{AA}		45		55		70	ns
Chip Select Access Time	t_{ACS}		45		55		70	ns
Output hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	20	0	25	0	30	ns
Output Enable to Output Varid	t_{OE}		20		25		30	ns
Output Enable to Output in Low Z	t_{OLZ}	5		5		5		ns
Output Disable to Output in High Z	t_{OHZ}	0	25	0	30	0	35	ns
Chip Selection to Power-up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Downtime	t_{PD}	0	30	0	40	0	40	ns

Read Cycle Waveforms

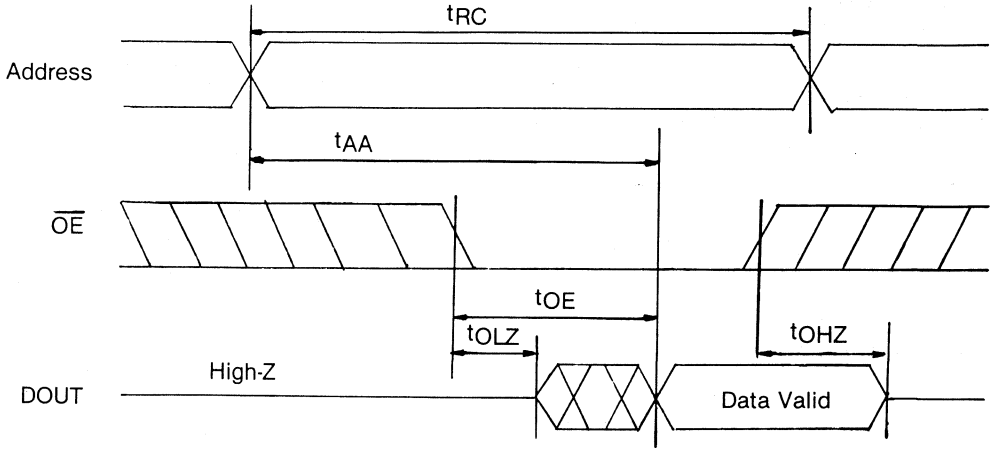
Read Cycle No. 1
(Address Access) (4) (5)



Read Cycle No. 2
(Chip Select Access) (4) (6)



Read Cycle No. 3
($\overline{OE}$ Access)



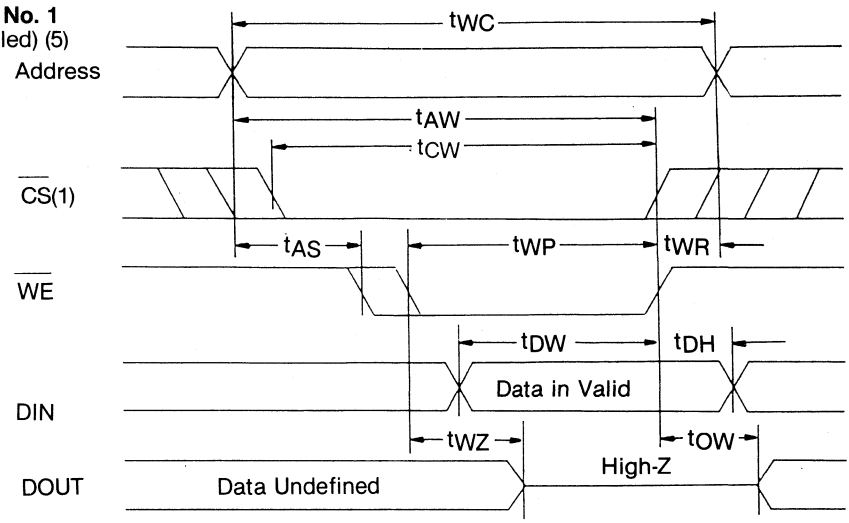
Notes: (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured +200mV from steady state voltage with specified loading in Figure 2.
(3) Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified load in Figure 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continuously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

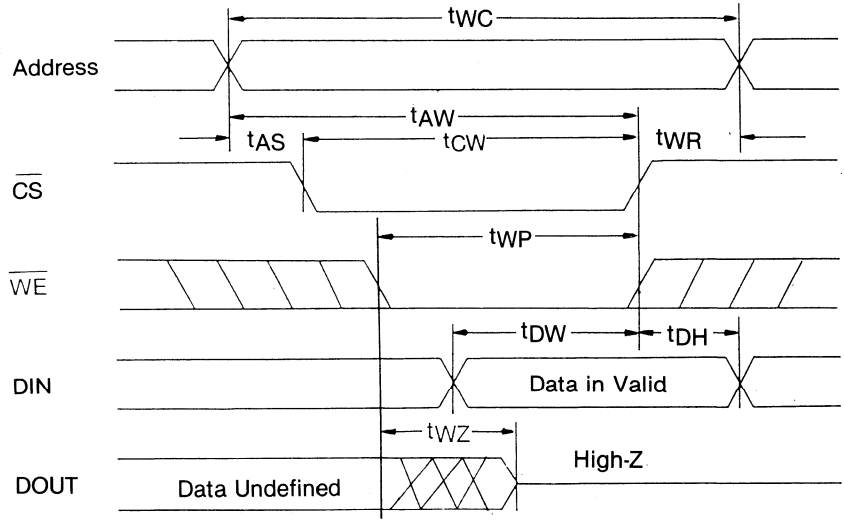
Parameter	Symbol	μPD4363C −45		μ4363C −55		μPD4363C −70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}(2)	45		55		70		ns
Chip Selection to End of Write	t_{CW}	40		50		60		ns
Address Valid to End of Write	t_{AW}	40		50		60		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	40		50		60		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	20		25		30		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enabled to Output in HZ	t_{WZ}(3)	0	20	0	25	0	30	ns
Output Active from End of Write	t_{OW}(4)	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1
($\overline{WE}$ Controlled) (5)



Write Cycle No. 2
(CS Controlled) (5)



Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH} −200mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

65.536 Bit Static CMOS RAM

DESCRIPTION

The μPD4364C/G is a high speed, low power, 8192 words by 8 bits static CMOS RAM fabricated with a silicon-gate CMOS technology. The μPD4364C/G is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD4364C/G a very low operating power device which requires no clock or refreshing to operate.
Two chip enable inputs are provided for battery back-up application, and one output enable input for easy interface.
Data retention is quaranteed at a power supply voltage as low as 2 volts. (μPD4364C/G-12L/15L/20L)
The μPD4364C is packaged in a standard 28-pin dual-in-line plastic package and plug-in compatible with 2764 type EPROMs.
The μPD4364G is packaged in a mini flat package providing high density application.

FEATURES

- Single + 5V Supply
- Fully Static Operation - no Clock or Refreshing required
- TTL compatible - all inputs and outputs
- Common I/O using Three-State output
- Output enable and two chip enable inputs for easy application
- Fast Access Time

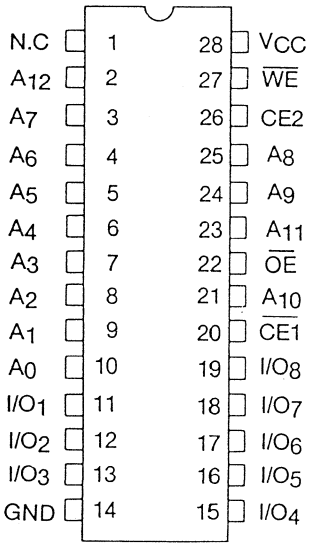
μPD4364C/G-10L	100ns max
μPD4364C/G-12L	120ns max
μPD4364C/G-15L	150ns max
μPD4364C/G-20L	200ns max

- Low power dissipation

Active	μPD4364C/G-10L	45mA max
	μPD4364C/G-12L	40mA max
	μPD4364C/G-15L	35mA max
	μPD4364C/G-20L	30mA max
Standby	μPD4364C/G-15L/20L/-12L/-10L	100 μA max.

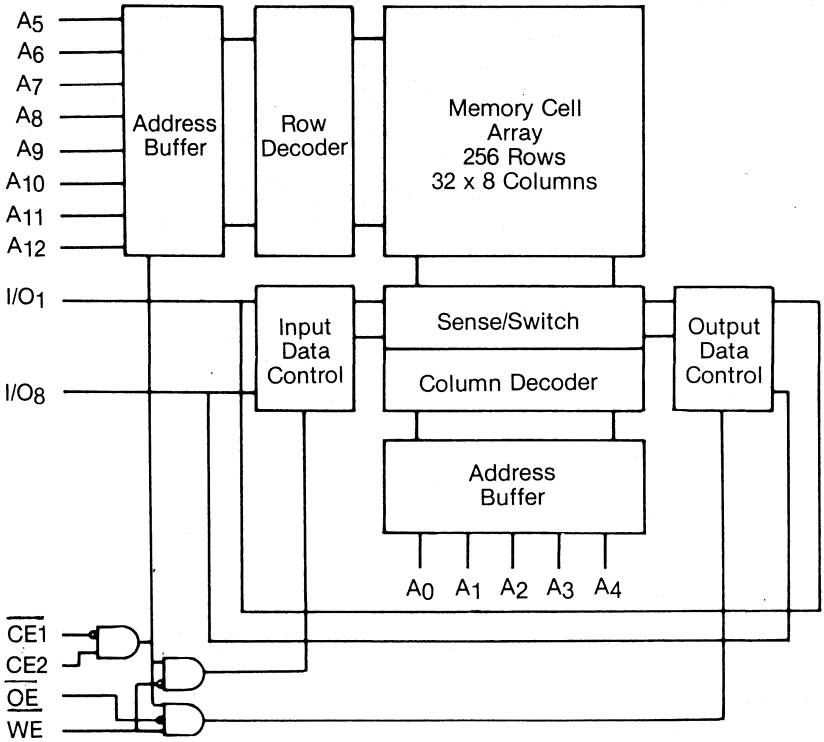
- Data Retention voltage -2 V min.
- Standard 28-pin plastic package (μPD4364C)
- Plug-in compatible with 2764 type EPROMs (μPD4364C)
- 28 pin miniflat package (μPD4364G)

PIN CONFIGURATION AND FUNCTION



A0 - A12	Addres Input
I/O0 - I/O8	Data Input/Output
$\overline{CE1}$	Chip Enable Active Low
CE2	Chip enable Active High
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VCC	Power (+ 5V)
GND	Ground
N.C.	No Connection

Block Diagram



Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	ICC
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	Dout disable	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Item	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to 7.0	V
V_{IN}	Input Voltage	−0.5 to V_{CC} + 0.5 −3.0V min. (Pulse width 50 ns)	V
V_{OUT}	Output Voltage	− 0.5 to V_{CC} +0.5 −3.0V min. (pulse width 50 ns)	V
Topr	Operating Temperature	0 to 70	°C
Tstg	Storage Temperature	−55 to + 125	°C
Pd	Power Dissipation	1.0	W

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IL}	Input Low Voltage	−0.3*		0.8	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.5	V

*−3.0V min. (Pulse width = 50ns)

DC Characteristics ($T_a = 0$ to 70°C, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{CC}$	-1		1	μA
I_{LO}	I/O Leakage Current	$V_{I/O} = 0 \sim V_{CC}$, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1		1	μA
I_{CCA1}	Operating Supply Current	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, Min. Cycle $I_{I/O} = 0$		1)	1)	mA
I_{CCA2}	Operating Supply Current	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$ $I_{I/O} = 0$ DC Current		5	10	mA
I_{CCA3}	Operating Supply Current	$V_{\overline{CE1}} \leqq 0.2V$, $V_{CE2} \geqq V_{CC} - 0.2V$ $V_{IH} \geqq V_{CC} - 0.2V$, $V_{IL} \leqq 0.2V$, Cycle=1MHz, $I_{I/O}=0$		3	5	mA
I_{SB}	Standby Supply Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$			2)	mA
I_{SB1}	Standby Supply Current	$\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$		3)	3)	μA
I_{SB2}	Standby Supply Current	$CE2 \leqq 0.2V$		3)	3)	μA
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1.0$ mA	2.4			V

Notes: (1) μPD4364C/G-10L 45mA max.
μPD4364C/G-12L 20mA Typ, 40mA max.
μPD4364C/G-15L 16mA Typ, 40mA max.
μPD4364C/G-20L 12mA Typ, 35mA max.
(2) μPD4364C/G-10L/12L/15L/20L 3mA max.
(3) μPD4364C/G-12L/15L/20L 2μA typ 100μA max.

Capacitance ($t_a = 25$°C, $f = 1$ MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0V$	8	pF

AC Test Conditions

Input Pulse Levels	0.8 to 2,2V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	1TTL Gate and CL = 100pF

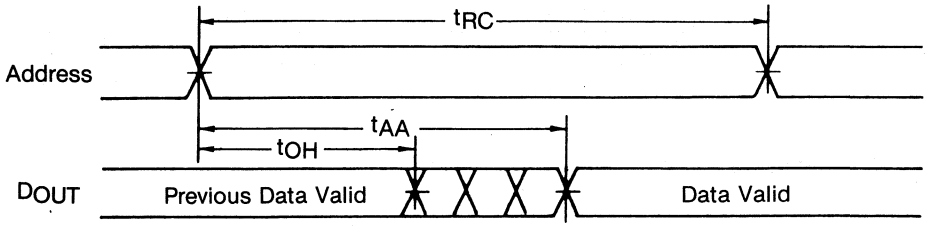
AC Characteristics ($T_a = 0$ to 70°C, $V_{CC} = 5V \pm 10\%$)

Read Cycle

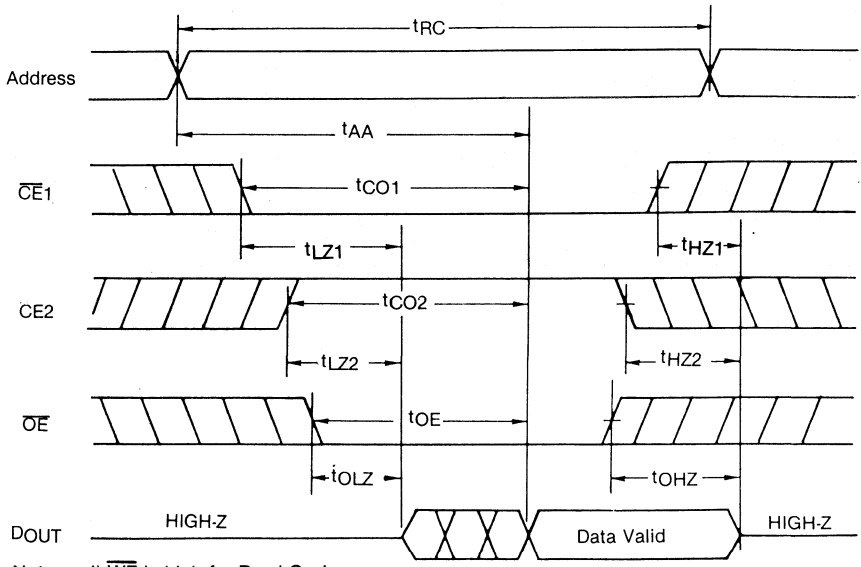
Parameter	Symbol	μPD4364C -10L		μPD4364C/G —12L		μPD4364C/G —15L		μPD4364C/G —20L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		200		ns
Address Access Time	t_{AA}		100		120		150		200	ns
$\overline{CE}$1 Access Time	t_{CO1}		100		120		150		200	ns
CE2 Access Time	t_{CO2}		100		120				200	ns
Output enable to Ouput Valid	t_{OE}		50		60		70		100	ns
Output hold fromAddress Change	t_{OH}	10		10		10		15		ns
Chip enable ($\overline{CE}$1) to Output	t_{LZ1}	10		10		10		15		ns
Chip enable (CE2) to Output in Low-Z	t_{LZ2}	10		10		10		15		ns
Output enable to Output in Low-Z	t_{OLZ}	5		5		5		5		ns
Chip enable ($\overline{CE}$1) to Output in High-Z	t_{HZ1}		35		40		50		100	ns
Chip enable (CE2) to Output in High-Z	t_{HZ2}		35		40		50		100	ns
Output enable to Output in High-Z	t_{OHZ}		35		40		50		80	ns

Timing Waveforms

Read Cycle No. 1
(Address access) (1) (2)



Read Cycle No. 2
(Chip enable Access) (1,3)

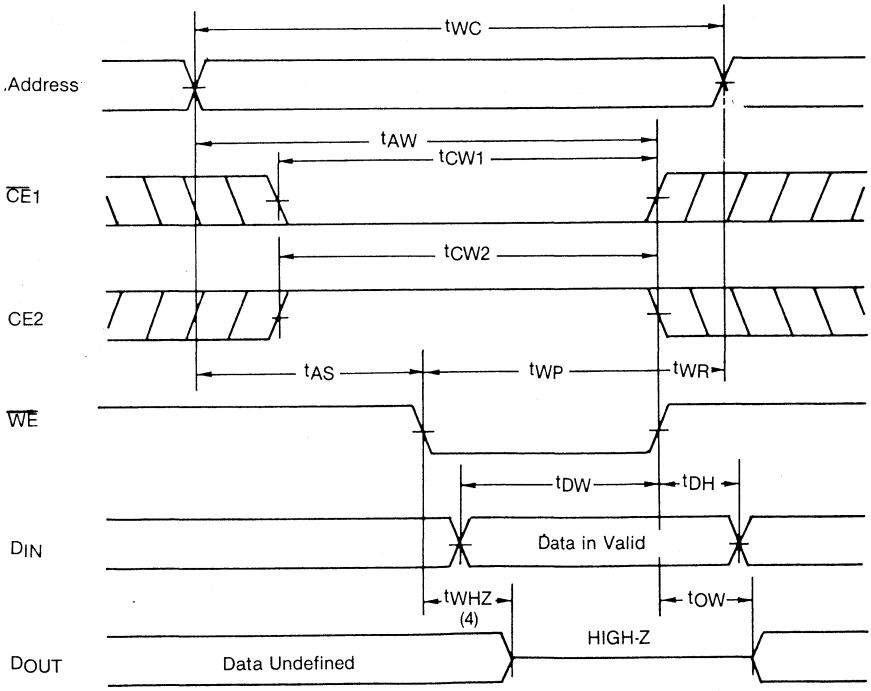


Notes: 1) $\overline{WE}$ is high for Read Cycles
2) Device is continuously selected, $\overline{CE1} = \overline{OE} = V_{IL}$, CE2 = V_{IH}.
3) Addresses valid prior to or coincident with $\overline{CE1}$ transition low, CE2 transition high.

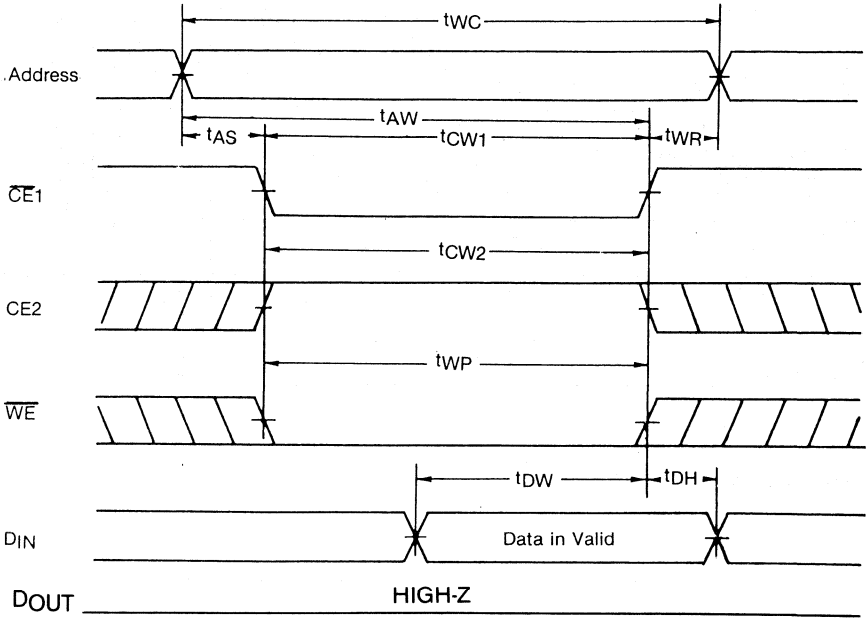
Write Cycle

Parameter	Symbol	μPD4364C/G -10L		μPD4364C/G -12L		μPD4364C/G -15L		μPD4364C/G -20L		
		Min	Max.	Min.	Max.	Min.	Max.	Unit		
Write Cycle Time	t_{WC}	100		120		150		200		ns
Chip enable ($\overline{CE}$1) to End of Write	t_{CW1}	80		85		100		180		ns
Chip enable (CE2) to End of Write	t_{CW2}	80		85		100		180		ns
Address valid to End of Write	t_{AW}	80		85		100		180		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		140		ns
Write Recovery Time	t_{WR}	5		5		5		5		ns
Data valid to End of Write	t_{DW}	40		50		60		80		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write enable to Output in High-Z	t_{WHZ}		35		40		50		100	ns
Output active from End of Write	t_{OW}	5		5		10		10		ns

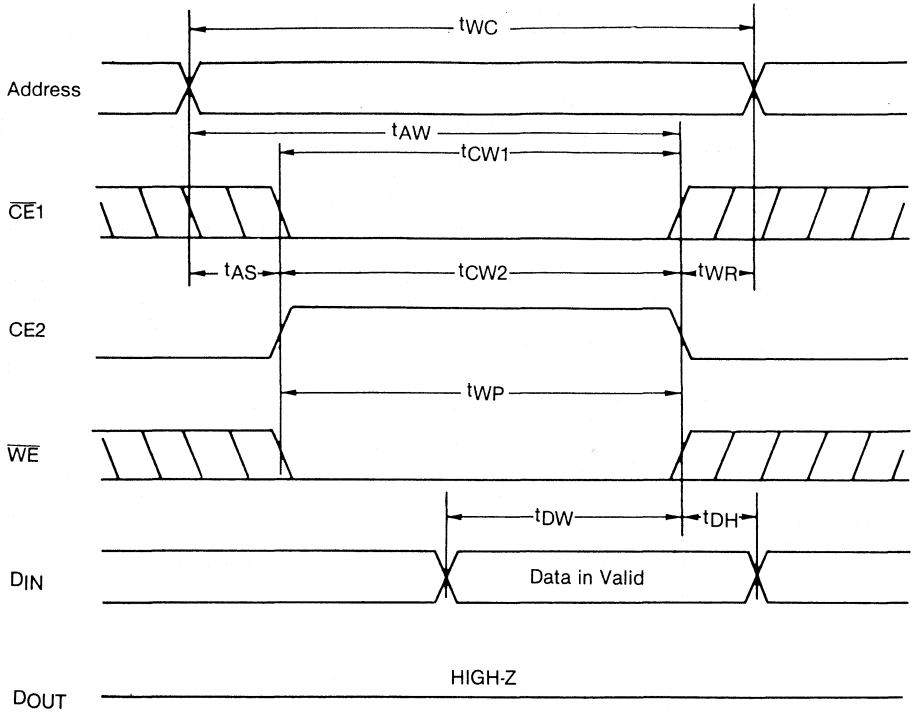
Write Cycle No. 1 ($\overline{WE}$ Controlled) (1, 2, 3)



Write Cycle No. 2 ($\overline{CE}$1 Controlled) (1, 2)



Write Cycle No. 3 (CE2 Controlled) (1, 2)



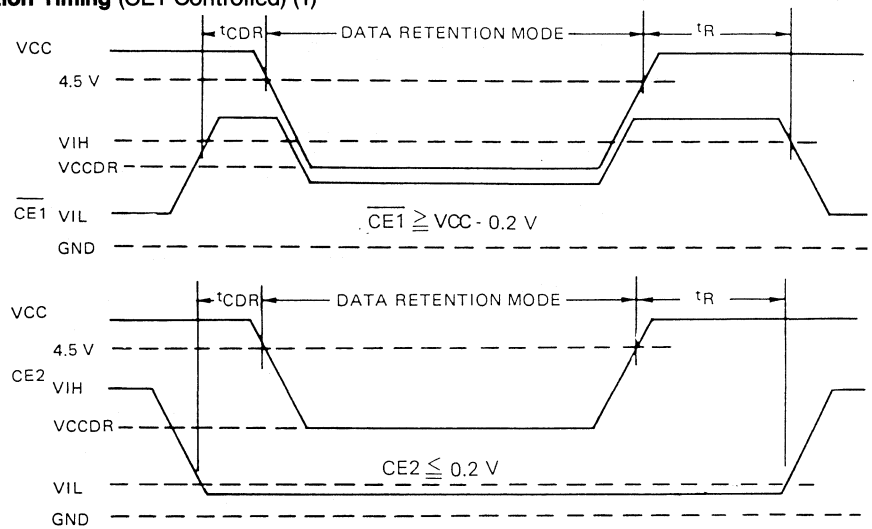
Notes: 1) A write occurs during the overlap of a low $\overline{CE1}$ and a high CE2 and a low $\overline{WE}$.
2) $\overline{CE1}$ or $\overline{WE}$ (or CE2) must be high (low) during address transition.
3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

Low V_{CC} Retention Characteristics (T_a = 0 to 70 °C)

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{CCDR1}	Data Retention Supply Voltage	$\overline{CE1} \geq V_{CC} - 0.2V$ $CE2 \geq V_{CC} - 0.2V$	2.0		5.5	V
V_{CCDR2}	Data Retention Supply Voltage	$CE2 \leq 0.2V$	2.0		5.5	V
I_{CCDR1}	Data Retention Supply Current	$V_{CC} = 3.0V$, $\overline{CE1} \geq V_{CC} - 0.2V$ $CE2 \geq V_{CC} - 0.2V$		1	1) 50	μA
I_{CCDR2}	Data Retention Supply Current	$V_{CC} = 3.0V$, $CE2 \leq 0.2V$		1	1) 50	μA
t_{CDR}	Chip Deselect to Data Retention Time		0			ns
t_R	Operating Recovery Time		t_{RC}			ns

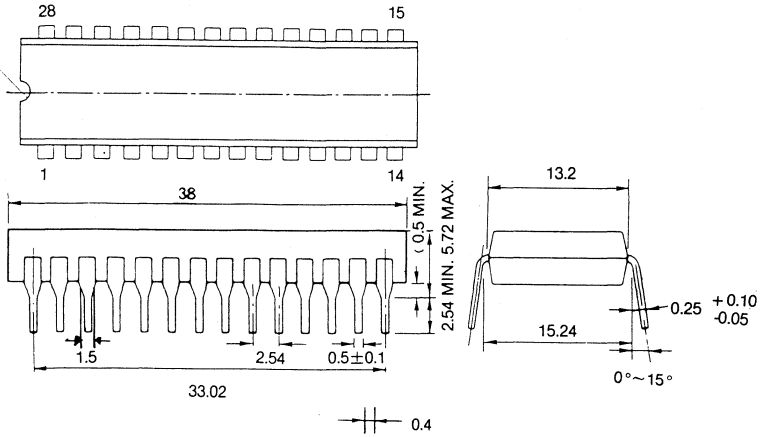
1) 15 μA Max. with T_a = 0 to 40 °C.

Data Retention Timing ($\overline{CE1}$ Controlled) (1)

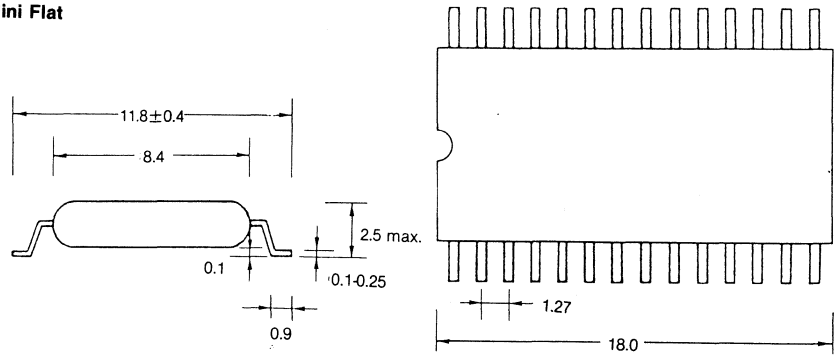


Notes: 1) CE2 must be equal to or higher than V_{CC}-0.2 V. The other inputs (Addresses, $\overline{WE}$, $\overline{OE}$, I/Os) can be in a high impedance.
2) The inputs (Addresses, $\overline{CE1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

Package Outline
(Unit: mm)
μPD4364C Plastic



μPD4364G Mini Flat



Very Low Power Version 65,536 Bit Static CMOS RAM

Description

The μPD4364C/G is a high speed, low power, 8192 words by 8 bits static CMOS RAM fabricated with advanced silicon-gate CMOS technology. The μPD4364C/G is a low standby power device using n-channel memory cell with polysilicon resistors. Furthemore, a novel circuitry technique makes the μPD4364C/G a very low operating power device which requires no clock or refreshing to operate.
Two chip enable inputs are provided for battery back-up application, and one output enable input for easy interface.
Data retention is guaranteed at a power supply voltage as low as 2 volts.
The μPD4364C is packaged in a standard 28-pin dual-in-line Plastic package and plug-in compatible with 2764 type EPROMs.
The μPD4364G is packaged in a mini flat package providing high density application.

Features

- Single + 5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All inputs and Outputs
- Common I/O Using Three-State Output
- Two Chip Enable and One Output Enable Inputs for Easy Application
- Fast Access Time

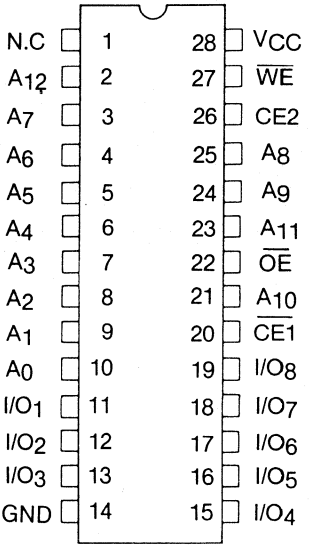
μPD4364C/G-10LL	100 ns MAX
μPD4364C/G-12LL	120 ns MAX
μPD4364C/G-15LL	150 ns MAX
μPD4364C/G-20LL	200 ns MAX

- Low Power Dissipation

Active	μPD4363C/G-10LL	45 mA MAX
	μPD4364C/G-12LL	40 mA MAX
	μPD4364C/G-15LL	40 mA MAX
	μPD4364C/G-20LL	35 mA MAX
Standby	μPD4364C/G-12LL/15LL/20LL	50 μA MAX

- Data Retention Voltage - 2V min (μPD4364C/G-10LL/12LL/15LL/20LL)
- Standard 28-pin Plastic Package (μPD4364C)
- Plug-in Compatible with 2764 type EPROMs (μPD4364C)
- 28-pin Mini Flat Package (μPD4364G)

Pin Configuration and Function

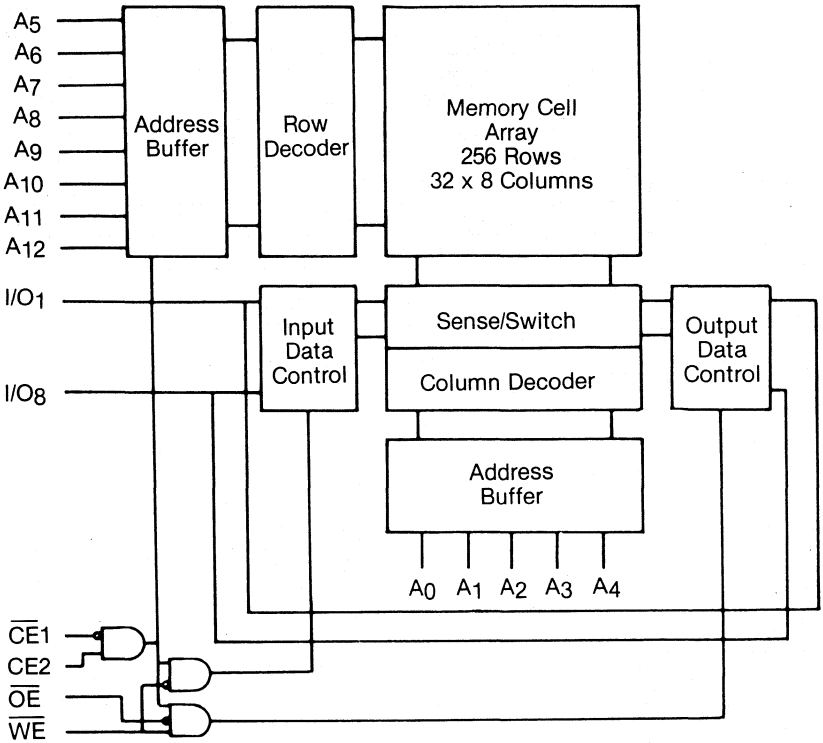


A_0 - A_{12}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CE}1$	Chip Enable Active Low
CE2	Chip Enable Active High
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
GND	Ground
N.C	No Connection

Truth Table

$\overline{CE}1$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	ICC
H	X	X	X	Not selected	HZ	Standby
X	L	X	X	Not selected	HZ	Standby
L	H	H	H	Dout disable	HZ	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5* to 7.0	V
Input Voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Output Voltage	V_{OUT}	−0.5* to V_{CC} + 0.5	V
Operating Temperature	Topr	0 to 70	°C
Storag Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

*—3.0V min. (Pulse Width 50ns)

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3*		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.5$	V

*−3.0V min. (Pulse Width 50ns)

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN}=0\sim V_{CC}$	-1		1	μA
I/O Leakage Current	I_{LO}	$V_{I/O}=0\sim V_{CC}$ $\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	-1		1	μA
Operating Supply Current	I_{CCA1}	$\overline{CE1}=V_{IL}$, $CE2=V_{IH}$ Min. Cycle $I_{I/O}=0$			(1)	mA
Operating Supply Current	I_{CCA2}	$\overline{CE1}=V_{IL}$, $CE2=V_{IH}$ $I_{I/O}=0$ DC Current		5	10	mA
Operating Supply Current	I_{CCA3}	$V_{CE1}\leqq 0.2V$, $V_{CE2}\geqq V_{CC}-0.2V$ V $V_{IH}\geqq V_{CC}-0.2V$, $V_{IL}\leqq 0.2V$ Cycle = 1MHz, $I_{I/O}=0$		3	5	mA
Standby Supply Current	I_{SB}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$			3	mA
Standby Supply Current	I_{SB1}	$\overline{CE1}\geqq V_{CC}-0.2V$ $CE2\geqq V_{CC}-0.2V$		2	50*	μA
Standby Supply Current	I_{SB2}	$CE2\leqq 0.2V$		2	50*	μA
Output Low Voltage	V_{OL}	$I_{OL}=2.1mA$			0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4			V

*15μ Max. (Ta = 0 to 40°C)

Notes (1) μPD4364C/G-10LL 20 mA Typ 45 mA Max.
μPD4364C/G-12LL 20 mA Typ 40 mA Max.
μPD4364C/G-15LL 18 mA Typ 40 mA Max.
μPD4364C/G-20LL 14 mA Typ 35 mA Max.

Capacitance (Ta = 25°C f = 1MHz)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN}=0V$	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	8	pF

AC Test Condition

Input Pulse Levels	0.8 to 2.2V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	1TTL Gate and CL = 100pF

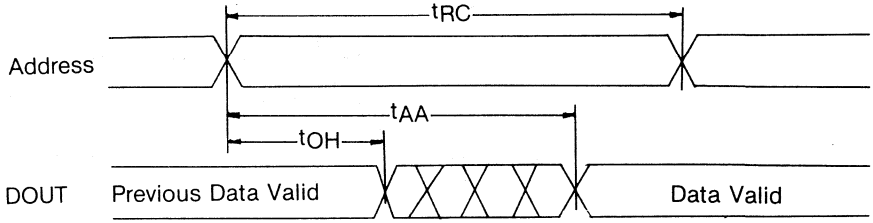
AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ± 10%)

Read Cycle

Parameter	Symbol	μPD4364C/G -10LL		μPD4364C/G -12LL		μPD4364C/G -15LL		μPD4364C/G -20LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		200		ns
Address Access Time	t_{AA}		100		120		150		200	ns
$\overline{CE}$1 Access Time	t_{CO1}		100		120		150		200	ns
CE2 Access Time	t_{CO2}		100		120				200	ns
Output enable to Ouput Valid	t_{OE}		50		60		70		100	ns
Output hold fromAddress Change	t_{OH}	10		10		10		15		ns
Chip enable ($\overline{CE}$1) to Output	t_{LZ1}	10		10		10		15		ns
Chip enable (CE2) to Output in Low-Z	t_{LZ2}	10		10		10		15		ns
Output enable to Output in Low-Z	t_{OLZ}	5		5		5		5		ns
Chip enable ($\overline{CE}$1) to Output in High-Z	t_{HZ1}		35		40		50		100	ns
Chip enable (CE2) to Output in High-Z	t_{HZ2}		35		40		50		100	ns
Output enable to Output in High-Z	t_{OHZ}		35		40		50		80	ns

Read Cycle Timing Chart

Read Cycle No. 1 (Address access) (1) (2)

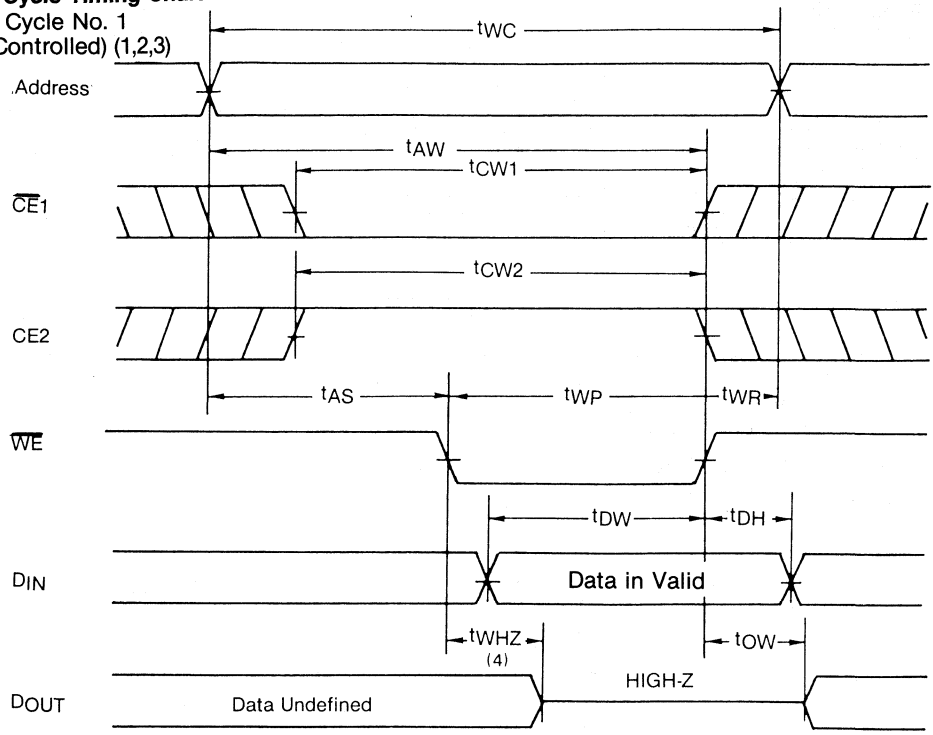


Write Cycle

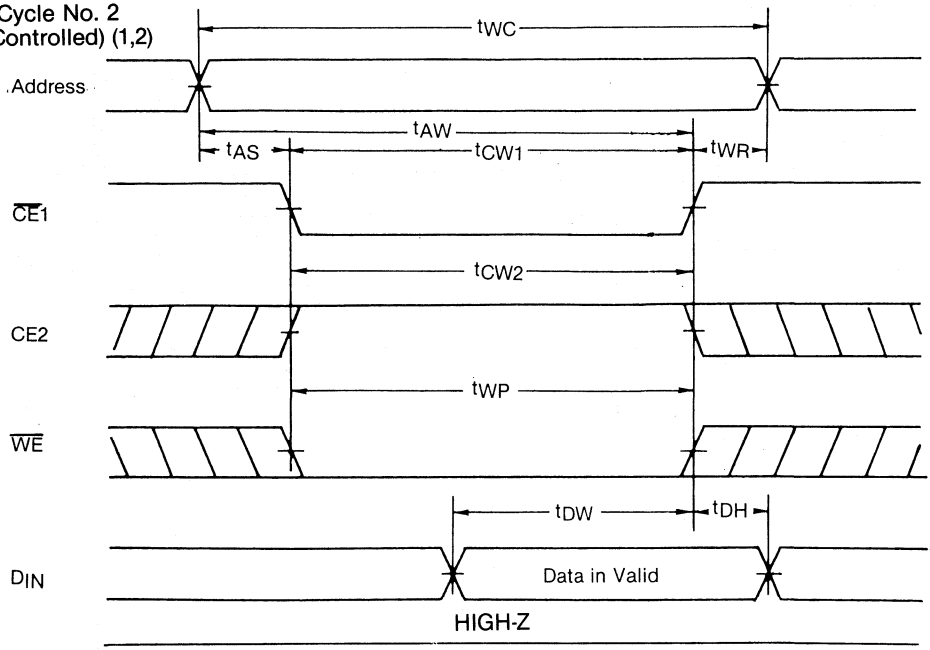
Parameter	Symbol	μPD4364C/G -10LL		μPD4364C/G -12LL		μPD4364C/G -15LL		μPD4364C/G -20LL		
		Min	Max.	Min.	Max.	Min.	Max.	Unit		
Write Cycle Time	t_{WC}	100		120		150		200		ns
Chip enable ($\overline{CE}$1) to End of Write	t_{CW1}	80		85		100		180		ns
Chip enable (CE2) to End of Write	t_{CW2}	80		85		100		180		ns
Address valid to End of Write	t_{AW}	80		85		100		180		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		140		ns
Write Recovery Time	t_{WR}	5		5		5		5		ns
Data valid to End of Write	t_{DW}	40		50		60		80		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write enable to Output in High-Z	t_{WHZ}		35		40		50		100	ns
Output active from End of Write	t_{OW}	5		5		10		10		ns

Write Cycle Timing Chart

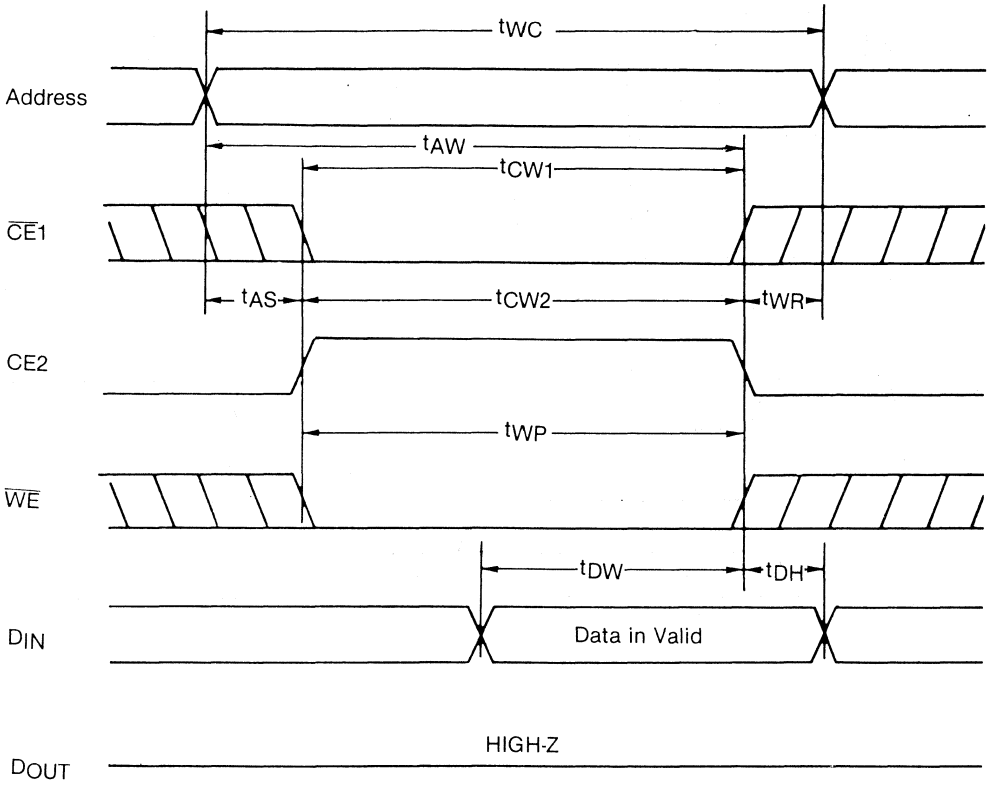
Write Cycle No. 1
($\overline{WE}$ Controlled) (1,2,3)



Write Cycle No. 2
($\overline{CE1}$ Controlled) (1,2)



Write Cycle No. 3
(CE2 Controlled) (1,2)



Notes: 1) A write occurs during the overlap of a low $\overline{CE}1$ and a high CE2 and a low $\overline{WE}$.
2) $\overline{CE}1$ or $\overline{WE}$ (or CE2) must be high (low) during address transition.
3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

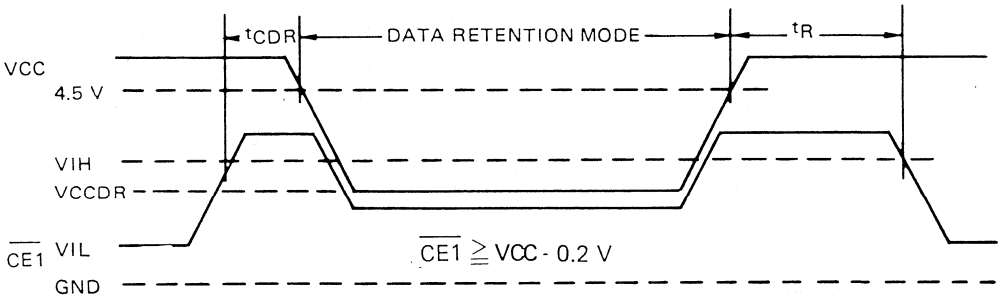
Low V_{CC} Data Retention Characteristics (T_a = 0 to 70 °C) for μPD4364C/G-10LL/12LL/15LL/20LL

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Data Retention Supply Voltage	V_{CCDR1}	$\overline{CE1} \geqq V_{CC}$ −0.2V or $CE_2 \leqq 0.2V$ $CE2 \geqq V_{CC}$ −0.2V or $CE_2 \leqq 0.2V$	2.0		5.5	V
Data Retention Supply Voltage	V_{CCDR2}	CE2 = 0.2V	2.0		5.5	V
Data Retention Supply Current	I_{CCDR1}	V_{CC} = 3.0V CE1 = V_{CC} −0.2V CE2 = V_{CC} −0.2V		1	20*	μA
Data Retention Supply Current	I_{CCDR2}	V_{CC} = 3.0V CE2 = 0.2V		1	20*	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

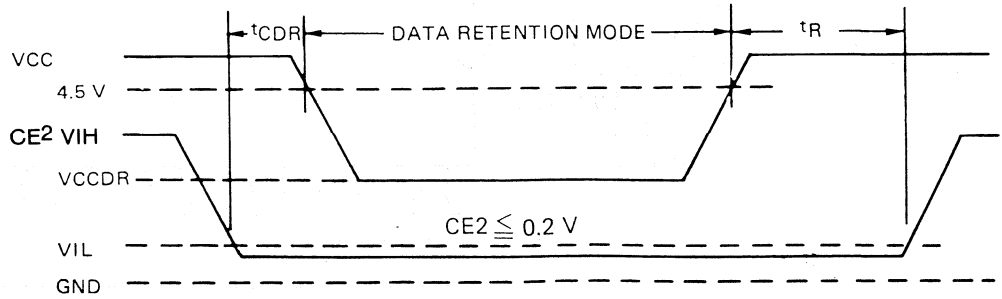
*5μA Max. (T_a = 0 to 40 °C)

Data Retention Timing Chart

($\overline{CE1}$ Controlled) (1)

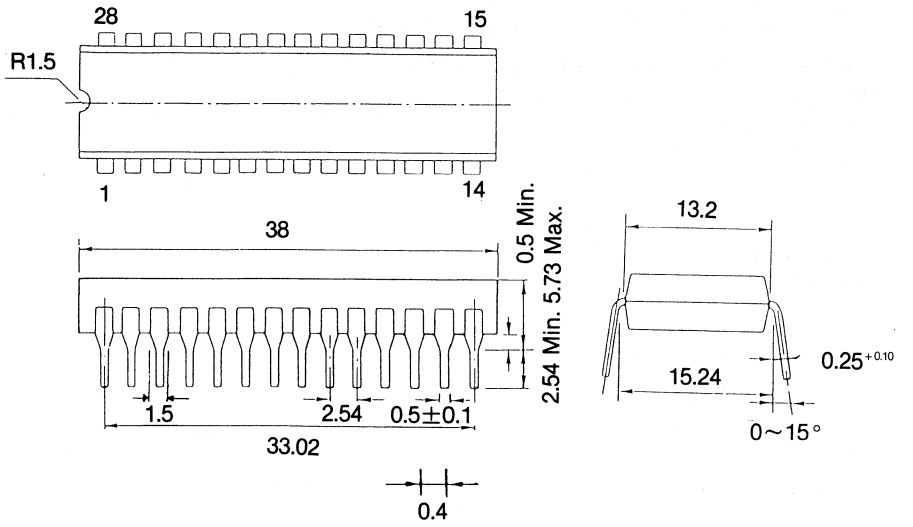


CE_2 Controlled (2)

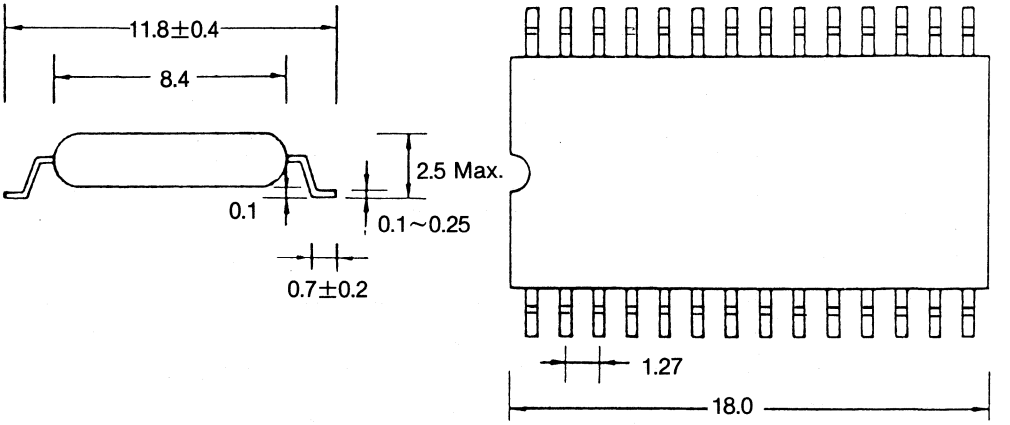


Notes: 1) CE2 must be equal to or higher than V_{CC}-0.2V or $CE_2 \leqq 0.2V$. The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.
2) The inputs (Addresses, $\overline{CE1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

Package Outline
(Unit: mm)
μPD4364C Plastik



μPD4364G Mini Flat



65 536 BIT STATIC CMOS RAM

Description

The μPD4364CX is a high speed, low power, 8192 words by 8 bits static CMOS RAM fabricated with advanced silicon-gate CMOS technology. The μPD4364CX is a low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD4364CX a very low operating power device which requires no clock or refreshing to operate.
Two chip enable inputs are provided for battery back-up application, and one output enable input for easy interface.
Data retention is guaranteed at a power supply voltage as low as 2 volts (μPD4364CX-10L/12L/15L).
The μPD4364CX is packaged in 300 mil slim dual-in-line plastic package providing high density application.

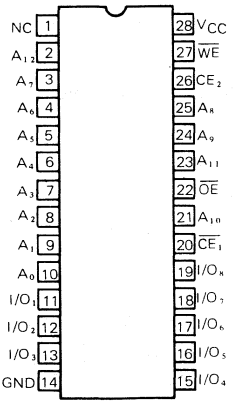
Features

- Single +5 V supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Input and Output
- Common I/O Using Three-State Output
- Fast Access Time

	μPD4364CX-10/-10L	100 ns MAX.
	μPD4364CX-12/-12L	120 ns MAX.
	μPD4364CX-15/-15L	150 ns MAX.
Low Power Dissipation		
Active	μPD4364CX-10/-10L	45 mA MAX.
	μPD4364CX-12/-12L	40 mA MAX.
	μPD4364CX-15/-15L	35 mA MAX.
Standby	μPD4364CX-10/-12/-15	2 mA MAX.
	μPD4364CX-10L/-12L/-15L	100 μA MAX.

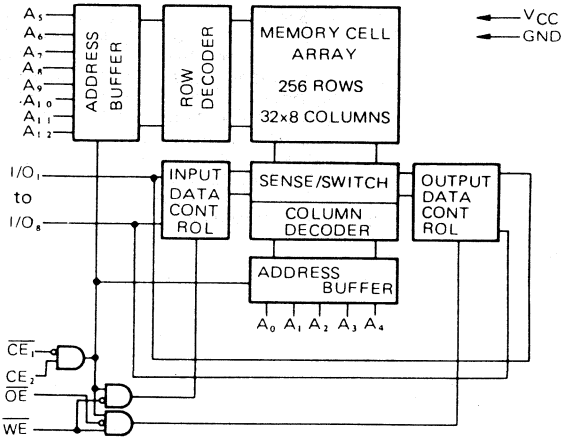
- 28 pin 300 mil slim plastic DIP

Pin Configuration



A_0 to A_{12}	:	ADDRESS INPUT
I/O_1 to I/O_8	:	DATA INPUT/OUTPUT
$\overline{CE_1}$, CE_2	:	CHIP ENABLE
$\overline{WE}$	:	WRITE ENABLE
$\overline{OE}$	:	OUTPUT ENABLE
V_{CC}	:	POWER (+5 V)
GND	:	GND
NC	:	NO CONNECTION

BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	X	NOT SELECTED	Hz	STANDBY
X	L	X	X			
L	H	H	H	D_{OUT} DISABLE		ACTIVE
L	H	L	H	READ	D_{OUT}	
L	H	X	L	WRITE	D_{IN}	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5* to 7.0	V
Input, Output Voltage	V_T	−0.5* to V_{CC}+0.5	V
Operating Temperature	T_{opt}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

* −3.0 V min. (Pulse Width 50 ns)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.3*		0.8	V
Ambient Temperature	T_a	0		70	°C

* −3.0 V min. (Pulse Width 50 ns)

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD4364CX-10/-12/-15			μPD4364CX-10L/-12L/-15L			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Input Leakage Current	I_{LI}	−1.0		1.0	−1.0		1.0	μA	V_{IN}=0 to V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	−1.0		1.0	μA	$V_{\overline{CE1}}=V_{IH}$ or $V_{CE2}=V_{IL}$ or $V_{\overline{OE}}=V_{IH}$ or $V_{\overline{WE}}=V_{IL}$, $V_{I/O}$=0 to V_{CC}
Operating Supply Current	I_{CCA1}			①			①	mA	$V_{\overline{CE1}}=V_{IL}$, $V_{CE2}=V_{IH}$ MIN cycle, $I_{I/O}$=0
	I_{CCA2}		5	10		5	10	mA	$V_{\overline{CE1}}=V_{IL}$, $V_{CE2}=V_{IH}$, $I_{I/O}$=0
	I_{CCA3}		3	5		3	5	mA	$V_{\overline{CE1}}\leqq 0.2$ V, $V_{CE2}\geqq V_{CC}-0.2$ V $V_{IH}\geqq V_{CC}-0.2$ V, $V_{IL}\leqq 0.2$ V Cycle = 1 MHz, $I_{I/O}$=0
Standby Supply Current	I_{SB}			5			3	mA	$V_{\overline{CE1}}=V_{IH}$ or $V_{CE2}=V_{IL}$
	I_{SB1}			2			0.1	mA	$V_{\overline{CE1}}\geqq V_{CC}-0.2$ V, $V_{CE2}\geqq V_{CC}-0.2$ V
	I_{SB2}			2			0.1	mA	$V_{CE2}\leqq 0.2$ V
Output High Voltage	V_{OH}	2.4			2.4			V	I_{OH}=−1.0 mA
Output Low Voltage	V_{OL}			0.4			0.4	V	I_{OL}=2.1 mA

① μPD4364CX-10/-10L ..... 45 mA MAX.
μPD4364CX-12/-12L ..... 40 mA MAX.
μPD4364CX-15/-15L ..... 35 mA MAX.

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

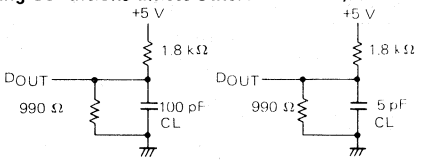
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0 V

Note This parameter is periodically sampled and not 100 % tested.

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

AC TEST CONDITIONS

Input Pulse Levels	0.8 to 2.2 V
Input Pulse Rise and Fall Time	5 ns
Timing Reference Levels	1.5 V
Output Load	Fig. 1, 2



* CL including scope and jig.

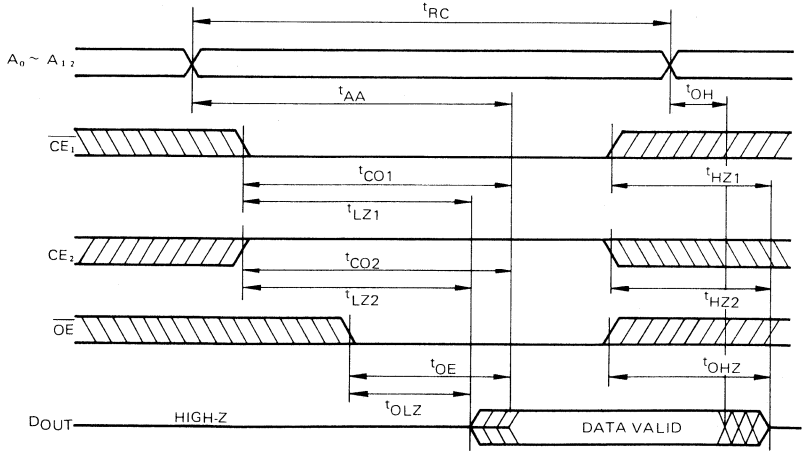
Fig. 1

Fig. 2 (For t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{WHZ}, t_{OW})

READ CYCLE

PARAMETER	SYMBOL	μPD4364CX-10/-10L		μPD4364CX-12/-12L		μPD4364CX-15/-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
$\overline{CE}_1$ Access Time	t_{CO1}		100		120		150	ns
CE_2 Access Time	t_{CO2}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		50		60		70	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Enable ($\overline{CE}_1$) to Output in LZ	t_{LZ1}	10		10		10		ns
Chip Enable (CE_2) to Output in LZ	t_{LZ2}	10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	5		5		5		ns
Chip Disable ($\overline{CE}_1$) to Output in HZ	t_{HZ1}		35		40		50	ns
Chip Disable (CE_2) to Output in HZ	t_{HZ2}		35		40		50	ns
Output Disable to Output in HZ	t_{OHZ}		35		40		50	ns

READ CYCLE TIMING CHART [1], [2], [3]



Notes [1] $\overline{WE}$ is high for read cycle.

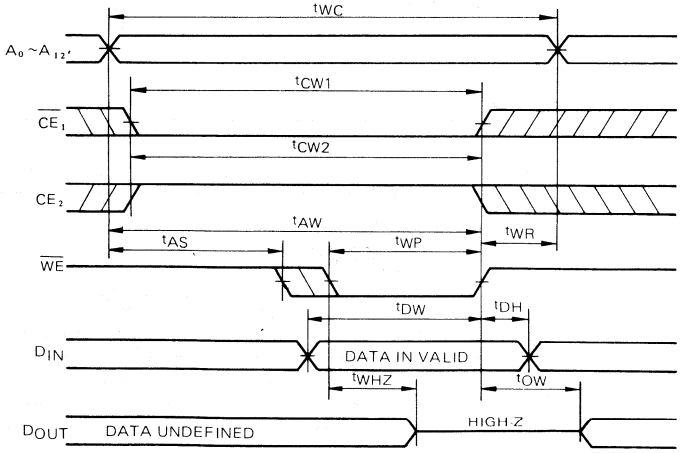
[2] Device is continuously selected, $\overline{CE}_1$=$\overline{OE}$=V_{IL}, CE_2=V_{IH}.

[3] Address valid prior to or coincident with $\overline{CE}_1$ transition low, CE_2 transition high.

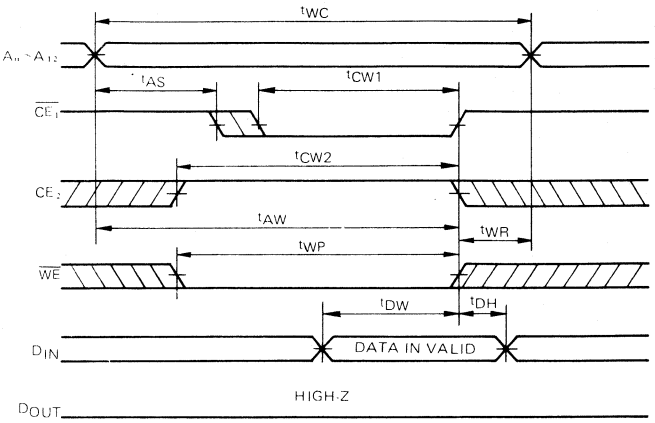
WRITE CYCLE

PARAMETER	SYMBOL	μPD4364CX-10/-10L		μPD4364CX-12/-12L		μPD4364CX-15/-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	100		120		150		ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	80		85		100		ns
Chip Enable (CE_2) to End of Write	t_{CW2}	80		85		100		ns
Address Valid to End of Write	t_{AW}	80		85		100		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Write Recovery Time	t_{WR}	5		5		5		ns
Data Valid to End of Write	t_{DW}	40		50		60		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		35		40		50	ns
Output Active from End of Write	t_{OW}	10		10		10		ns

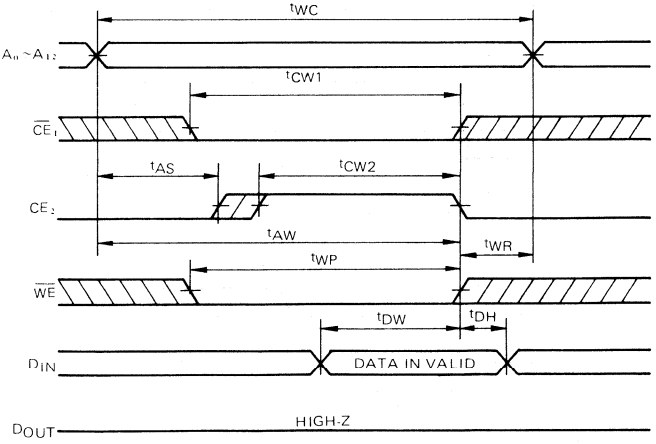
WRITE CYCLE TIMING CHART [1], [2], [3]
($\overline{WE}$ CONTROLLED)



WRITE CYCLE TIMING CHART [1], [2]
($\overline{CE}_1$ CONTROLLED)



WRITE CYCLE TIMING CHART [1], [2]
(CE_2 CONTROLLED)



Notes [1] A Write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.

[2] $\overline{CE}_1$ or $\overline{WE}$ (or CE_2) must be high (low) during address transitions.

[3] If $\overline{OE}$ is high, I/O pins remain in a high impedance state.

[4] During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

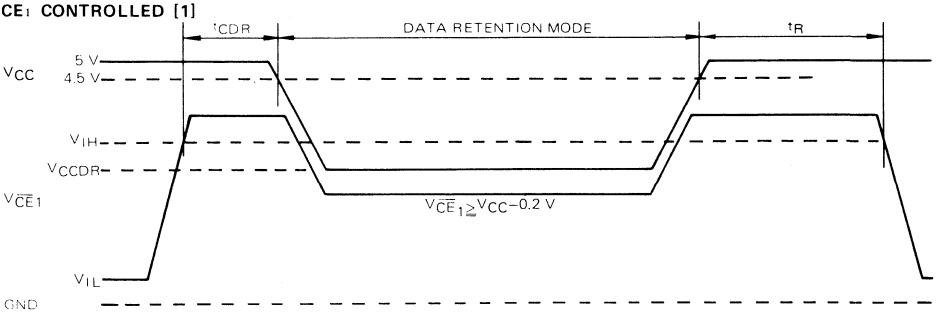
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a=0 to 70 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR1}	2.0		5.5	V	$V_{\overline{CE}1} \geq V_{CC}-0.2$ V, $V_{CE2} \geq V_{CC}-0.2$ V
	V_{CCDR2}	2.0		5.5	V	$V_{CE2} \leq 0.2$ V
Data Retention Supply Current	I_{CCDR1}		1	①	μA	V_{CC}=3.0 V, $V_{\overline{CE}1} \geq V_{CC}-0.2$ V $V_{CE2} \geq V_{CC}-0.2$ V or $V_{CE2} \leq 0.2$ V
	I_{CCDR2}		1	①	μA	V_{CC}=3.0 V, $V_{CE2} \leq 0.2$ V
Chip Deselection to Data Retention Mode	t_{CDR}	0			ns	
Operation Recovery Time	t_R	t_{RC}**			ns	

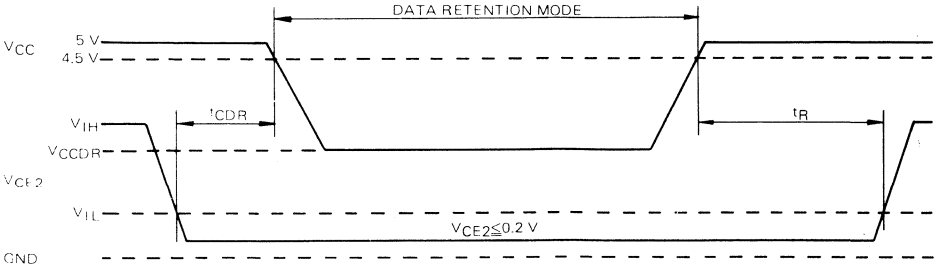
Note ① μPD4364CX-10L/-12L/-15L/-20L ..... 50 μA MAX.; 15 μA MAX. (0 to 40°C)

DATA RETENTION TIMING CHART

$\overline{CE}_1$ CONTROLLED [1]



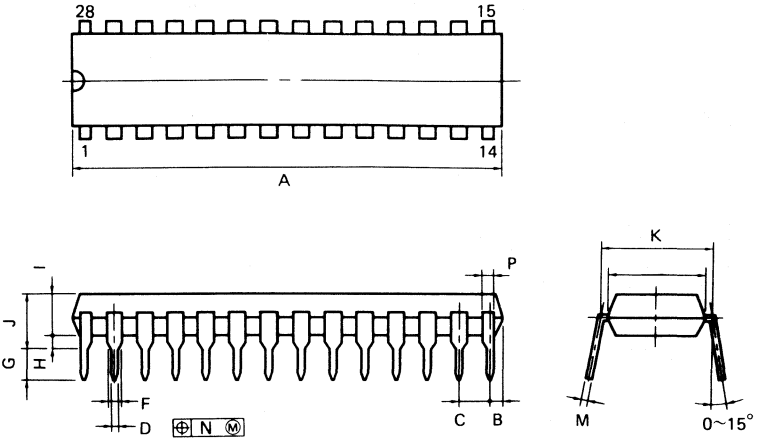
CE_2 CONTROLLED [2]



Notes [1] CE_2 must be equal to or higher than $V_{CC}-0.2$ V, the other inputs (Address, $\overline{OE}$, $\overline{WE}$, I/O_s) can be in high impedance state.
[2] The input (Address, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, I/O_s) can be in a high impedance state.

28 PIN Plastic DIP (300 mil)

ITEM	MILLIMETERS
A	35.56 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	$0.50^{+0.10}$
F	1.2 MIN.
G	$3.2^{+0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.7
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	1.0 MIN.



65,536 Bit Static CMOS RAM

Description

The μPD4464C/G is a high speed, low power, 8192 words by 8 bits static CMOS RAM fabricated with a silicon-gate CMOS technology. The μPD4464C/G is a very low standby power device using full CMOS memory cell with 6 transistors. Furthermore, a unique circuitry technique makes the μPD4464C/G a very low operating power device which requires no clock or refreshing to operate.
Two chip enable inputs are provided for battery back-up application, and one output enable input for easy interface.
Data retention is guaranteed at a power supply voltage as low as 2 volts.
The μPD4464C is packaged in a standard 28-pin dual-in-line plastic package and plug-in compatible with 2764 type EPROMs.
The μPD4464G is packaged in a mini flat package providing high density application.

Features

- Single + 5V Supply
- Fully Static Operation - No Clock or Refreshing required
- TTL Compatible - All Inputs and Outputs
- Common I/O Using Three-State Output
- Two Chip Enable and One Output Enable Inputs for Easy Application
- Fast Access Time

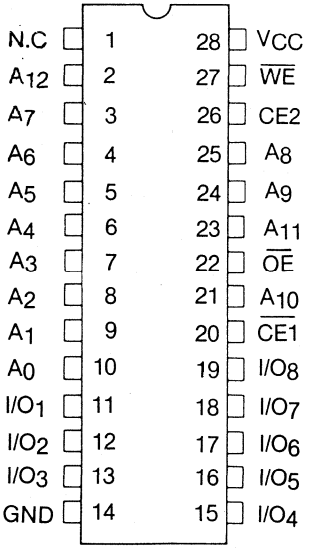
μPD4464C/G-12L	120ns max
μPD4464C/G-15L	150ns max
μPD4464C/G-20L	200ns max

- Low Power Dissipation

Active	μPD4464C/G-12L	40mA max
	μPD4464C/G-15L	40mA max
Standby	μPD4464C/G-20L	35mA max

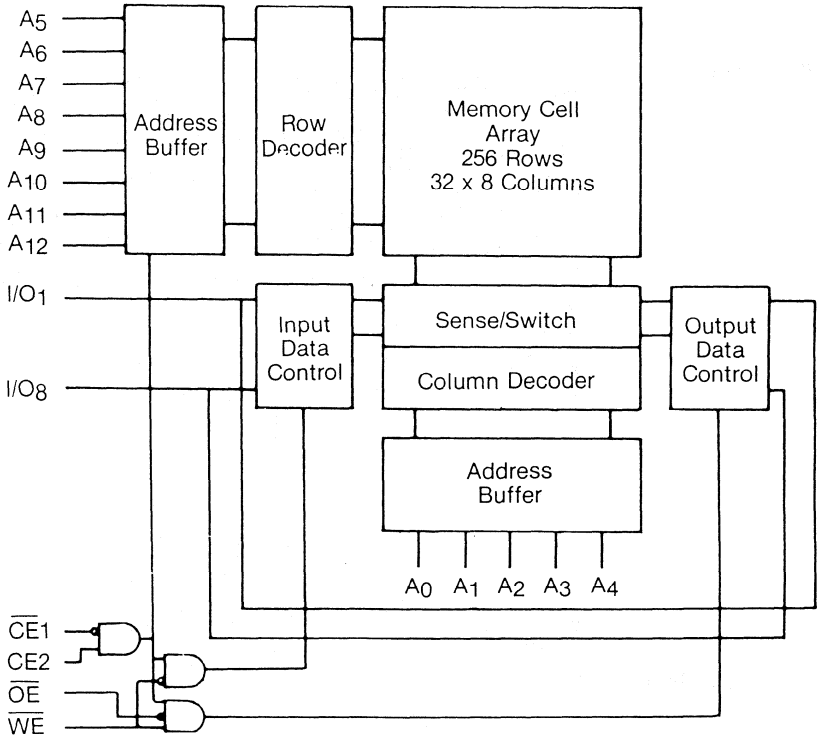
- Data Retention Voltage -2V min — 1.0μA max at Ta = 60°C / 0.2μA max at Ta = 25°C
- Standard 28-pin Plastic Package (μPD4464C)
- Plug-in Compatible with 2764 type EPROMs (μPD4464C)
- 28-pin Mini Flat Package (μPD4464G)

Pin Configuration and Function



A_0 - A_{12}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CE}1$	Chip Enable Active Low
CE2	Chip Enable Active High
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
GND	Ground
N.C	No Connection

Block Diagram



Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	ICC
H	X	X	X	Not selected	HZ	Standby
X	L	X	X	Not selected	HZ	Standby
L	H	H	H	Dout disable	HZ	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Item	Ratings	Unit
V_{CC}	Supply Voltage	−0.5* to 7.0	V
V_{IN}	Input Voltage	−0.5* to V_{CC} + 0.5	V
V_{OUT}	Output Voltage	−0.5* to V_{CC} + 0.5	V
Topr	Operating Temperature	−40 to + 85	°C
Tstg	Storage Temperature	−55 to + 125	°C
Pd	Power Dissipation	1.0	W

*−3.0V min. (pulse width 50ns)

Recommended DC Operating Conditions (Ta = −40 to +85°C)

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IL}	Input Low Voltage	−0.3*		0.8	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.5	V

*−3.0V min. (Pulse Width 50ns)

DC Characteristics (Ta = −40 to 85°C, V_{CC} = 5V±10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0~V_{CC}	-1		1	μA
I/O Leakage Current	I_{LO}	$V_{I/O}$ = 0~V_{CC} $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	-1		1	μA
Operating Supply Current	I_{CCA1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} Min. Cycle $I_{I/O}$ = 0			(1)	mA
Operating Supply Current	I_{CCA2}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0, DC Current		5	10	mA
Standby Supply Current	I_{CCS1}	$\overline{CE1}$ ≧ V_{CC} −0.2V CE2 ≧ V_{CC} −0.2V		0.004	(2)	μA
Standby Supply Current	I_{CCS2}	CE2 ≦ 0.2V		0.004	(2)	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4			V

Notes (1) μPD4464C/G-12L 40mA Max
μPD4464C/G-15L 40mA Max
μPD4464C/G-20L 35mA Max

(2) μPD4464C/G-12L/15L/20L 1.0μA Max. (Ta = −40 to 60°C)
0.2μA Max. (Ta = −40 to 25°C)
4.0μA Max. (Ta = −40 to 85°C)

Capacitance (Ta = 25°C f = 1MHz)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	8	pF

AC Test Conditions

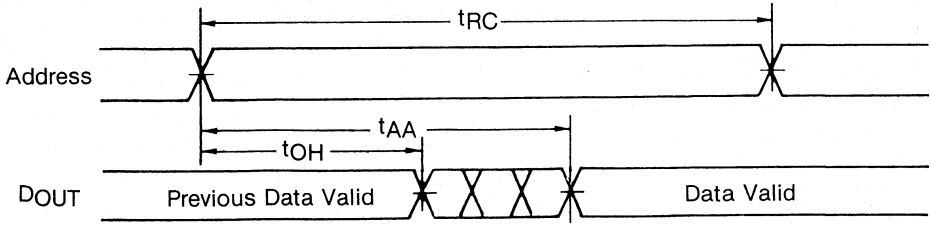
Input Pulse Levels	0.8 to 2.4V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	1TTL Gate and CL = 100pF

AC Characteristics (Ta = −40 to 85°C, V_{CC} = 5V±10%)
Read Cycle

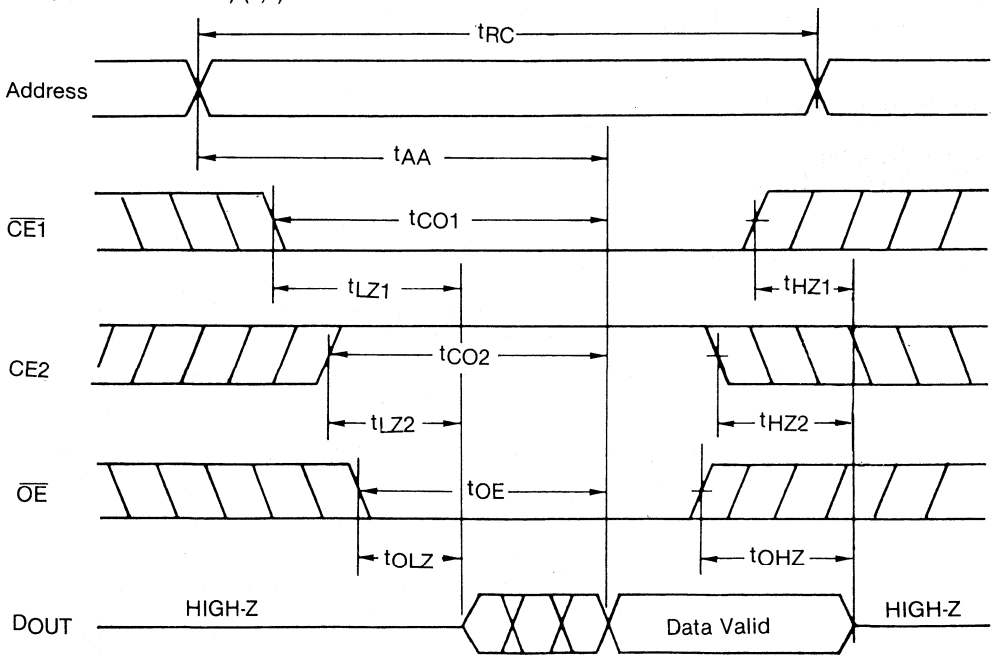
Parameter	Symbol	μPD4464C/G −12L		μPD4464C/G −15L		μPD4464/CG −20L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
$\overline{CE}$ 1 Access Time	t_{CO1}		120		150		200	ns
CE2 Access Time	t_{CO2}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		80		75		100	ms
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Enable ($\overline{CE}$1) to Output in LZ	t_{LZ1}	10		10		10		ns
Chip Enable (CE2) to Output in LZ	t_{LZ2}	10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	8		5		5		ms
Chip Enable ($\overline{CE}$1) to Output in HZ	t_{HZ1}		40		75		100	ns
Chip Enable (CE2) to Output in HZ	t_{HZ2}		40		75		100	ns
Output Enable to Output in HZ	t_{OHZ}		40		60		80	ns

Read Cycle Timing Chart

Read Cycle No. 1 (Address Access) (1) (2)



Read Cycle No. 2
(Chip Enable Access) (1,3)



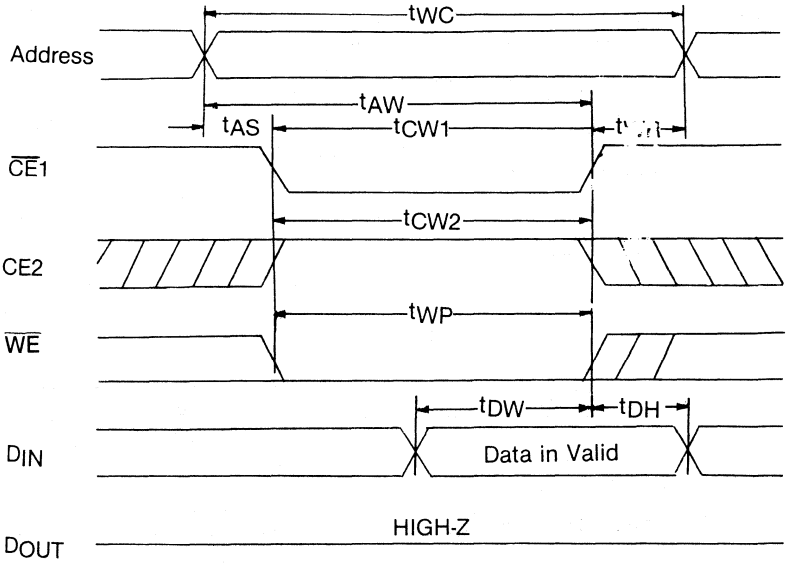
Notes: 1) $\overline{WE}$ is high for read cycle.
2) Device is continuously selected, $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}
3) Address valid prior to or coincident with $\overline{CE1}$ transition low, CE2 transition high.

Write Cycle

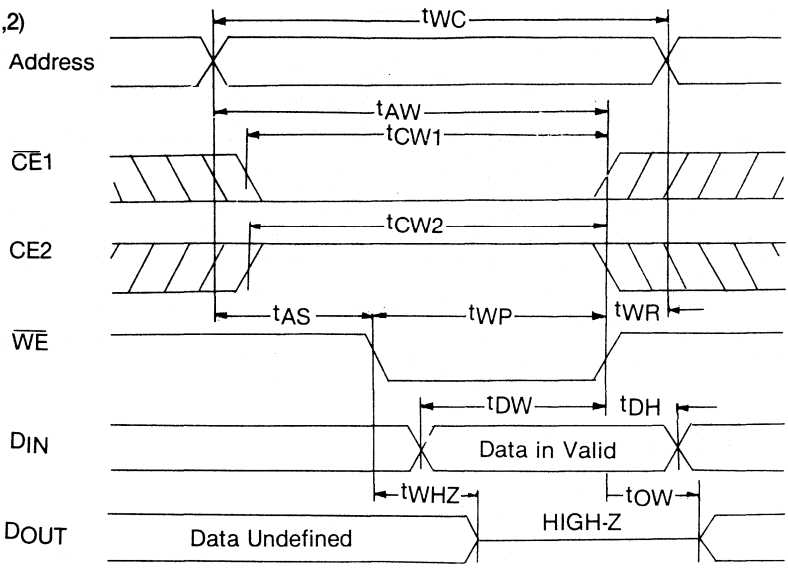
Parameter	Symbol	μPD4464C/G -15L		μPD4464C/G -20L		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	150		200		ns
Chip Enable ($\overline{CE}$1) to End of Write	t_{CW1}	130		180		ns
Chip Enable (CE2) to End of Write	t_{CW2}	130		180		ns
Address Valid to End of Write	t_{AW}	130		180		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	100		140		ns
Write Recovery Time	t_{WR}	5		5		ns
Data Valid to End of Write	t_{DW}	70		80		ns
Data Hold Time	t_{DH}	5		5		ns
Write Enable to Output in HZ	t_{WHZ}		75		100	ns
Output Active from End of Write	t_{CW}	10		10		ns

Write Cycle Timing Chart

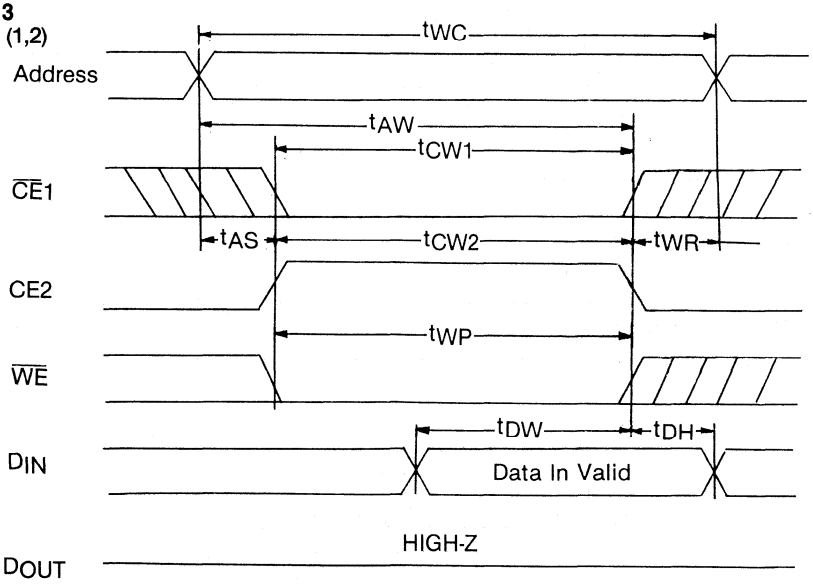
Write Cycle No. 1
($\overline{WE}$ Controlled) (1,2,3)



Write Cycle No. 2
($\overline{CE1}$ Controlled) (1,2)



Write Cycle No. 3
(CE2 Controlled) (1,2)



Notes: 1) A write occurs during the overlap of a low $\overline{CE1}$ and a high CE2 and a low $\overline{WE}$.
2) $\overline{CE1}$ or $\overline{WE}$ (or CE2) must be high (low) during address transition.
3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

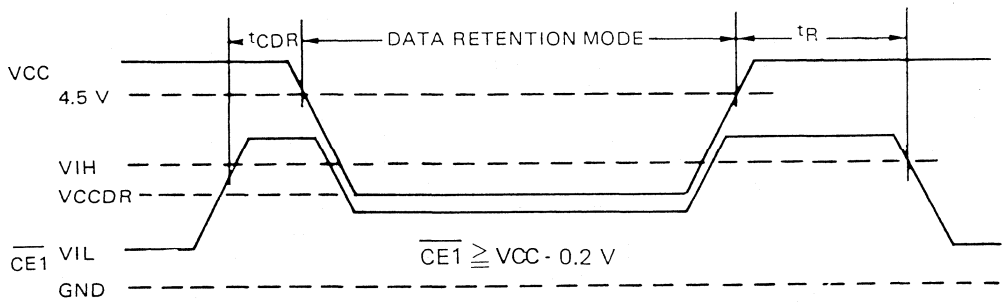
Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Data Retention Supply Voltage	V_{CCDR1}	$\overline{CE1} \geqq V_{CC} - 0.2V$ CE2 $\geqq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Supply Voltage	V_{CCDR2}	CE2 $\leqq$ 0.2V	2.0		5.5	V
Data Retention Supply Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CE1} \geqq V_{CC} - 0.2V$ CE2 $\geqq V_{CC} - 0.2V$		0.01	(1)	μA
Data Retention Supply Current	I_{CCDR2}	V_{CC} = 3.0V CE2 $\geqq$ 0.2V		0.01	(1)	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

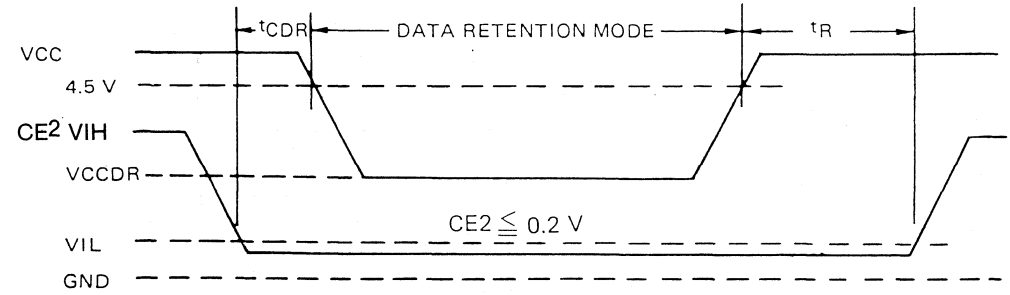
Notes (1) μPD4464C/G-15L/20L 1.0μA Max. (Ta = −40 to 60°C)
0.2μA Max. (Ta = −40 to 25°C)

Data Rentention Timing

(CE1 Controlled) (1)



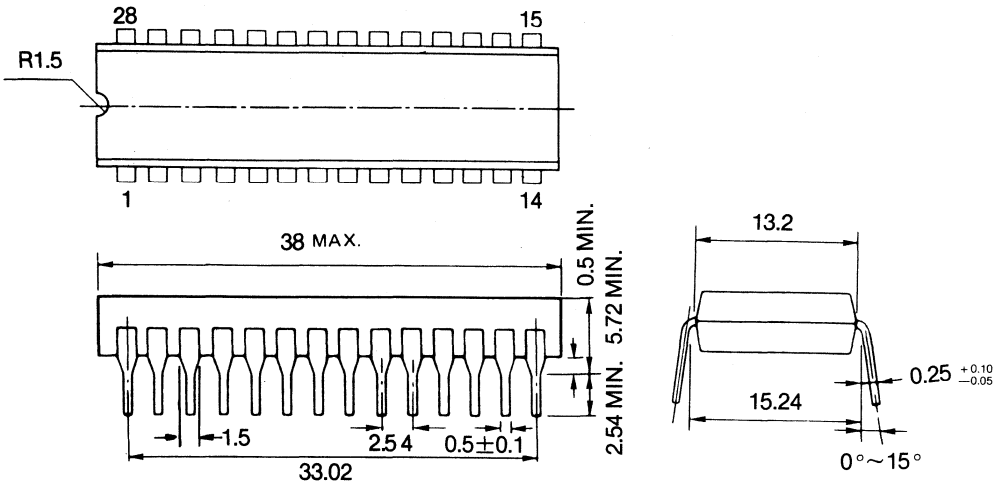
(CE2 Controlled) (2)



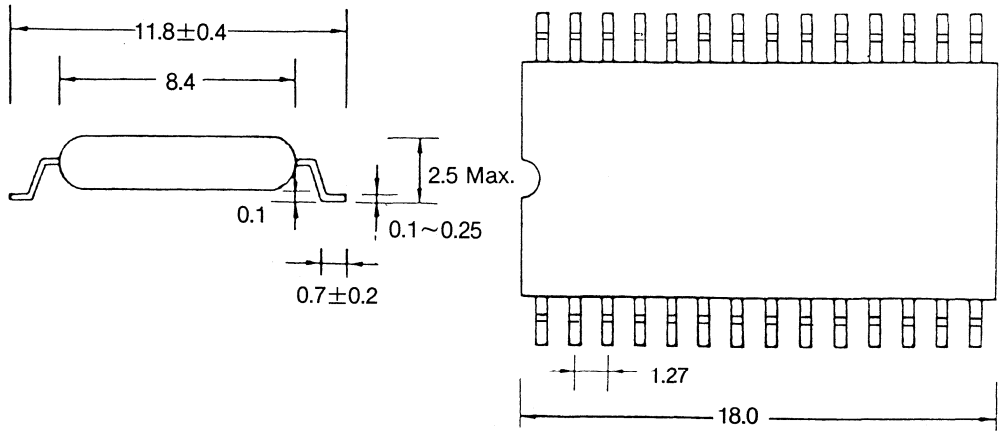
NOTES: 1. $\overline{CE_2}$ must be equal to or higher than V_{CC} = 0.2V. The other inputs Addresses, $\overline{WE}$, $\overline{OE}$, I/Os) can be in a high impedance.

2. The inputs (Adresses, $\overline{CE_2}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

Package Outline μPD4464C Plastic



μPD4464G Mini Flat



262, 144 Bit STATIC CMOS RAM *

Description

The μPD43251C is a high speed, low power, 262,144 words by 1 bit static CMOS RAM fabricated with short channel silicongate CMOS process. The μPD43251C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD43251C requires no clock or refreshing to operate. Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 35ns, 45ns and 55ns.

Features

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and an Output
- Separated Data Input and Output
- Three-State Output
- Fast Access Time

μPD43251C-35	35ns MAX
μPD43251C-45	45ns MAX
μPD43251C-55	55ns MAX

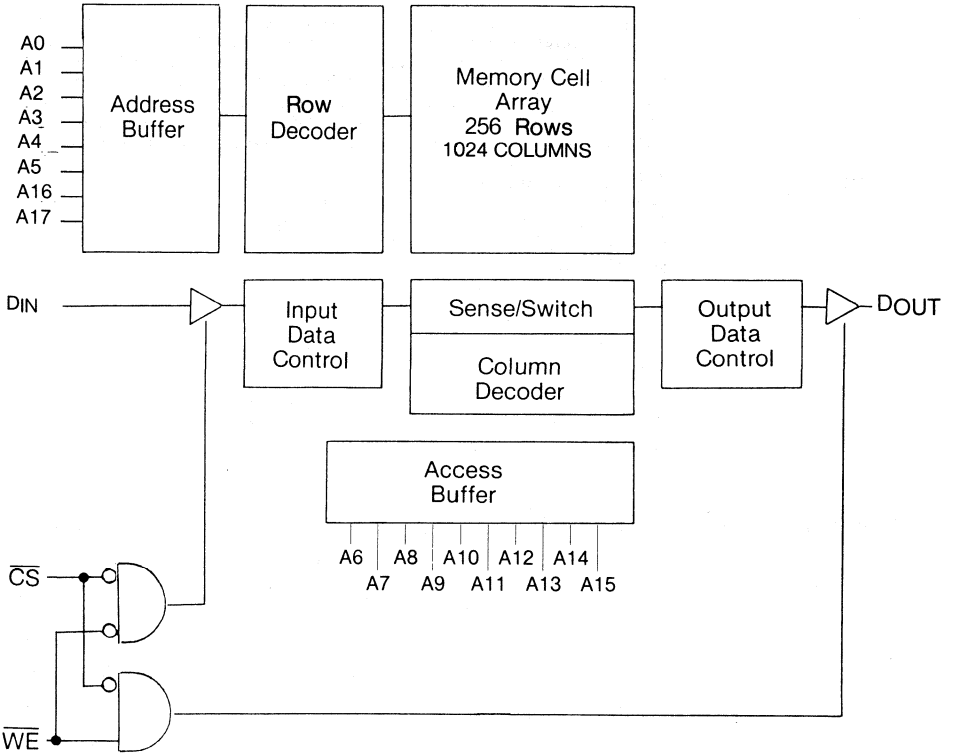
- Low Standby Current 20mA MAX
- Low Active Current 90mA MAX
- Standard 300 mil 24-pin Plastic DIP

Pin Configuration

A0	1	24	VCC	A0 – A17	ADDRESS INPUT
A1	2	23	A17	DIN	DATA-INPUT
A2	3	22	A16	DOUT	DATA-OUTPUT
A3	4	21	A15	$\overline{CS}$	CHIP SELECT
A4	5	20	A14	$\overline{WE}$	WRITE ENABLE
A5	6	19	A13	VCC	POWER (+5V)
A6	7	18	A12	VSS	GND
A7	8	17	A11		
A8	9	16	A10		
DOUT	10	15	A9		
$\overline{WE}$	11	14	DIN		
VSS	12	13	$\overline{CS}$		

*under development

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0V min. while 20ns pulse width.

Recommended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V

Note (1) −3.0V min. while 20ns pulse width

Capacitance (Ta = 25 °C f = 1 MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data Output Capacitance	C_{DOUT}	V_{DOUT} = 0V	6	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0° to 70 °C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}, V_{CC} = Max.	−2		2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max.	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA		80	90	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V, V_{IN} < 0.2V or > V_{CC} −0.2V			2	mA
Output low Voltage	V_{OL}	I_{OL} = 8.0mA			0.4	V
Output High Voltage	I_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

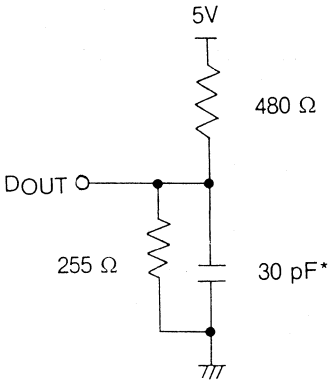


Figure 1 Output Load

*Including Scope and jig

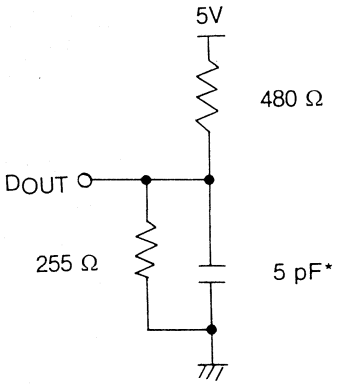


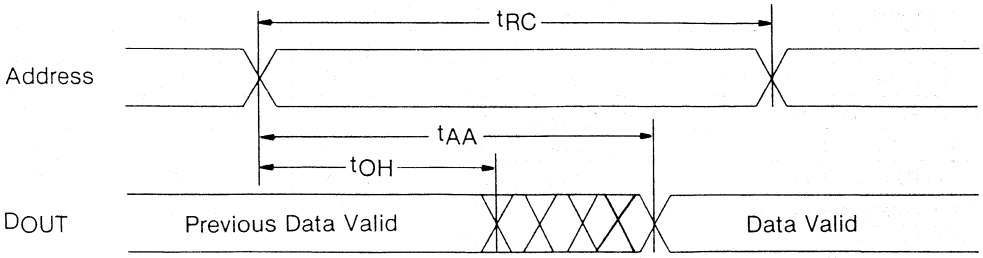
Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

AC Characteristics ($T_a = 0°$ to $70°C$, $V_{CC} = 5V \pm 10\%$)
Read Cycle

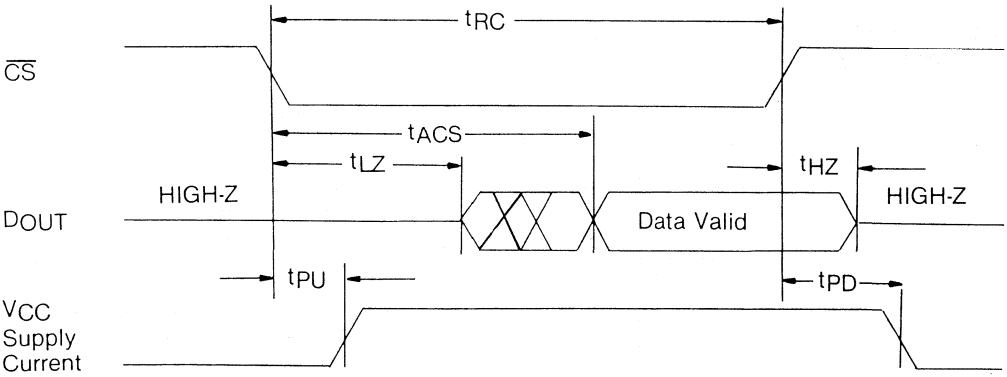
Parameter	Symbol	μPD43251 C–35		μPD43251 C–45		μPD43251 C–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	20	0	25	0	30	ns
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns
Chip Selection to Power-Down Time	t_{PD}	0	TBD	0	TBD	0	TBD	ns

Read Cycle Waveforms

Read Cycle No. 1
(Address Access) (4) (5)



Read Cycle No. 2
(Chip Select Access) (4) (6)



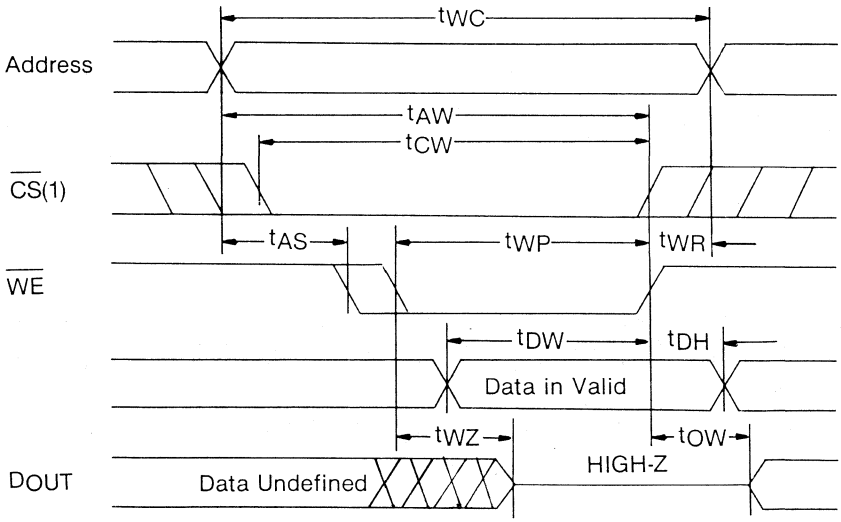
Notes: (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
(3) Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified load in Figure 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continuously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

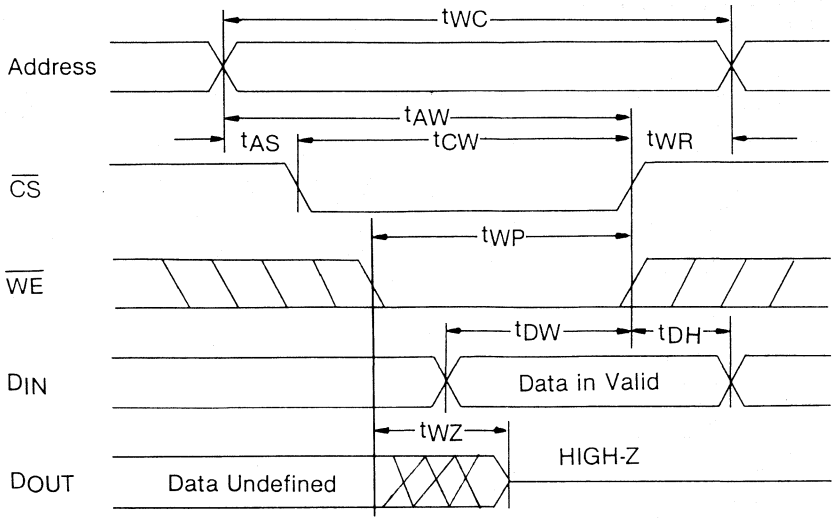
Parameter	Symbol	μPD43251 C–35		μPD43251 C–45		μPD43251 C–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}(2)	35		45		55		ns
Chip Selection to end of Write	t_{CW}	35		40		45		ns
Address Valid to end of Write	t_{AW}	35		40		45		ns
Address Setup Time	t_{AS}	TBD		TBD		TBD		ns
Write Pulse Width	t_{WP}	30		40		50		ns
Write Recovery Time	t_{WR}	TBD		TBD		TBD		ns
Data Valid to end od Write	t_{DW}	20		25		25		ns
Data hold Time	t_{DH}	TBD		TBD		TBD		ns
Write Enabled to Output in HZ	t_{WZ}(3)	0	20	0	25	0	30	ns
Output Active from end of Write	t_{OW}(4)	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1
($\overline{WE}$ Controlled) (5)



Write Cycle No. 2
($\overline{CS}$ Controlled) (5)

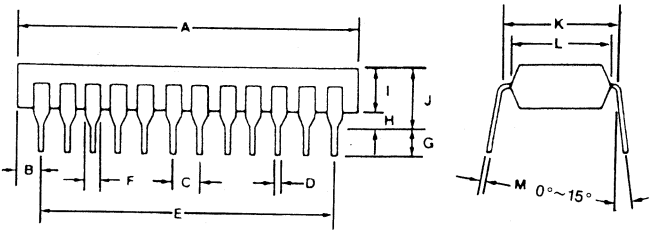


Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimensions

24 Pin Plastic Shrinkdip
μPD43251C

Item	Millimeters
A	33 max.
B	1.03
C	2.54
D	0.5±0.1
E	27.94
F	1.5
G	2.54 min.
H	0.5 min.
I	5.22 max.
J	5.72 max.
K	7.62
L	6.4
M	$0.25^{+0.01}_{-0.05}$



262,144 BIT STATIC CMOS RAM *

DESCRIPTION

The μPD43254C is a high speed, low power, 65,531 words by 4 bit static CMOS RAM fabricated with short channel silicongate CMOS process. The μPD43254C is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, an excellent circuitry technique achieves very high speed and low operating power. The μPD43254C requires no clock or refreshing to operate. Two kinds of access time, address access time and chip select access time, are the same and very fast. The grades of access time are 35ns, 45ns and 55ns.
The μPD43254C is packaged in a 24-pin plastic Dual In-line Package (DIP) used with the standard JEDEC pin configuration.

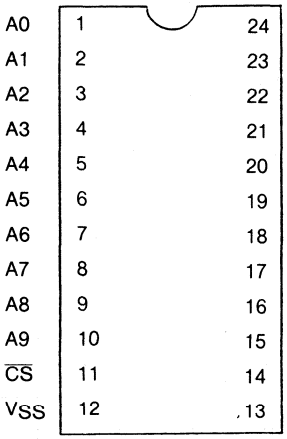
FEATURES

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and Output
- Common I/O Capability
- Three-State Output
- Fast Access Time

μPD43254C-35	35ns MAX
μPD43254C-45	45ns MAX
μPD43254C-55	55ns MAX

- Low Standby Current 20mA TYP
- Low Active Current 120mA
- Standard 300 mil 20-pin Plastic DIP

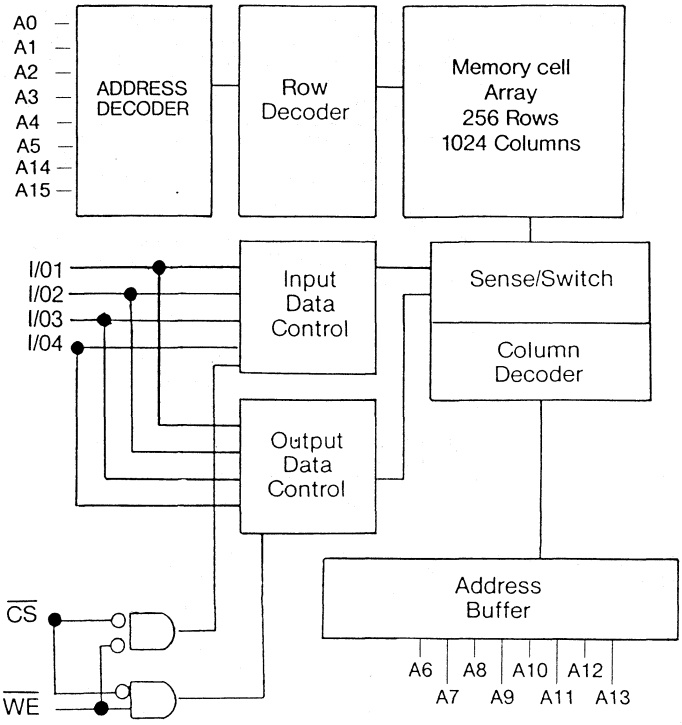
Pin Configuration and Function



A0 - A15	ADDRESS INPUT
I/O1 - I/O4	DATA-INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER (+5V)
V_{SS}	GND

*under development

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not Selected	High Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High Z	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
All Input and Output Voltage	V_{IN}	−0.5(1) to 7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Note (1) V_{IN} = −3.0V min. while 20ns pulse width.

Recommended DC Operating Conditions (T_A = 0° to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.5(1)		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

Note (1) V_{IL} = −3.0V Min. while 20ns pulse width.

Capacitance Ta = 25°C f = 1MHz) (1)

Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data-Output Capacitance	C_{DOUT}	V_{DOUT}=0V	7	pF

Note (1) This parameter is sampled and not 100% tested.

DC Characteristics (Ta = 0° to 70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0~V_{CC}, V_{CC} = Max.	−2		2	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0~V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max.	−2		2	μA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0mA			120	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}			20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} −0.2V V_{IN} ≤0.2V or≥ V_{CC} −0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA			0.4	
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Pulse Rise and Fall Time	5ns
Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

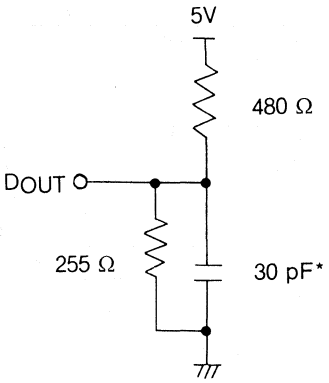


Figure 1 Output Load

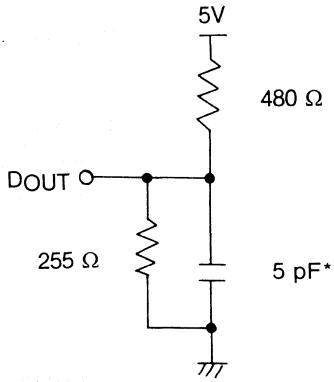


Figure 2 Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

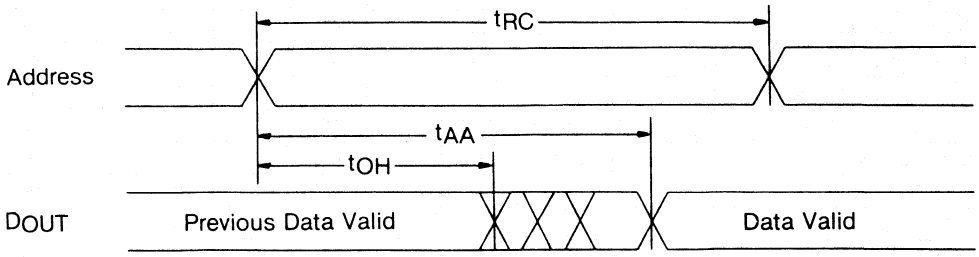
*Including Scope and Jig

AC Characteristics ($T_a = 0°$ to $70°C$, $V_{CC} = 5V \pm 10\%$)
Read Cycle

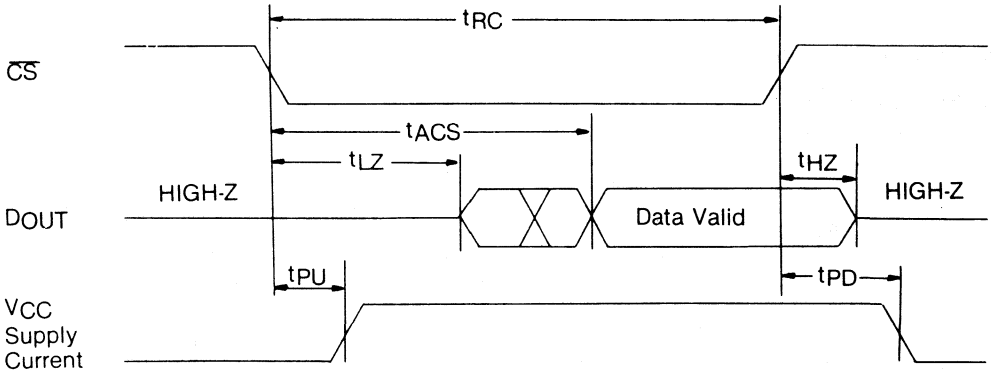
Parameter	Symbol	μPD43254 -35		μPD43254 -45		μPD43254 -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}(1)	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low Z	t_{LZ}(2)	5		5		5		ns
Chip Deselection to Output in High Z	t_{HZ}(3)	0	20	0	25	0	30	ns
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power-Down Time	t_{PD}	0	35	0	45	0	55	ns

Read Cycle Waveforms

Read Cycle No. 1 (Address Access) (4) (5)



Read Cycle No. 2 (Chip Select Access) (4) (6)



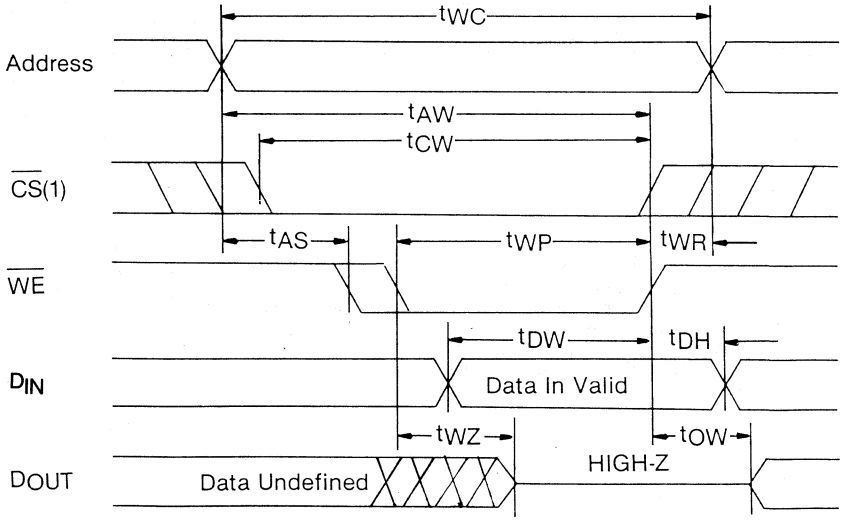
Notes (1) All Read Cycle timings are referenced from the last valid address to the first transitioning address.
(2) Transition is measured ±200 mV from steady state voltage with specified loading in FIGURE 2.
(3) Transition is measured at V_{OL} + 200mV and V_{OH}-200mV with specified load in FIGURE 2.
(4) $\overline{WE}$ is high for Read Cycle.
(5) Device is continously selected, $\overline{CS} = V_{IL}$.
(6) Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

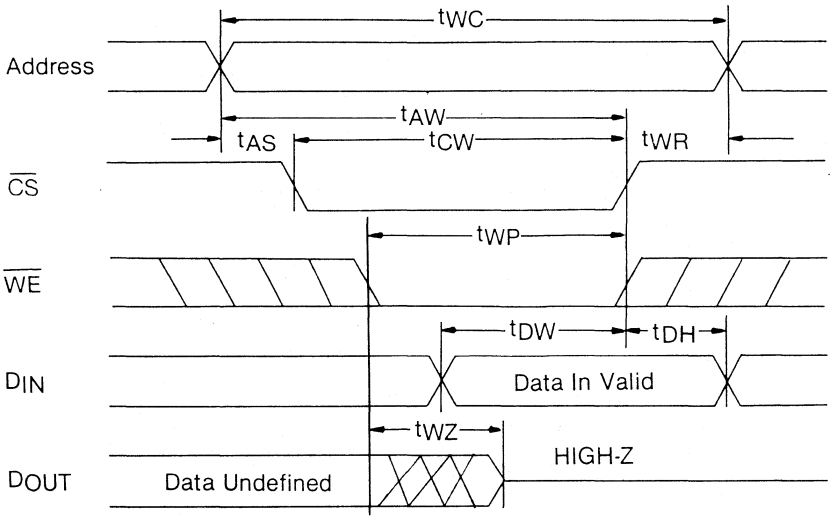
Parameter	Symbol	μPD43254 —45		μPD43254 —55		μPD43254 —70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}(2)	35		45		55		ns
Chip Selection to end of Write	t_{CW}	35		40		45		ns
Address Valid to end of Write	t_{AW}	35		40		45		ns
Address Setup Time	t_{AS}	TBD		TBD		TBD		ns
Write Pulse Width	t_{WP}	30		40		50		ns
Write Recovery Time	t_{WR}	TBD		TBD		TBD		ns
Data Valid to end od Write	t_{DW}	20		25		25		ns
Data hold Time	t_{DH}	TBD		TBD		TBD		ns
Write Enabled to Output in HZ	t_{WZ}(3)	0	20	0	25	0	30	ns
Output Active from end of Write	t_{OW}(4)	0		0		0		ns

Write Cycle Waveforms

Write Cycle No. 1
($\overline{WE}$ Controlled) (5)



Write Cycle No. 2
($\overline{CS}$ Controlled) (5)

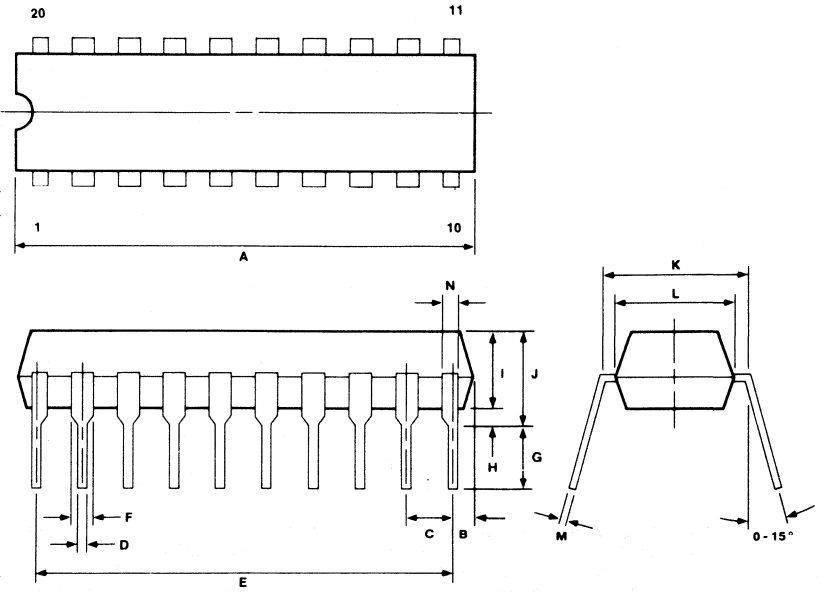


Notes: (1) If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
(2) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
(3) Transition is measured at V_{OL} + 200mV and V_{OH} −200mV with specified loading in Figure 2.
(4) Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
(5) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Dimension

20 PIN Plastic DIP (300 mil)

μPD43254C



Item	Millimeters
A	25.40 max
B	1.27 max
C	2.54 [TP]
D	.50 ± .10
E	22.86
F	1.1 min
G	3.5 ± .30
H	.51 min
I	4.31 max
J	5.08 max
K	7.62 [TP]
L	6.4
M	$.25^{+.10}_{-.05}$
N	.9 min

262 144 BIT STATIC CMOS RAM

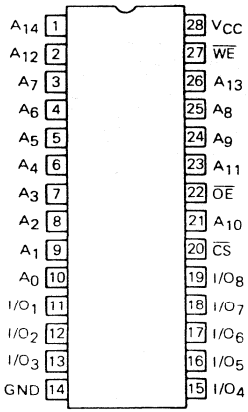
Description

The μPD43256C/GU is a high speed, low power, 32768 words by 8 bits static CMOS RAM fabricated with advanced silicon-gate CMOS technology. The μPD43256C/GU is a low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD43256C/GU a high speed and low operating power device which requires no clock or refreshing to operate.
Minimum standby power is drawn by this device when $\overline{CS}$ is at a high level, independently of the other inputs level.
Data retention is guaranteed at a power supply voltage as low as 2 volts. (μPD43256C/GU-10L/12L/15L)
The μPD43256C is packaged in a standard 28-pin dual-in-line plastic package. The μPD43256GU is packaged in a mini flat package providing high density application.

Features

- Single +5V Supply
- Fully Static Operation: No Clock or Refreshing required
- TTL Compatible: All Inputs and Outputs
- Commom I/O Using Three-State Output
- One Chip Select and One Output Enable Inputs for easy Application
- Fast Access Time:
  - μPD43256C/GU-10L 100ns MAX
  - μPD43256C/GU-12L 120ns MAX
  - μPD43256C/GU-15L 150ns MAX
- Low Power Dissipation:
  - Active 70mA MAX.
  - Standby μPD43256C/GU-10L/12L/15L 100μA MAX.
  - Data Retention 1μA MAX.
- Data Retention Voltage: 2V MIN. (μPD43256C/GU-10L/12L/15L)
- Standard 28-pin Plastic Package (μPD43256C)
- Miniflat package (μPD43256GU)

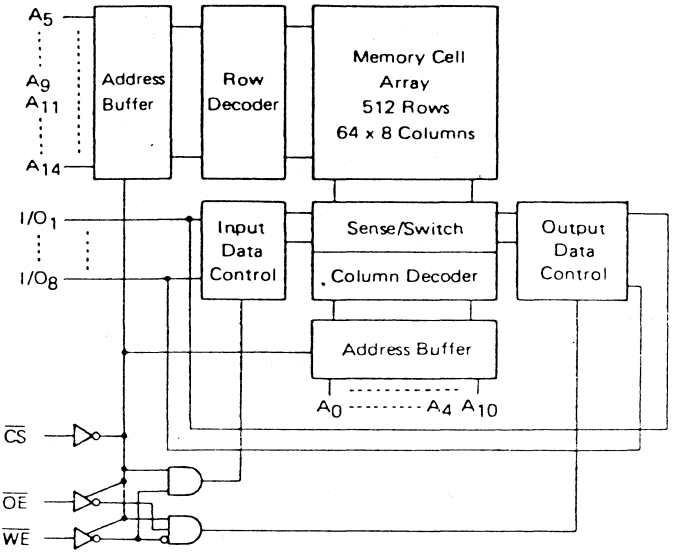
PIN CONFIGURATION



PIN NAMES

A_0–A_{14}	Address Input
I/O_1–I/O_8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5 V)
GND	GND

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	Not Selected	HZ	Standby
L	H	H	Not Selected	HZ	Active
L	L	H	Read	DOUT	Active
L	X	L	Write	DIN	Active

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5* to 7.0	V
Input Voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Output Voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

***COMMENT**

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.

* −3.0V MIN. (Pulse Width 50 ns)

μPD43256GU should be soldered by Vapour Phase soldering process. Pre-Baking is recommended. Infrared Reflow soldering is not applicable.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.3 **	–	0.8	V
Ambient Temperature	T_a	0	–	70	°C

** −3.0 V MIN. (Pulse Width 50 ns)

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Leakage Currnet	I_{LI}	−1		1	μA	V_{IN}=0 to V_{CC}
I/O Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$=0 to V_{CC}, $V_{\overline{CS}}=V_{IH}$ or $V_{\overline{OE}}=V_{IH}$ or $V_{\overline{WE}}=V_{IL}$
Operating Supply Current	I_{CCA}		(1)	70	mA	$V_{\overline{CS}}=V_{IL}$, MIN. CYCLE $I_{I/O}$=0
Standby Supply Current	I_{SB}			(2)	mA	$V_{\overline{CS}}=V_{IH}$
	I_{SB1}		(3)	(3)	mA	$V_{\overline{CS}} \geq V_{CC}-0.2$ V
Output Low Voltage	V_{OL}			0.4	V	I_{OL}=2.1 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH}=−1.0 mA

Note: (1) μPD43256C/GU-10L 35 mA TYP.
μPD43256C/GU-12L 30 mA TYP.
μPD43256C/GU-15L 25 mA TYP.
(2) μPD43256C/GU-10L/-12L/-15L 3mA MAX.
(3) μPD43256C/GU-10L/-12L/-15L 2μA TYP. 100 μA MAX.

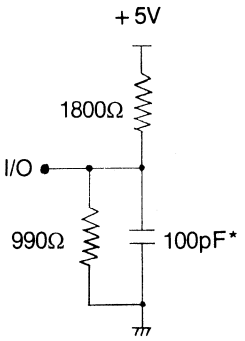
CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V

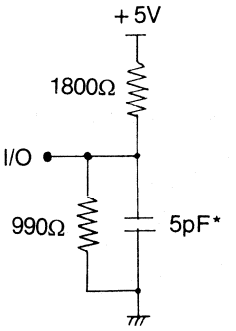
Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Pulse Rise and fall Time	5ns
Timing Reference Levels	1.5V

Output Load



for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}

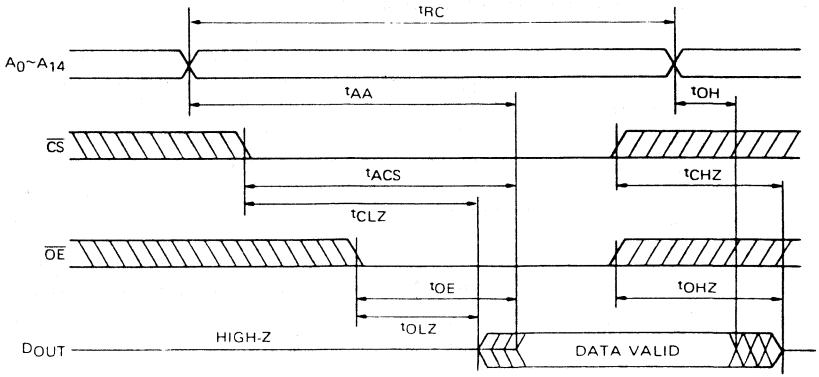


*including scope and jig.

READ CYCLE

Parameter	Symbol	μPD43256C/GU -10L		μPD43256C/GU -12L		μPD43256C/GU -15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Chip Select Access Time	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output in Low Z	t_{CLZ}	10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	5		5		5		ns
Chip Select to Output in HZ	t_{CHZ}		35		40		50	ns
Output Enable to Output in HZ	t_{OHZ}		35		40		50	ns

READ CYCLE TIMING CHART [1], [2], [3]



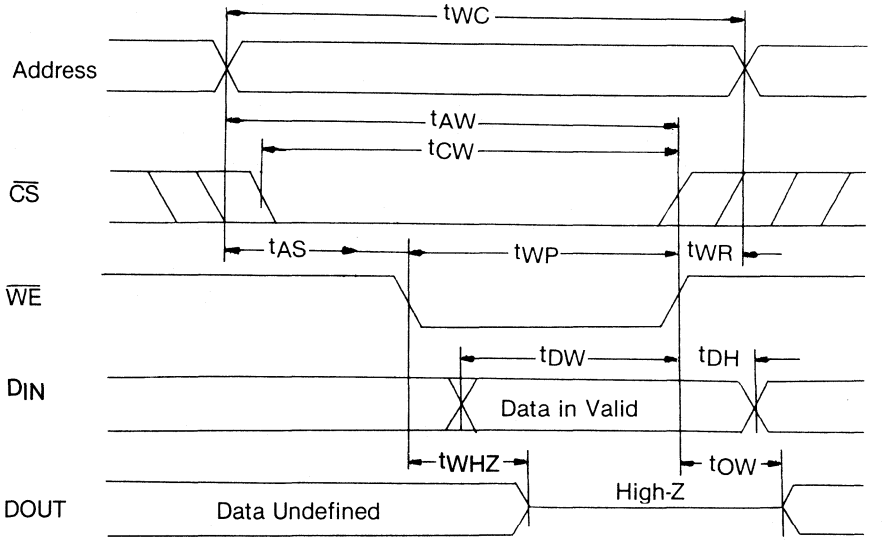
Notes [1] $\overline{WE}$ is high for read cycle.
[2] Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.
[3] Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

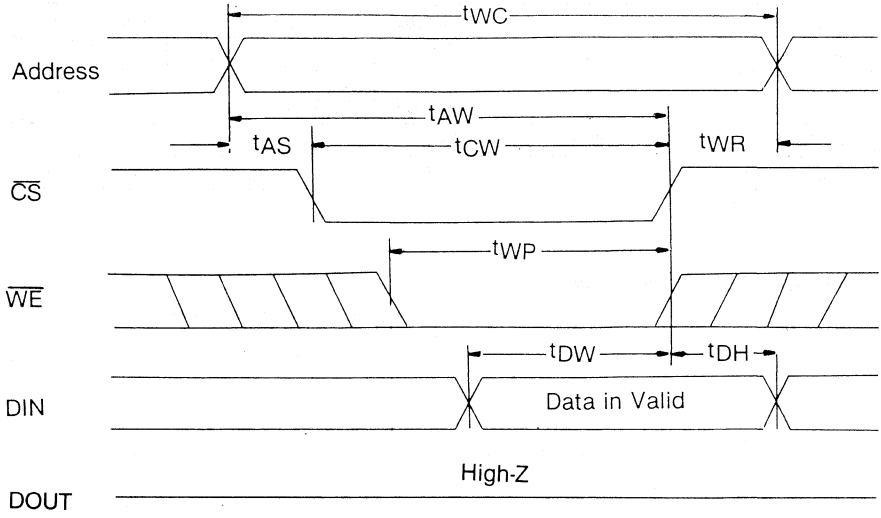
Parameter	Symbol	μPD43256C/GU -10L		μPD43256C/GU -12L		μPD43256C/GU -15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	100		120		150		ns
Chip Select to End of Write	tCW	80		85		100		ns
Address Valid to End of Write	tAW	80		85		100		ns
Address Set-up Time	tAS	0		0		0		ns
Write Pulse Width	tWP	70		70		90		ns
Write Recovery Time	tWR	5		5		5		ns
Data Valid to End of Write	tDW	40		50		60		ns
Data Hold Time	tDH	0		0		0		ns
Write Enable to Output in HZ	tWHZ		35		40		50	ns
Output Active from End of Write	tOW	10		10		10		ns

Write Cycle Timing Chart

Write Cycle No. 1 ($\overline{WE}$ Controlled) (1) (2) (3)



Write Cycle No. 2 ($\overline{CS}$ Controlled) (1) (2)

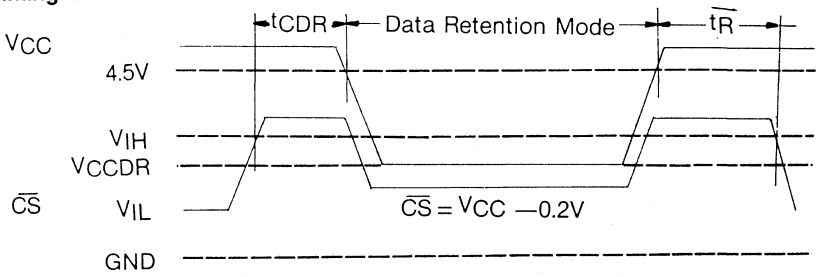


Notes (1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
(3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
(4) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Data Retention Supply Voltage	V_{CCDR}	$\overline{CS} \geq V_{CC}$ −0.2V	2.0		5.5	V
Data Retention Supply Current	I_{CCDR}	V_{CC} = 3.0V $\overline{CS} \geq V_{CC}$ −0.2V		1	50	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

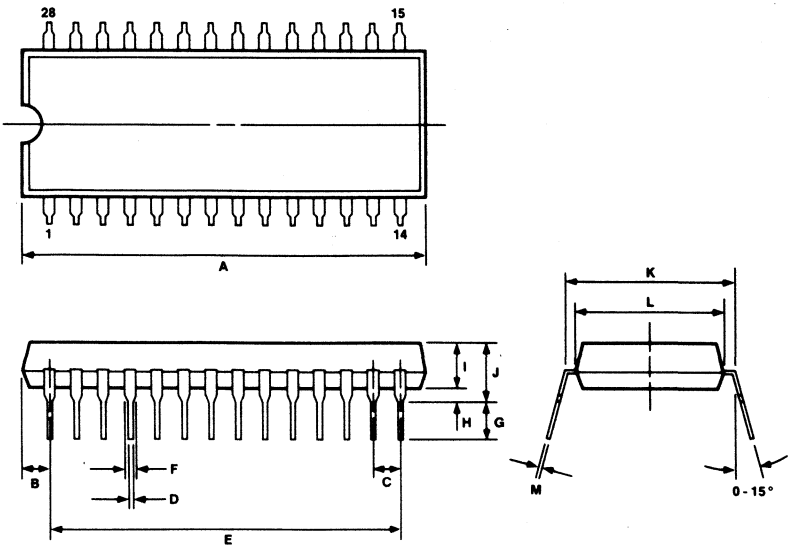
Data Retention Timing Chart



Notes: The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/O's) can be in High Impedance state.

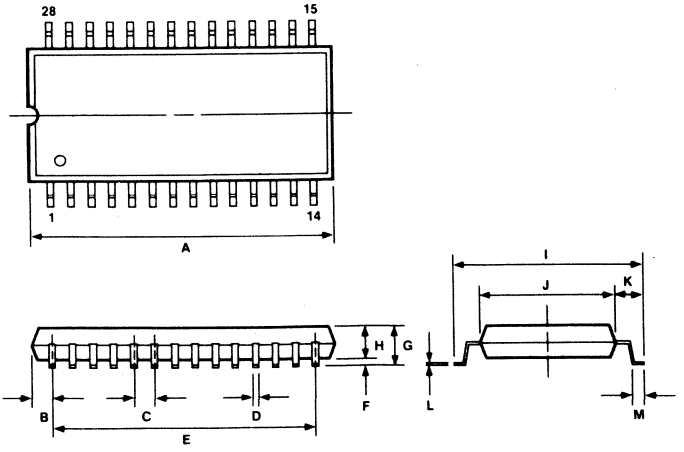
28 PIN Plastic DIP (600 mil)

Item	Millimeters
A	38.10 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	33.02
F	1.2 min
G	3.5 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	14.66
M	.25 ± .05
N	8.89 dia



28 PIN Miniflat

Item	Millimeters
A	19.05 max
B	1.27 max
C	1.27 [TP]
D	.40 ± .10
E	16.51
F	$.1^{+.2}_{-.1}$
G	3.0 max
H	2.55
I	11.8 ± .3
J	8.4
K	1.7
L	$.15^{+.10}_{-.05}$
M	.7 ± .2



262 144 BIT STATIC CMOS RAM

Description

The μPD43257C is a high speed, low power, 32768 words by 8 bits static CMOS RAM fabricated with advanced silicon-gate CMOS technology. The μPD43257C is a low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD43257C a high speed and low operating power device which requires no clock or refreshing to operate.
Two chip enable inputs ($\overline{CE}_1$, CE_2) are provided for battery back-up application.
Data retention is guaranteed at a power supply voltage as low as 2 volts. (μPD43257C-10L/12L/15L)
The μPD43257C is packaged in a standard 28-pin dual-in-line plastic package.

Features

: Single + 5V Supply
: Fully Static Operation – No Clock or Refreshing required
: TTL Compatible – All Inputs and Outputs
: Common I/O Using Three-State Output
: Two Chip Enable Inputs for Battery Back-Up Application
: Fast Access Time

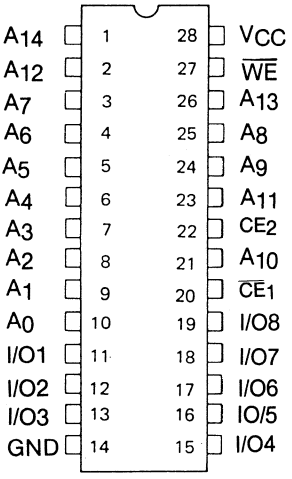
	μPD43257C-10L	100ns max
	μPD43257C-12L	20ns max
	μPD43257C-15L	150ns max

: Low Power Dissipation

Active		70ns max
Standby	μPD43257C-10L/12L/15L	100μA max

: Data Retention Voltage – 2V min (μPD43257C-10L/12L/15L)
: Standard 28-pin Plastic Package

Pin Configuration and Function

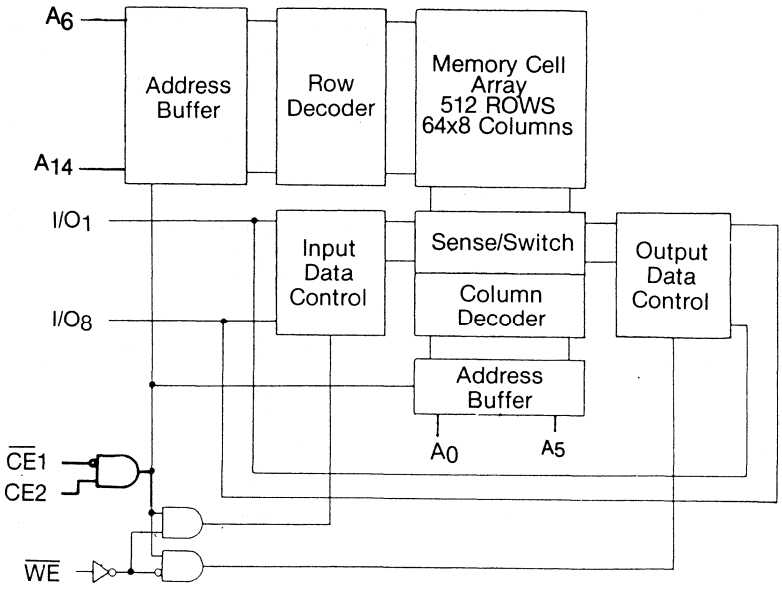


A_0-A_{14}	Address Inputs
$\overline{I/O}1$-I/O8	Data-Input/Output
$\overline{CE}_1$	Chip Enable Active Low
$\overline{CE}_2$	Chip Enable Active High
$\overline{WE}$	Write Enable
V_{CC}	Power (+ 5V)
GND	GND

Truth Table

$\overline{CE1}$	CE2	$\overline{WE}$	Mode	I/O	ICC
H	X	X	Not selected	HZ	Standby
X	L	X	Not selected	HZ	Standby
L	H	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	−0.5* to 7.0	V
Input Voltage	V_{IN}	−0.5* to $V_{CC}+0.5$	V
Output Voltage	V_{out}	−0.5* to $V_{CC}+0.5$	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	−55 to 125	°C
Power Dissipation	Pd	1.0	W

Recomended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3*		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.5$	V

*−3.0V min (Pulse Width 50ns)

DC Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim V_{CC}$			1	μA
I/O Leakage Current	I_{LO}	$V_{I/O} = 0 \sim V_{CC}$, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$			1	μA
Operating Supply Current	I_{CCA}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, Min. Cycle $I_{I/O} = 0$		1)	70	mA
Standby Supply Current	I_{SB}	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$			2)	mA
Standby Supply Current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$		3)	3)	μA
Standby Supply Current	I_{SB2}	$CE2 \leq 0.2V$		3)	3)	μA
Output Low Voltage	V_{OL}	$I_{OL} = 2.1$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1.0$ mA	2.4			V

Notes
[1]
μPD43257C-10L 35mA Typ
μPD43257C-12L 30mA Typ
μPD43257C-15L 25mA Typ

[2]
μPD43257C-10L/12L/15L 3mA max

[3]
μPD43257C-10L/12L/15L (3 μA typ) 100μA max

Capacitance Ta = 25 °C f = 1MHz) (1)

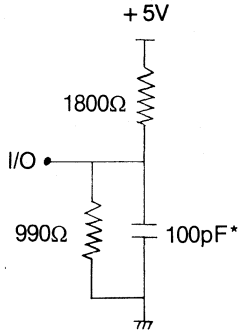
Parameter	Symbol	Conditions	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	7	pF
Data-Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	10	pF

Note (1) This parameter is sampled and not 100% tested.

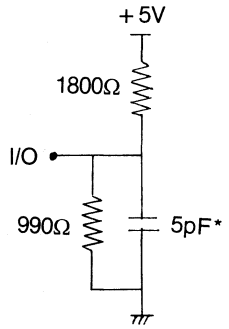
Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Pulse Rise and fall Time	5ns
Timing Reference Levels	1.5V

Output Load



for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}



*including scope and jig.

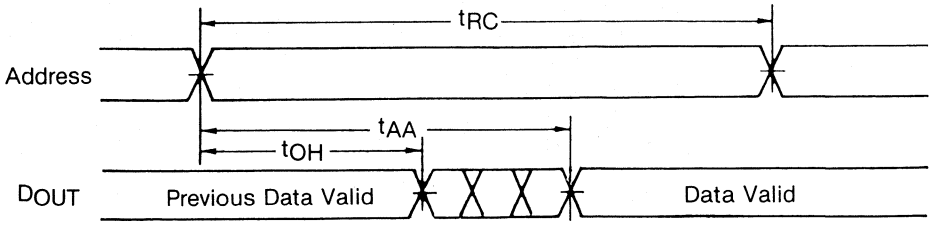
AC Characteristics ($T_a = 0$ to 70°C $V_{CC} = 5V \pm 10\%$)

Read Cycle

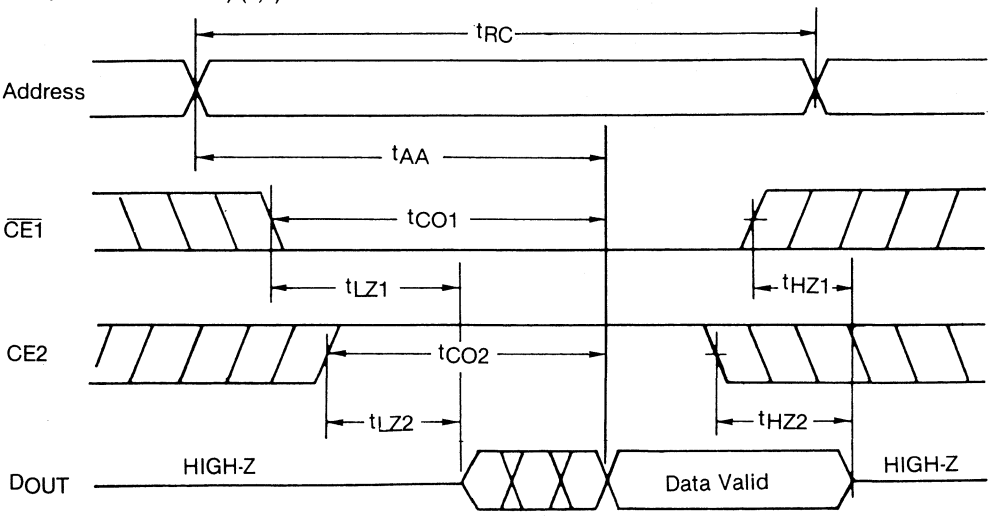
Parameter	Symbol	μPD43257C 10L		μPD43257C 12L		μPD43257C 15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
$\overline{CE}_1$ Access Time	t_{001}		100		120		150	ns
$\overline{CE}_2$ Access Time	t_{002}		100		120		150	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Enable $(\overline{CE})_1$ to Output in LZ	t_{LZ1}	10		10		10		ns
Chip Enable (CE_2) to Output in LZ	t_{LZ2}	10		10		10		ns
Chip Enable ($\overline{CE}_1$) to Output in HZ	t_{HZ1}		35		40		50	ns
Chip Enable (CE_2) to Output in HZ	t_{HZ2}		35		40		50	ns

Read Cycle Timing Chart

Read Cycle No. 1 (Address Access) (1) (2)



Read Cycle No. 2
(Chip Enable Access) (1,3)



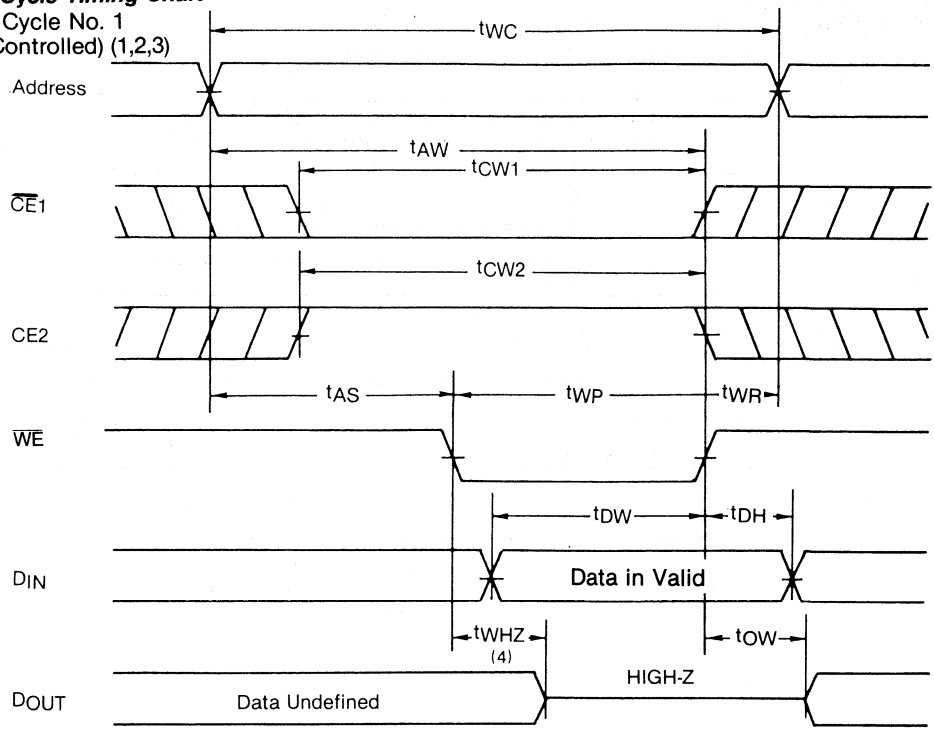
Notes: 1) $\overline{WE}$ is high for read cycle.
2) Device is continuously selected, $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$
3) Address valid prior to or coincident with $\overline{CE1}$ transition low, CE2 transition high.

Write Cycle

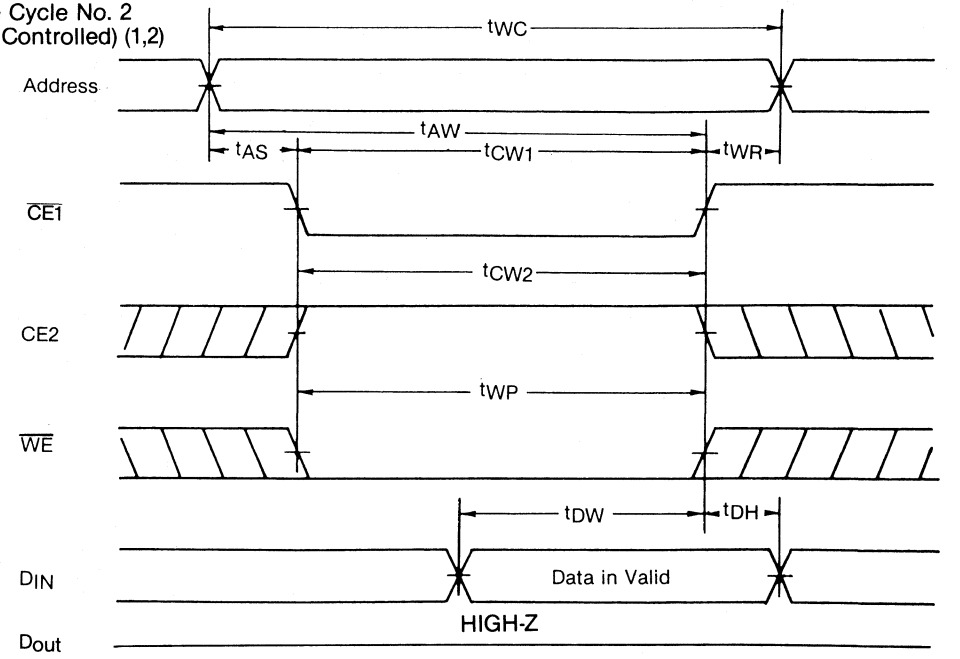
Parameter	Symbol	μPD43257C 10L		μPD43257C 12L		μPD43257C 15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100		120		150		ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	85		100		120		ns
Chip Enable (CE_2) to End of Write	t_{CW2}	85		100		120		ns
Address Valid to End of Write	t_{AW}	85		100		120		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	75		85		105		ns
Write Recovery Time	t_{WR}	10		10		10		ns
Data Valid to End of Write	t_{DW}	45		50		60		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		35		40		50	ns
Output Active from End of Write	t_{OW}	10		10		10		ns

Write Cycle Timing Chart

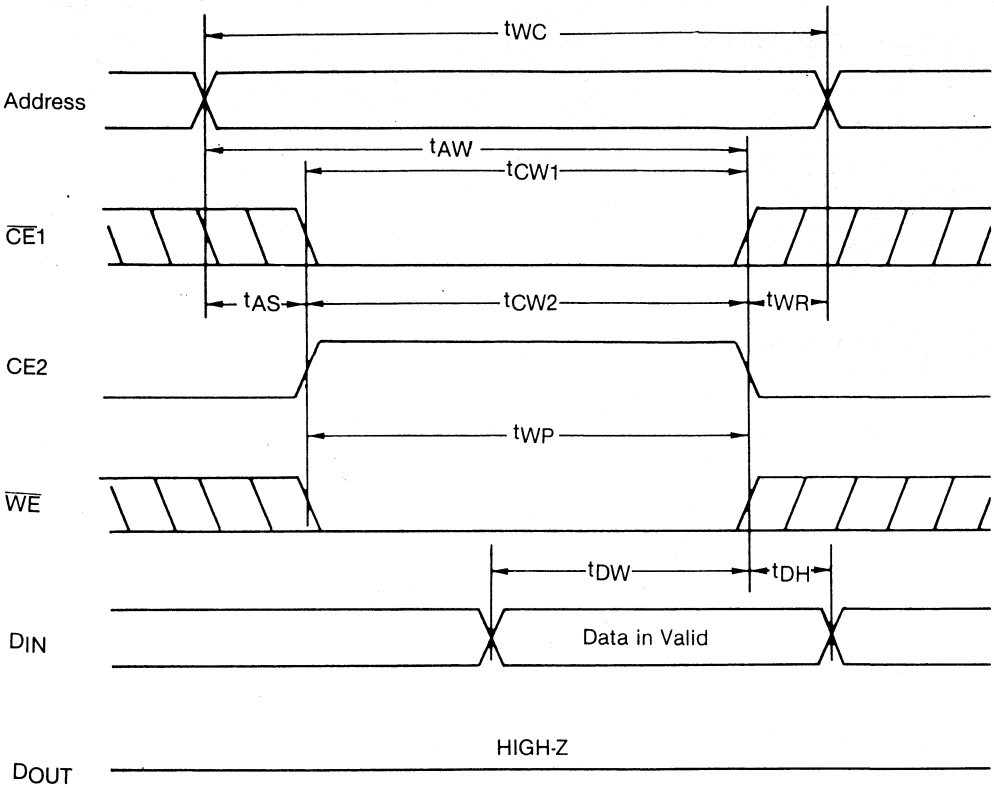
Write Cycle No. 1
($\overline{WE}$ Controlled) (1,2,3)



Write Cycle No. 2
($\overline{CE1}$ Controlled) (1,2)



Write Cycle No. 3
(CE2 Controlled) (1,2)



Notes: 1) A write occurs during the overlap of a low $\overline{CE}1$ and a high CE2 and a low $\overline{WE}$.
2) $\overline{CE}1$ or $\overline{WE}$ (or CE2) must be high (low) during address transition.
3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

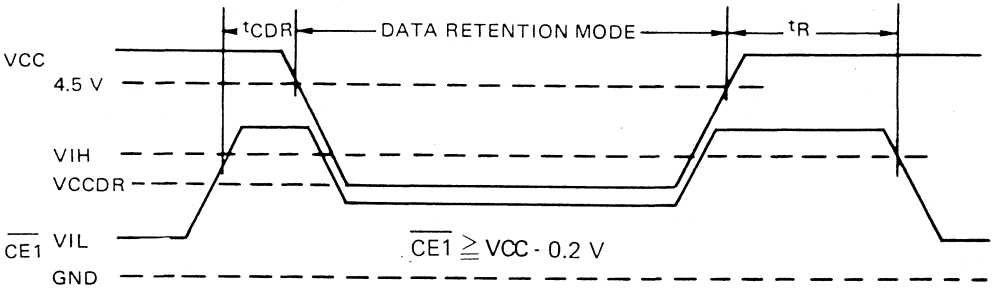
Low V_{CC} Data Retention Characteristics (Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Data Retention Supply Voltage	V_{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $CE2 \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Supply Voltage	V_{CCDR2}	CE2 = 0.2V	2.0		5.5	V
Data Retention Supply Current	I_{CCDR1}	$V_{CC} = 3.0V$ $CE1 = V_{CC} - 0.2V$ $CE2 = V_{CC} - 0.2V$		1	50	μA
Data Retention Supply Current	I_{CCDR2}	$V_{CC} = 3.0V$ CE2 = 0.2V		1	50	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

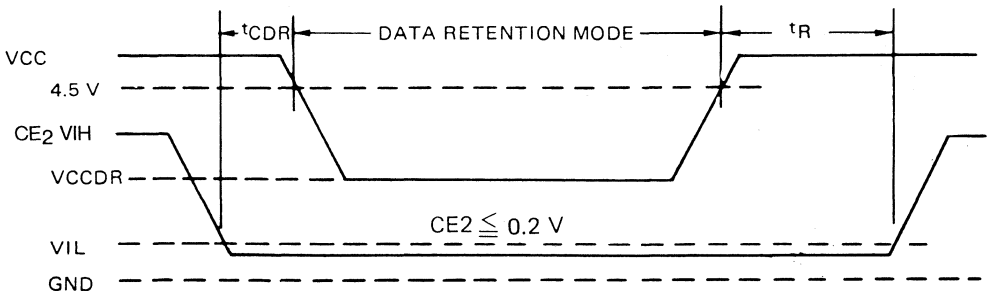
*5μA Max. (Ta = 0 to 40°C)

Data Retention Timing Chart

($\overline{CE}$1 Controlled) (1)



CE_2 Controlled (2)

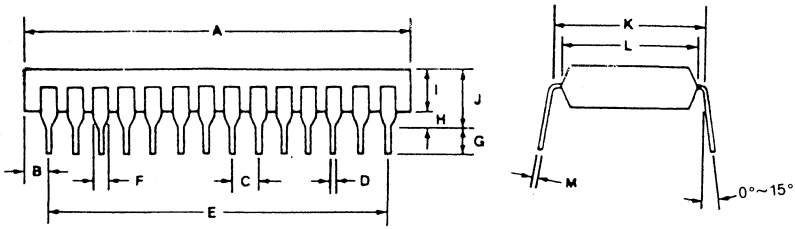


Notes: 1) CE2 must be equal to or higher than V_{CC}-0.2V or $CE_2 \leq 0.2V$. The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.
2) The inputs (Addresses, $\overline{CE}$1, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

Package Dimensions

28 PIN Plastic DIP (600 mil)
μPD43257C

Item	Millimeters
A	38.0 max
B	2.49
C	2.54
D	0.5 ± 0.1
E	33.02
F	1.5
G	2.54 min
H	0.5 min
I	4.31 max
J	5.72 max
K	15.24
L	13.2
M	$0.25^{+0.01}_{-0.05}$



8192 X 8 Bit Pseudo Static RAM

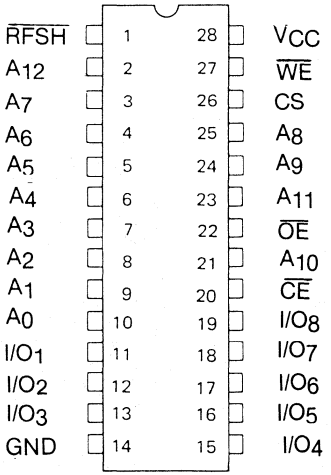
Description

The μPD4168C is a high performance 8192 words x 8 bits pseudo static RAM which uses a combination of dynamic storage cells with static Input/Output circuitry to achieve high speed and low power in the same device. By integrating the refresh control circuitry on the chip, the pin one refresh becomes available without refresh interface.

Features

- 8192 x 8 bits organization
- Single + 5V ±10% power supply
- On chip substrate bias generator
- Access time 120 ns, 150 ns, 200 ns
- Cycle time 220 ns, 260 ns, 330 ns
- Low power dissipation
  Active 358 mW, 330 mW, 303 mW
  Standby 28 mW
- All pins TTL compatible
- 128 Refresh cycles / 2 ms
- 28-pin ROM/PROM compatible package
- Built-in refresh multiplexer and refresh address counter
- Power down self refresh mode
- Automatic precharge allows cycle time to be independent of system skews
- Latched address and CS function along with OE function allows use on multiplexed address / data buses
- Available cycles types:
  Memory Cycle - Read, Early Write, Late Write
  Refresh Cycle - External Refresh
  Pulse Refresh
  Self Refresh

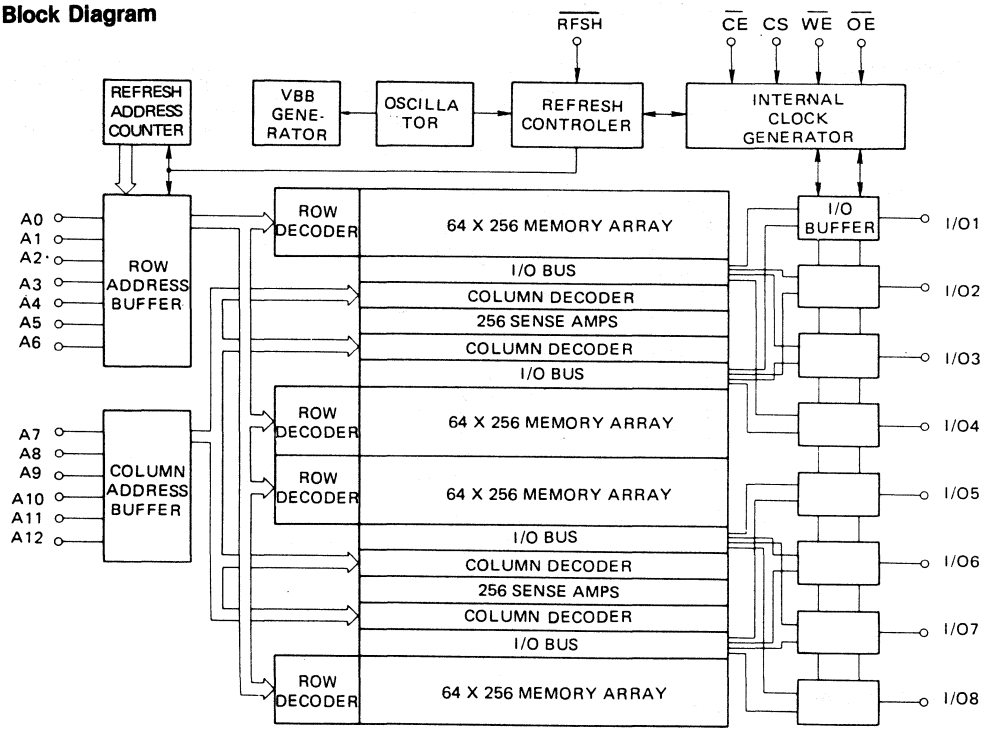
Pin Configuration



Pin Names

$\overline{RFSH}$	Internal Refresh
A_0 - A_{12}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Block Diagram



Address inputs (A0-A12) ..... The μPD4168C requires 13 address inputs to select a particular word of data from its 8,192 words. Because these address inputs are internally read onto the chip at the trailing edge of a $\overline{CE}$ clock pulse, they have their address setup time and hold time (t_{ACS}, t_{AHC}) prescribed for the $\overline{CE}$ clock. External refresh perform by low-order address inputs A0-A6.

Data inputs/outputs (I/O1-I/O8) ..... With common I/O pins, the μPD4168C requires data control by $\overline{WE}$ and $\overline{OE}$ inputs. Data I/O has its data setup time and hold time (t_{DSC}, T_{DHC}, t_{DSW}, t_{DHW}) prescribed for the $\overline{CE}$ clock and the $\overline{WE}$ input during a memory write cycle and access time (t_{OEA}) prescribed for the $\overline{OE}$ input during a read cycle.

Chip enable input ($\overline{CE}$) ..... Chip enable clock used to initiate a read/write cycle or external refresh cycle. It causes addresses, CS, and data inputs (only during an early cycle) to be internally resd onto the chip.

Chip select input (CS) ..... The μPD4168C can perform read/write operations only if the CS input is active high when the $\overline{CE}$ clock is enabled. If the CS input is latched nonactive (low) at this time, I/O1-I/O8 remain in the high-impedance state, regardless of the status of the $\overline{WE}$ and $\overline{OE}$ inputs.

Write enable input ($\overline{WE}$) ..... Read/write operation control input. Two types of write cycles are provided according to $\overline{WE}$ input timing: early write and late write.

Output enable input ($\overline{OE}$) ..... I/O1-I/O8 output timing control input. The μPD4168C has its access time (t_{CEA}, t_{OEA}) from either $\overline{CE}$ clock or $\overline{OE}$ input prescribed according to $\overline{OE}$ input timing.

Refresh input ($\overline{RFSH}$) ..... Built-in refresh control circuit enables input. Two refresh modes are provided: pulse refresh using the $\overline{RFSH}$ input as a clock input, and power-down self-refresh using the $\overline{RFSH}$ input as a logical level input. It is nonactive (high) during usual read/write cycles.

Function Mode

Mode	$\overline{RFSH}$	$\overline{CE}$	CS	$\overline{WE}$	$\overline{OE}$	I/O	Remark
Read cycle	H	↓	H	H	L	Data-out	OE: logic level or clock pulse
Write cycle	H	↓	H	L	H	Data-in	Early write cycle
	H	↓	H	↓	H		Late write cycle
External refresh cycle	H	↓	H	H	H	High impedance	
	H	↓	L	X	X		Standby
Pulse refresh cycle	↓	H	X	X	X		
	↓	↓	H	H	H		After external Refresh cycle
	↓	↓	H	H	L	*	After read cycle
	↓	↓	H	L	H	Data-in	After early write cycle
	↓	↓	H	↓	H		After late write cycle
Power-down self-refresh cycle	L	H	X	X	X	High impedance	
Standby	H	H	X	X	X		

↓ = clock pulse (negative edge)
H = V_{IH} level, L = V_{IL} level, X = V_{IH} or V_{IL} level
* = depend on previous cycle

Absolute Maximum Ratings

Voltage on V_{DD} relative to V_{SS}	−1.0V to 7.0V
Storage Temp. (Plastic Package)	−55°C to + 125°C
Operating Temp.	0 to + 70°C
Power Dissipation	1 W
Short Circuit Output Current	50mA

DC Operating Condition

Symbol	Parameter	Min.	Typ	Max.	Units
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Logic "I" Voltage	2.4		5.5	V
V_{TL}	Logic "I" Voltage	−1.0		0.8	V
T_A	Ambient Operating Temperature	0		70	°C

DC electrical Characteristic

(0°C≤Ta≤70°C, V_{CC} = 5.0V±10%)

Parameter	Symbol	Min.	Typ	Max.	Units	Test Condition
Supply Voltage	VCC	4.5	5.0	5.5	V	All Voltages Referenced to GND
High Level Input Voltage	VIH	2.4		5.5	V	
Low level Input Voltage	VIL	−1.0		0.8	V	
Average VCC Power Supply Current (Active)	ICC1			65 60 55	mA mA mA	TC = 220ns TC = 260ns TC = 330ns
Standby Current	ICC2			5	mA	$\overline{CE}$≥VIH (min.) $\overline{RFSH}$≥VIH (min.)
Self Refresh Average Current	ICC3			3.5	mA	$\overline{RFSH}$≤VIL (max.)
Input Leakage Current	II(L)	−10		10	μA	0V≤VI≤5.5V Others = 0V
Output Leakage Current	IO(L)	−10		10	μA	0V≤V0≤5.5V Dout = HIZ
Output Low Voltage	VOL	0		0.4	V	IOL = 2mA
Output High Voltage	VOH	2.4		VCC	V	IOH = 1mA

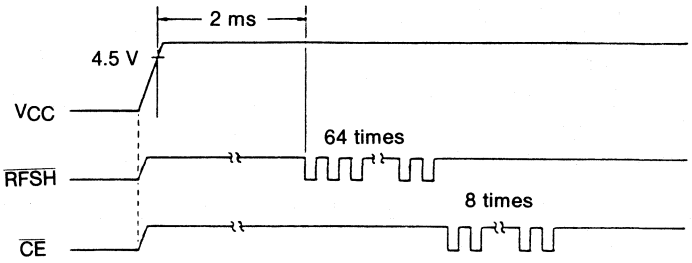
Capacitance (V_{CC} = 5.0V±10%, 0°C≥Ta≥70°C)

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
$C_{I/C}$	Data in, Data out			10	pF	—
C_I	Input			10	pF	—

AC Characteristics ($T_a = 0°\sim70°C$, $V_{CC} = 5V \pm 10\%$)

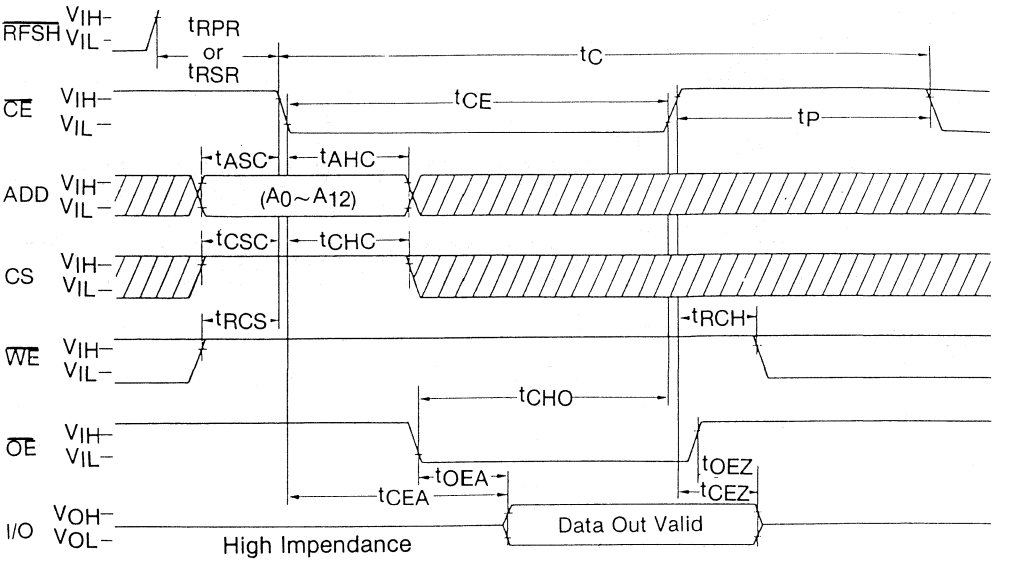
Symbol	Parameter	μPD4168C-12		μPD4186C-15		μPD4168C-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	$t_C = t_C$(Min.)		65		60		55	mA
t_C	Read Write or Refresh Cycle Time	220		260		330		ns
t_{CEA}	Access Time from $\overline{CE}$		120		150		200	ns
t_{CEZ}	Data off Time from $\overline{CE}$		30		35		45	ns
t_{OEA}	Access Time from $\overline{OE}$		45		55		70	ns
t_{OEZ}	Dato of Time from $\overline{OE}$		30		35		45	ns
t_{CE}	$\overline{CE}$ Pulse Width	120	10000	150	10000	200	10000	ns
t_P	$\overline{CE}$ Precharge Time	90		100		120		ns
t_{ASC}	Address to $\overline{CE}$ Set-up Time	0		0		0		ns
t_{AHC}	Address from $\overline{CE}$ Hold Time	35		45		55		ns
t_{CSC}	CS to $\overline{CE}$ Set-up Time	0		0		0		ns
t_{CHC}	CS from $\overline{CE}$ Hold Time	35		45		55		ns
t_{DSC}	Data to $\overline{CE}$ Set-up Time for Early Write Cycle	−10		−10		−10		ns
t_{DHC}	Data from $\overline{CE}$ Hold Time for Early Write Cycle	90		100		120		ns
t_{DSW}	Data to $\overline{WE}$ Set-up Time for Late Write Cycle	0		0		0		ns
t_{DHW}	Data from $\overline{WE}$ Hold Time for Late Write Cycle	50		60		70		ns
t_{WSC}	$\overline{WE}$ to $\overline{CE}$ Set-up Time for Early Write Cycle	−30		−30		−30		ns
t_{WHC}	$\overline{WE}$ from $\overline{CE}$ Hold Time for Early Write Cycle	90		100		125		ns
t_{WD}	$\overline{WE}$ Pulse Duration	60		70		90		ns
t_{CHW}	$\overline{CE}$ from $\overline{WE}$ Hold Time for Late Write Cycle	90		105		135		ns
t_{RCS}	$\overline{WE}$ to $\overline{CE}$ Set-up Time for Read Cycle	0		0		0		ns
t_{RCH}	$\overline{WE}$ from $\overline{CE}$ Hold Time for Read Cycle	0		0		0		ns
t_{CHO}	$\overline{CE}$ from $\overline{OE}$ Hold Time for Read Cycle	45		55		70		ns
t_{OES}	$\overline{OE}$ to $\overline{CE}$ Set-up Time for Write Cycle	0		0		0		ns
t_{OEH}	$\overline{OE}$ from $\overline{CE}$ Hold Time for Write Cycle	0		0		0		ns
t_{CRD}	$\overline{CE}$ to $\overline{RFSH}$ Delay for Pulse Refresh Cycle	50		65		80		ns
t_{RDP}	$\overline{RFSH}$ Pulse Width for Pulse Refresh Cycle	50	4000	65	4000	80	4000	ns
t_{RPR}	$\overline{RFSH}$ Recovery Time for Pulse Refresh Cycle	90		100		120		ns
t_{RDS}	$\overline{RFSH}$ Pulse Width for Self Refresh Cycle	40		40		20		μS
t_{RSR}	$\overline{RFSH}$ Recovery Time for Self Refresh Cycle	2		2		2		μS
t_{CSH}	$\overline{CE}$ from $\overline{RFSH}$ Hold Time for Self Refresh Cycle	40		40		40		μS
t_{CSS}	$\overline{CE}$ to $\overline{RFSH}$ Set-up Time for Self Refresh Cycle	35		40		50		ns
t_T	Transition Time (Rise and Fall)	3	50	3	60	3	80	ns
t_{REF}	Refresh Period		2		2		2	ms
t_{RP}	$\overline{RFSH}$ Precharge Time	90		100		120		ns
t_{OEL}	$\overline{OE}$ Leadtime to Refresh Cycle	170		210		260		ns
t_{WEL}	$\overline{WE}$ Lead Time to Refresh Cycle	170		210		260		ns

Notes: 1. All voltages referenced to GND (=0V)
2. An initial pause of 2 ms is required after Power-up followed by any 8 $\overline{CE}$ cycles and 64 $\overline{RFSH}$ cycles before proper device operation is achieved.
Read cycle, Write cycle, and External Refresh cycle can be available for initialization as $\overline{CE}$ dummy cycle.
Refresh dummy cycle of 64 times can be performed before or after $\overline{CE}$ dummy cycle of 8 times.
Both dummy cycles have to keep the condition of AC parameters.

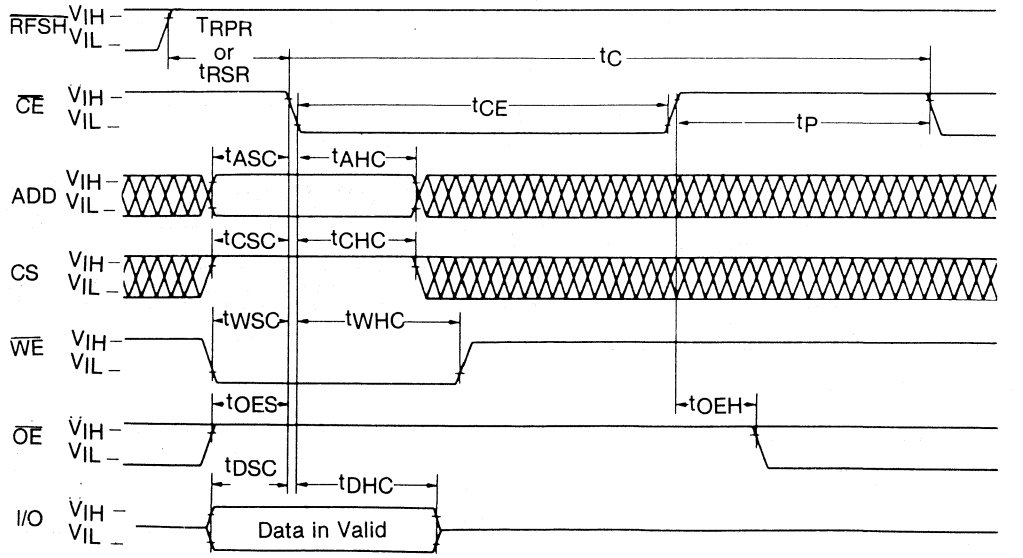


3. AC measurements assume $t_T = 5$ ns.
4. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. Load = 2TTL loads and 50 pF.
6. t_{CEZ}(max), t_{OEZ}(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. If $t_{WSC} \leqq t_{WSC}$(min), the cycle is late write cycle.
8. Power down Self Refresh cycle is initiated when the $\overline{RFSH}$ input is active low for a period of 40 μs.
(Refresh interval is about 15.6 μs.)

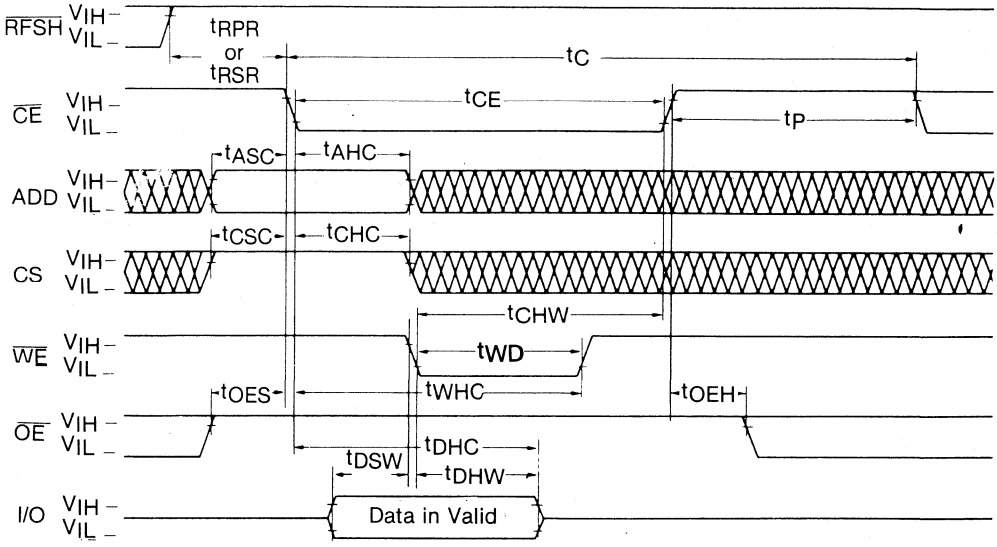
Read Cycle



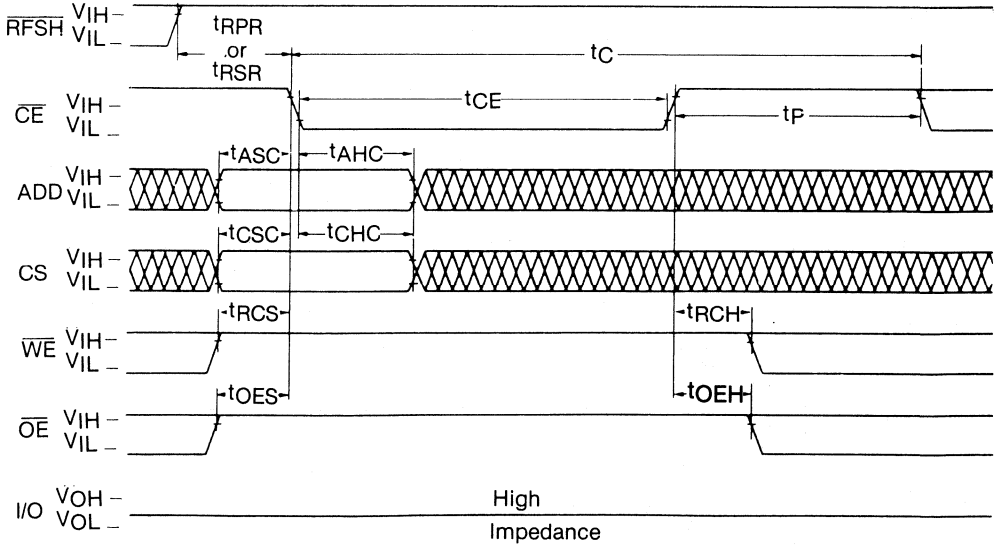
Early Write Cycle



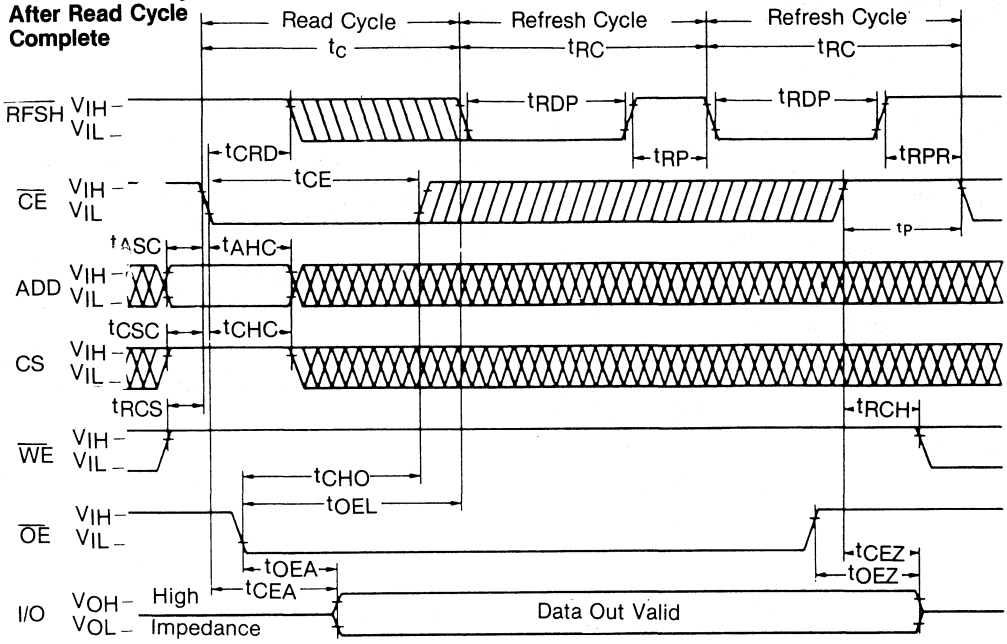
Late Write Cycle



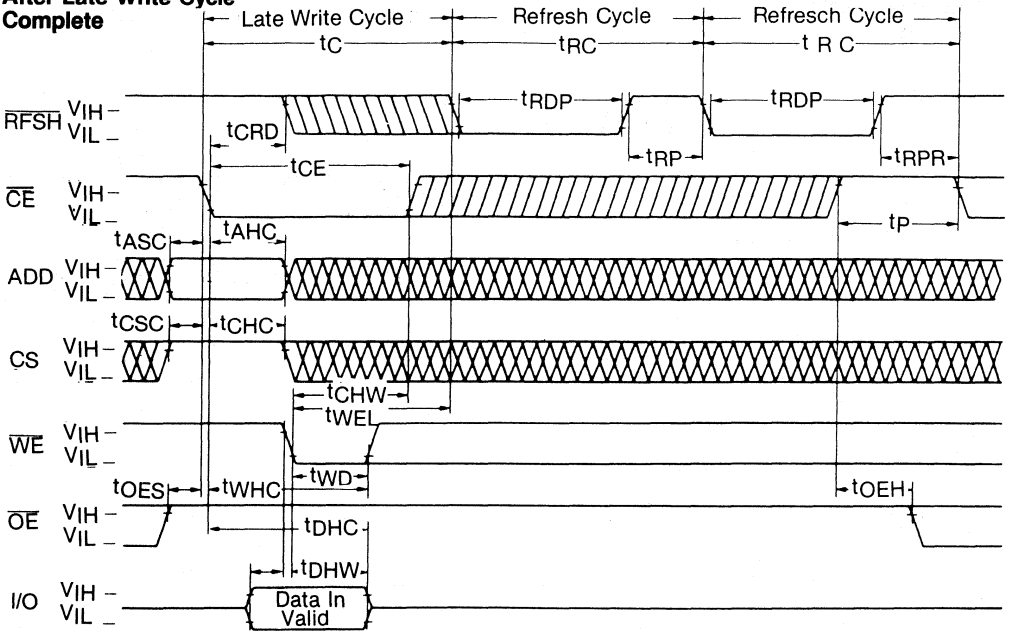
External Refresh Cycle



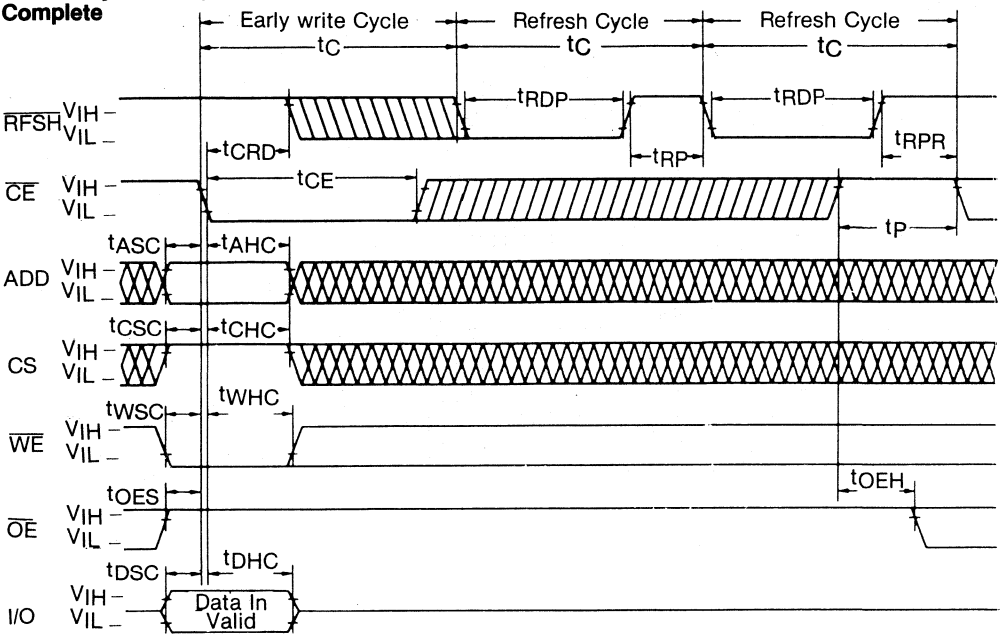
Pulse Refresh Cycle After Read Cycle Complete



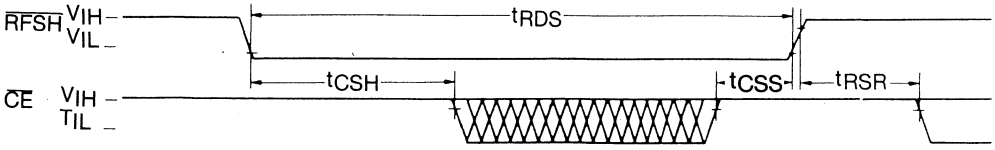
Pulse Refresh Cycle
After Late Write Cycle
Complete



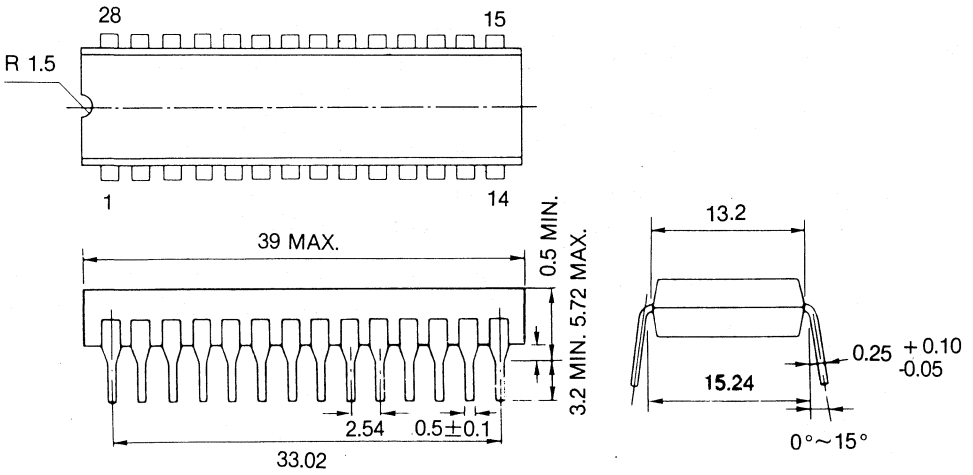
Pulse Refresh Cycle After Early Write Cycle Complete



Power Down Self Refresh



Package Dimensions
(Unit: mm)
Plastic



MOS PROMs AND ROMs

— NMOS —

131.072 (16 K x 8) BIT UV ERASABLE PROM

Description

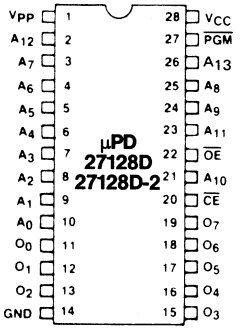
The μPD27128D is a 131,072-bit (16,384 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single + 5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.

A distinctive feature of the μPD27128D is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD27128D features fast, simple one-pulse programming controlled by TTL-level signals as well as high-speed programming mode. Total programming time for all 131,072 bits is 820 seconds for conventional mode and typically 120 seconds for high-speed mode.

Features

- Ultraviolet erasable and electrically programmable
- Access time
  - 250 ns (max) μPD27128D
  - 200 ns (max) μPD27128D-2
- Single location progamming
- Programmable with single pulse
- Low power dissipation: 100 mA max active current,
  25 mA max standby current
- High-speed programming mode (typical program time 120 s)
- Programmable with single pulse (total program time 820 s)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin Ceramic DIP
- Three-State outputs

Pin Configuration



Package D

PIN NAMES

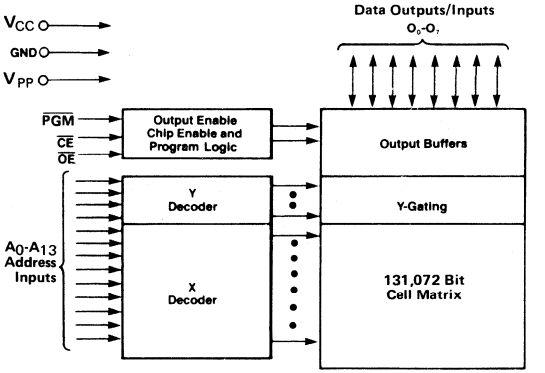
A_0-A_{13}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs/Inputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11 - 13, 15 - 19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
High-speed programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}

X can be either V_{IL} or V_{IH}

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings * (T_a = 25°C)

Operating Temperature . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Output Voltage . . . . . −0.6 to + 6.5 V
Input Voltage . . . . . −0.6 to + 6.5 V
Supply Voltage V_{CC} . . . . . −0.6 to + 6.5 V
Supply Voltage V_{PP} . . . . . −0.6 to +22 V

* COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		12	14	pF	V_{OUT} = 0V

DC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 5 %

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current		I_{LI1}			10	μA	V_{IN} = 5.25V
V_{PP} Current		I_{PP1}			15	mA	V_{PP} = 5.25V
V_{CC} Current	Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
	Active	I_{CC2}		60	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}

DC CHARACTERISTICS (CONT.)

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C, V_{CC} = +5V ± 5 % ①, V_{PP} = +21V ± 0.5V ②

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Input Leakage Current		I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	Program Inhibit	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current	Program Verify	I_{CC2}			100	mA	
V_{PP} Current	Program	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL}
V_{PP} Current	Program Verify	I_{PP3}			15	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
V_{PP} Current	Program Inhibit	I_{PP4}			15	mA	$\overline{CE}$ = V_{IH}

① V_{CC} = 6V ± 5 % for high-speed programming mode

② V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

READ MODE AND STANDBY MODE

T_a = 0°C to +70°C; V_{CC} = +5V ± 5 %

PARAMETER	SYMBOL	μPD27128D LIMITS MIN	TYP	MAX	μPD27128D-2 LIMITS MIN	TYP	MAX	UNIT	TEST CONDITITIONS
Address to Output Delay	t_{ACC}			250			200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}			250			200	ns	$\overline{OE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}			100			75	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Float	t_{DF}	0		85	0		60	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0			0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Test Conditions –

Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 to 2.4 V

Timing Measurement Reference Level:
Inputs: 0.8V and 2.0V
Outputs: 0.8V and 2.0V

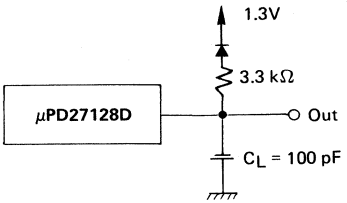
CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5 %; V_{PP} = +21V ± 0.5V

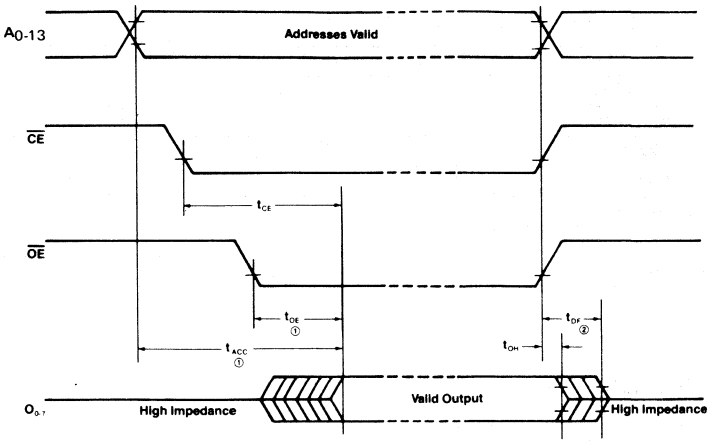
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width	t_{PW}	45	50	55	ms	
Vpp Setup Time	t_{VS}	2			μs	

Test Conditions –

Input Pulse Levels = 0.45 to 2.4V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20 ns



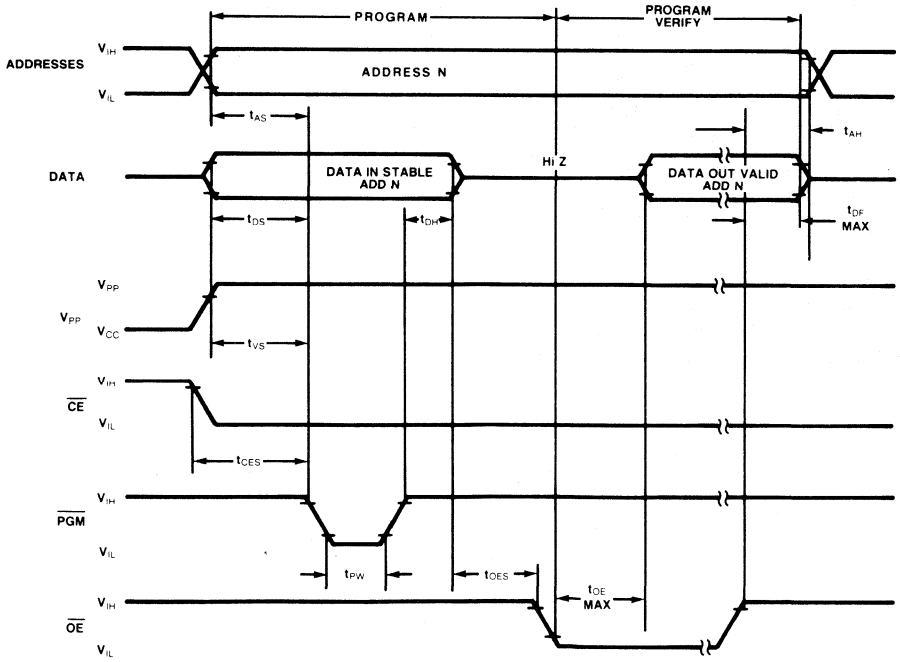
READ MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

CONVENTIONAL PROGRAM MODE



DC Characteristics

HIGH-SPEED PROGRAMMING MODE

(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1		0.8	V
Input Leakage Current	I_{LI}	$V_{IH} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	I_{OH} = –400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				100	mA
V_{PP} Current	I_{PP}	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC Characteristics

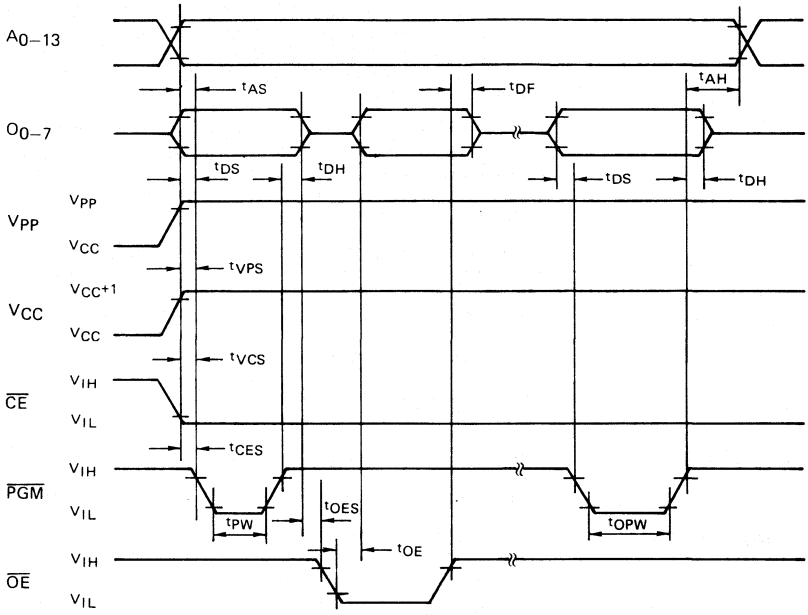
(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	t_{AS}		2			μs
$\overline{OE}$ Setup Time	t_{OES}		2			μs
Data Setup Time	t_{DS}		2			μs
Address Hold Time	t_{AH}		0			μs
Data Hold Time	t_{DH}		2			μs
$\overline{CE}$ to Ouput Float Time	t_{DF}		0		130	ns
V_{PP} Setup Time	t_{VPS}		2			μs
V_{CC} Setup Time	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{OPW}		3.8		63	ms
$\overline{CE}$ Setup Time	t_{CES}		2			μs
Data Valid from $\overline{OE}$	t_{OE}				150	ns

TEST CONDITIONS

- Input Pulse Levels: 0.45V and 2.0V
- Input Timing Reference Level: 0.8V and 2.0V
- Output Timing Reference Level: 0.8V and 2.0V

High-speed Program Mode (3)



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

(3) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Function

The μPD27128D operates from a single +5V power supply, making it ideal for microprocessor applications.

Erasure of the μPD27128D programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27128D. Consequently, if the μPD27128D is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD27128D is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm^2 power rating.

During erasure, the μPD27128D should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The six operation modes of the μPD27128D are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for V_{PP} which is pulsed from TTL level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD27128D is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced.

Programming Modes

The μPD27128D can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventionel mode basically a 50 ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm™, in which up to fifteen 1 ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4 ms $\overline{PGM}$ pulse for each number of 1 ms pulse applied before. The high-speed programming mode reduces the programming time to 120 s typical.

Conventional Programming Mode

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.
The μPD27128D is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8 bit in parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD27128Ds are connected in parallel, except for $\overline{CE}$, individual μPD27128Ds can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27128D to be programmed.

Programming of multiple μPD27128Ds in parallel with the same data is easily accomplished. All the like inputs are tied together and are programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-Speed Programming Mode

In this mode, programming begins by addressing the first location, and valid data appearing at the eight output pins (a low TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1 ms ± 5% is then applied in the same manner as decribed in the program mode timing diagram. The bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4 ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is applied and the bit verified. If the bit is not programmed at this stage, the device is rejected as a failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage V_{CC} and V_{PP} pins are lowered to 5V ± 5% and all bytes are then verified again for programming.

This algorithm is compatible with that of μPD2764D.

Programming Inhibit Mode

Programming multiple μPD27128Ds in parallel with different data is easier with the program Inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27128Ds may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27128D will inhibit it from being programmed.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at high (1) level.

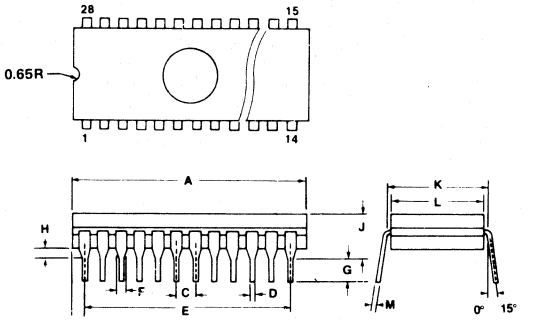
Output Disable

The data outputs of two or more μPD27128Ds may be wire-O Red together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27128Ds should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

TM: Intelligent Programming Algorithm is a registered trademark of Intel Corporation

Package Dimensions

μPD27128D (Cerdip)



Item	Millimeters
A	38.1 MAX.
C	2.54 ± 0.25
D	0.5 ± 0.10
E	33.02
F	1.3
G	2.54 MIN.
H	0.51 MIN.
J	5.08 MAX.
K	15.24
L	13.2
M	0.25 ± 0.05

262,144 (32 K X 8) BIT UV ERASABLE PROM

Features

- Ultraviolet erasable and electrically programmable
- Access time: 250 ns max (μPD27256D)
  200 ns max (μPD27256D-2)
- Single location programming
- High speed programming mode
- Low power dissipation: 100 mA (MAX) (active)
  25 mA (MAX) (standby)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-Pin DIP
- Three-state outputs
- Pin Compatible to 27C256 EPROM
- NMOS Double-Polysilicon Technology

Absolute Maximum Ratings

Operating Temperature	−10°C to + 80°C
Storage Temperature	−65°C to + 125°C
Output Voltage	−0.6 to + 6.5 V
Input Voltage	−0.6 to + 6.5 V
Supply Voltage V_{CC}	−0.6 to + 6.5 V
Supply Voltage V_{PP}	−0.6 to + 22 V

COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance *

(T_a = 25°C; f = 1 MHz)

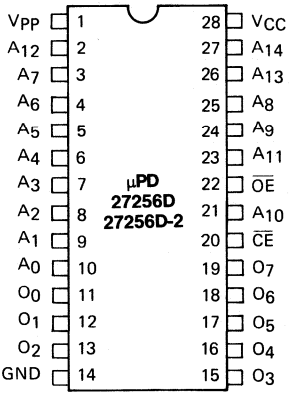
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Capacitance	C_{IN}	V_{IN} = 0V		4	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V		8	14	pF

* This parameter is periodically sampled.

Pin Configuration

(TOP VIEW)

Top View



Package D

PIN NAMES

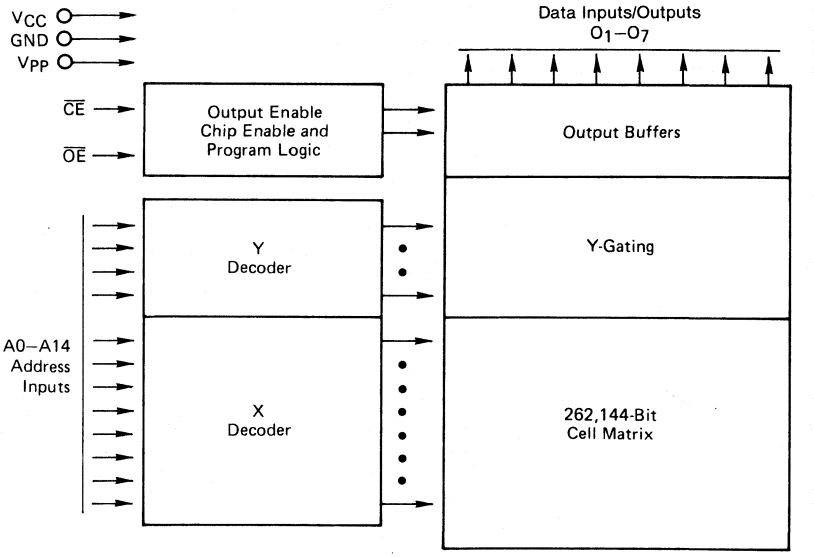
A_0–A_{14}	ADDRESSES
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE

Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Block Diagram



DC Characteristics

READ MODE AND STANDBY MODE

(T_a = 0°C to 70°C; V_{CC} = +5V ± 5 %; V_{PP} = V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output High Voltage	V_{OH}	I_{OH} = –400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Input High Voltage	V_{IH}		2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1		0.8	V
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{CC}			10	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}			10	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$ = V_{IH} Standby			25	mA
	I_{CC2}	$\overline{CE}$ = V_{IL} Active			100	mA
V_{PP} Current	I_{PP1}	V_{PP} = 5.25V			15	mA

DC Characteristics

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

(T_a = 25°C ± 5°C; V_{CC} = 6V ± 0.25V; V_{PP} = +21V ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input High Voltage	V_{IH}		2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}		−0.1		0.8	V
Input Leakage Current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	$I_{OH} = -400$ μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				100	mA
V_{PP} Current	I_{PP2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$			30	mA

AC Characteristics

READ MODE AND STANDBY MODE

(T_a = 0°C to +70°C; V_{CC} = +5V ± 5 %; $V_{PP} = V_{CC}$)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS				UNITS
			D		D-2		
			MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}	CE = OE = V_{IL}		250		200	ns
CE to Output Delay	t_{CE}	OE = V_{IL}		250		200	ns
Output Enable to Output Delay	t_{OE}	CE = V_{IL}		100		75	ns
Output Enable High to Output Float	t_{DF}	CE = V_{IL}	0	85	0	60	ns
Address to Output Hold	t_{OH}	CE = OE = V_{IL}	0		0		ns

TEST CONDITIONS

Output Load:	See Fig. 1
Input Rise and Fall Times:	20 ns
Input Pulse Levels:	0.45 to 2.4V
Timing Measurement Reference Level:	Input: 0.8V and 2.0V
	Output: 0.8V and 2.0V

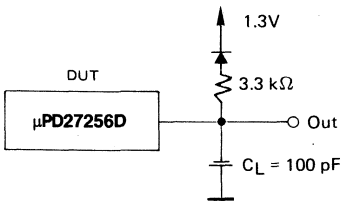
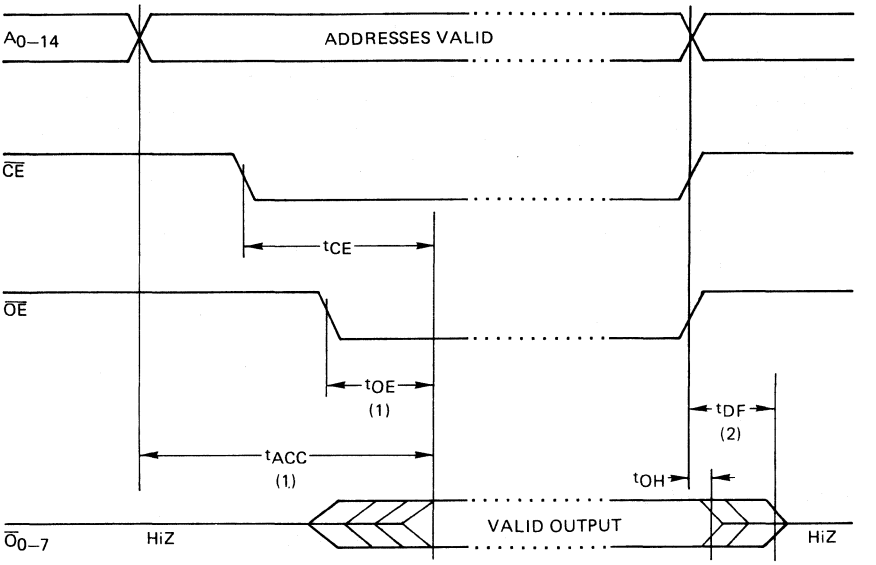


Fig. 1

READ MODE



Notes: 1 $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC Characteristics

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

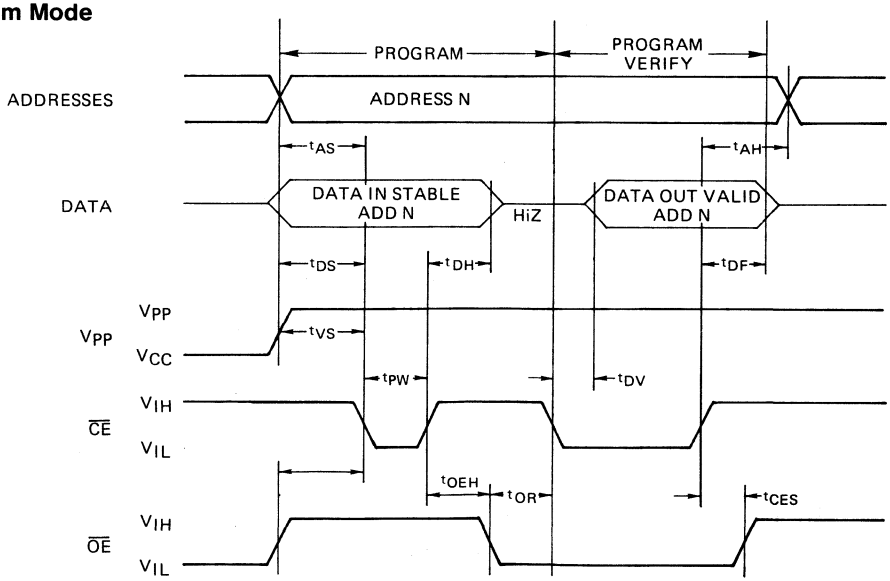
(T_a = 25°C ± 5°C; V_{CC} = +6V ± 0.25V; V_{PP} = 21V ± 0.5V)

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
Data Hold Time	t_{DH}	2			μs
Address Hold Time	t_{AH}	2			μs
Chip Enable to Output Float Delay	t_{DF}			130	ns
V_{CC} = Setup Time	t_{VS}	2			μs
Program Pulse Width	t_{PW}	0.95	1	1.05	ms
$\overline{CE}$ Setup Time	t_{CES}	2			μs
$\overline{OE}$ Setup Time	t_{OES}	2			μs
*$\overline{OE}$ Hold Time	t_{OEH}	2			μs
*$\overline{OE}$ Recovery Time	t_{OR}	2			μs
*$\overline{CE}$ to Output Valid	t_{DV}			1	μs

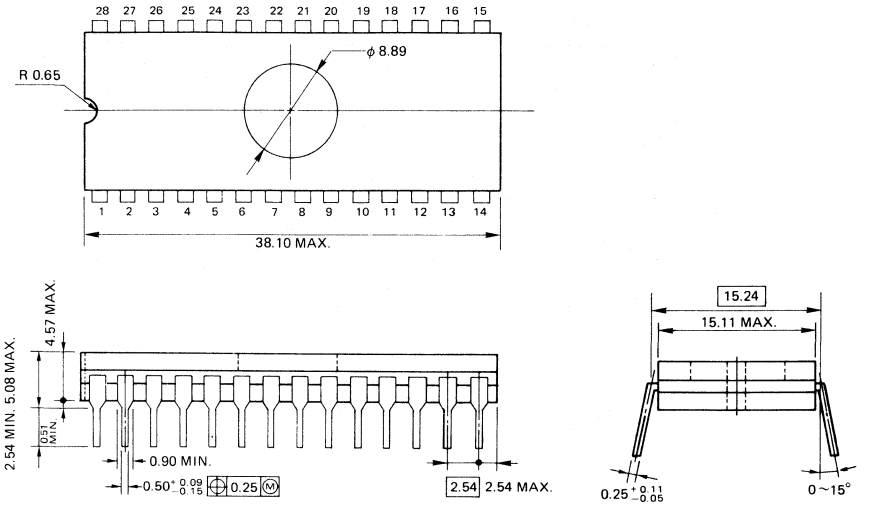
TEST CONDITION

Input Pulse Levels:	= 0.45V to 2.4V
Input Timing Reference Level:	= 0.8V and 2.0V
Output Timing Reference Level:	= 0.8V and 2.0V
Input Rise and Fall Times:	= 20 ns

Program Mode



Package Dimensions (Unit : mm)



262 144 BIT UV EPROM

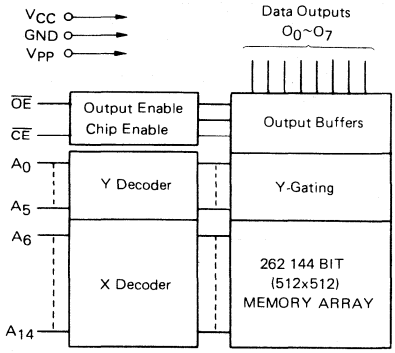
Description

The μPD27256 AD is a 262 144 bit (32 768 x 8-bit) ultraviolet erasable and electrically programmable read-only memory (UV EPROM). It operates from a single + 5 V power supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.
The μPD27256AD is available in a standard 28-pin cerdip package with a quartz window.

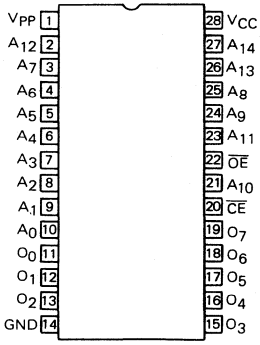
Feature

- 32 768-word by 8-bit organization
- Ultraviolet erasable and electrically programmable
- Fast access time: 200 ns MAX. (μPD2756AD-2)
  250 ns MAX. (μPD2756AD)
- Low power dissipation: 100 mA MAX. active current
  25 mA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single + 5 V power supply
- Three state outputs
- 28-pin DIP

Block Diagram



Pin Configuration



PIN NAMES

A_0 ~ A_{14}	Addresses
O_0 ~ O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
V_{PP}	Program Voltage
GND	Ground

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O_0~O_7
Read	V_{IL}	V_{IL}	+5 V	+5 V	D_{OUT}
Output Desable	V_{IL}	V_{IH}	+5 V	+5 V	High-Z
Standby	V_{IH}	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	+12,5V	+6 V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12,5V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	+12,5V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

Absolute Maximum Ratings*

Operating Temperature	−25 to +85°C
Storage Temperature	−65 to +125 °C
Output Voltage	−0.6 to +6.5 V
Input Voltage	−0.6 to +6.5 V
Supply Voltage V_{CC}	−0.6 to +6.5 V
Supply Voltage V_{PP}	−0.6 to +13.5 V

*COMMENT: Esposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Read Operation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.75	5.0	5.25	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP}=V_{CC}$			V
Input High Voltage	V_{IH}	2.0	–	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V
Operating Temperature	T_a	0	–	70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output High Voltage	V_{OH1}	2.4			V	I_{OH}=−400 μA
	V_{OH2}	V_{CC}−0.7			V	I_{OH}=−100 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL}=2.1 mA
Output Leakage Current	I_{LO}			10	μA	V_{OUT}=5.25 V
Input Leakage Current	I_{LI}			10	μA	V_{IN}=5.25 V
V_{PP} Current	I_{PP}		20	100	mA	V_{PP}=5.25 V
V_{CC} Current	I_{CC1}			25	mA	$\overline{CE}$=V_{IH}
	I_{CC2}		60	100	mA	$\overline{CE}$=$\overline{OE}$=V_{IL}

AC CHARACTERISTICS
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	μPD2756AD-2		μPD2756AD		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Address to Output Delay	t_{ACC}		200		250	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		200		250	ns	$\overline{OE}=V_{IL}$
$\overline{OE}$ to Outptut Delay	t_{OE}		75		100	ns	$\overline{CE}=V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	85	ns	$\overline{CE}=V_{IL}$
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

Test Conditions

- Output Load: See Fig. 1
- Input Rise and Fall Times≦20 ns
- Input Pulse Levels: 0.45 V and 2.4 V
- Timing Measurement Reference Level
  Input: 0.8 V and 2.0 V
  Output: 0.8 V and 2.0 V
- CL in Fig. 1 includes the floating capacitors of jig and probe.

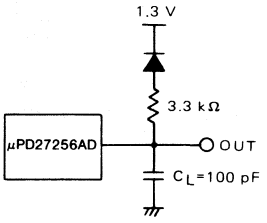
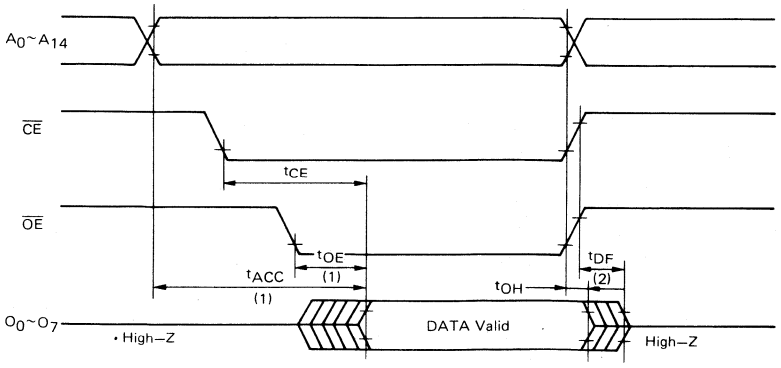


Fig. 1 Output Load

Capacitance (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	14	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Programming Operation

μPD27256AD is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27256AD is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel from at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight outputs pins. V_{CC} is then raised to +6±0.25 V followed by V_{PP} raised to +12.5±0.3 V. A $\overline{CE}$ pulse of 1 ms ± 5 % is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 25 times. If the bit gets programmed within 25 efforts, another pulse of 3 ms for each effort is applied and the next address is applied until all addresses are complete. If the bit does not get programmmed in 25 efforts, the device would be rejected as a program failure.

At this stage, V_{CC} and V_{PP} pins are lowered to +5 V ± 10 % and all bytes are then verified again for programming.

When programming multiple μPD2725AD in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel μPD2756AD may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with V_{PP} at +12.5 V. A high (1) level applied to the $\overline{CE}$ of the other μPD2756AD will inhibit it from being programmed.

DC Characteristics (T_a=25±5°C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

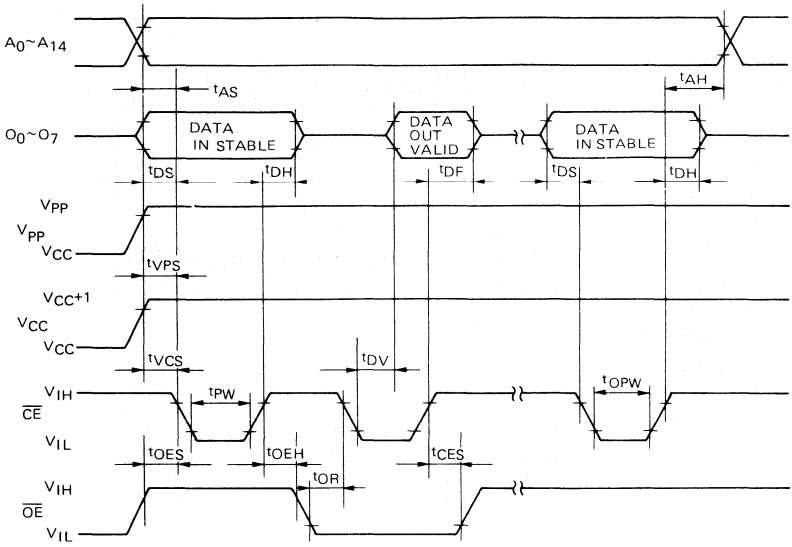
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	–0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = –400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			100	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$

AC CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
$\overline{CE}$ to Output Delay	t_{DV}			1	μs	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{OE}$ Hold Time	t_{OEH} *	2			μs	
$\overline{OE}$ Recovery Time	t_{OR} *	2			μs	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	

* $t_{OEH} + t_{OR} \geq 50$ μs

Programming Mode Timing



NOTES: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2) V_{PP} must not be greater than +13.5 V including overshoot.

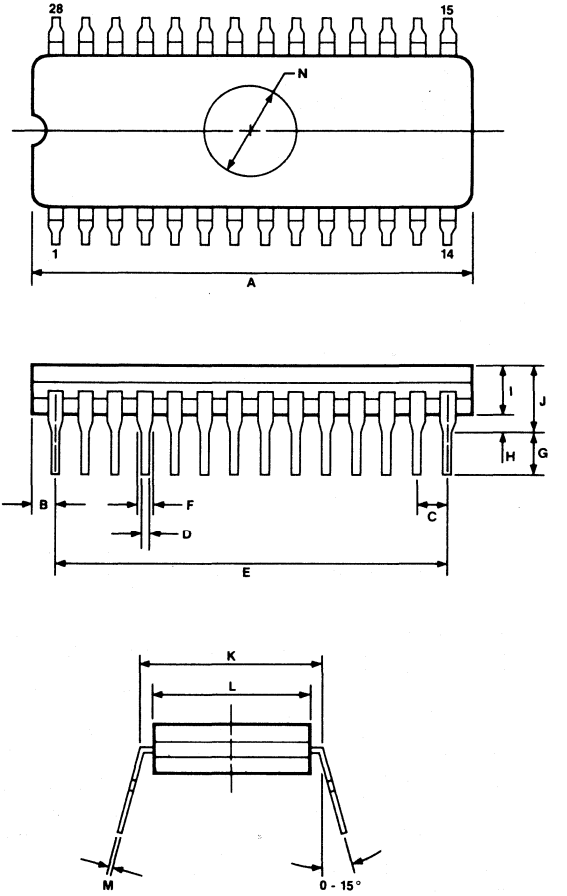
ERASURE

Easure of the μPD27256AD programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorecent lighting could erase the μPD27256AD. Consequently, if the μPD27256AD is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD27256AD is exposure to ultraviolet light with wavelengths of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12000 $\mu W/cm^2$ power rating. During erasure, the μPD27256AD should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Package Dimensions

Item	Millimeters
A	38.10 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	33.02
F	1.2 min
G	3.5 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	14.66
M	.25 ± .05
N	8.89 dia



OTPROM

— NMOS —

65,536 (8 K X 8) BIT PROM

Description

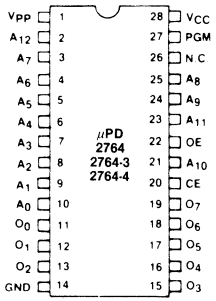
The μPD2764 is a 65,536-bit (8192 x 8 bit) Electrically Programmable Read-Only Memory (PROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 70 % savings in power consumption.

A distinctive feature of the μPD2764 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2764 features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 65,410 seconds for conventional programming mode.

Features

- Electrically programmable
- Access time
  - μPD2764 = 250 ns
  - μPD2764-3 = 300 ns
  - μPD2764-4 = 450 ns
- Single location programming
- Programmable with single pulse
- Low power dissipation: 80 mA max active current,
  25 mA max standby current
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin plastic DIP
- Three-state outputs

Pin Configuration



Package C

PIN NAMES

A_0-A_{12}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs/Inputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
N. C.	No Connect

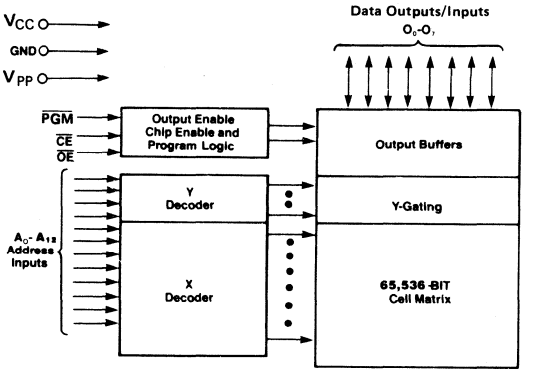
Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	V_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
High-Speed Programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}

X can be either V_{IL} or V_{IH}

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings* (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−55°C to +125°C
Output Voltage	−0.6 to +6.5 V
Input Voltage	−0.6 to +6.5 V
Supply Voltage V_{CC}	−0.6 to +6.5 V
Supply Voltage V_{PP}	−0.6 to +22 V

* COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

DC Characteristics

READ MODE AND STANDBY MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 5 %

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current		I_{LI1}			10	μA	V_{IN} = 5.25V
V_{PP} Current		I_{PP1}			15	mA	V_{PP} = 5.25V
V_{CC} Current	Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IN}
	Active	I_{CC2}		50	80	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (CONT.)

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{PP} = +21V ± 0.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC2}			100	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL}

AC Characteristics

READ MODE AND STANDBY MODE

T_a = 0°C to +70°C; V_{CC} = +5V ± 5 %

PARAMETER	SYMBOL	μPD2764 LIMITS MIN	TYP	MAX	μPD2764-3 LIMITS MIN	TYP	MAX	μPD2764-4 LIMITS MIN	TYP	MAX	UNIT	TEST CONDITITIONS
Address to Output Delay	t_{ACC}			250			300			450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}			250			300			450	ns	$\overline{OE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}			100			120			120	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Float	t_{DF}	0		85	0		105	0		105	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0			0			0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Test Conditions –

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2 V

Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5 %; V_{PP} = +21V ± 0.5V

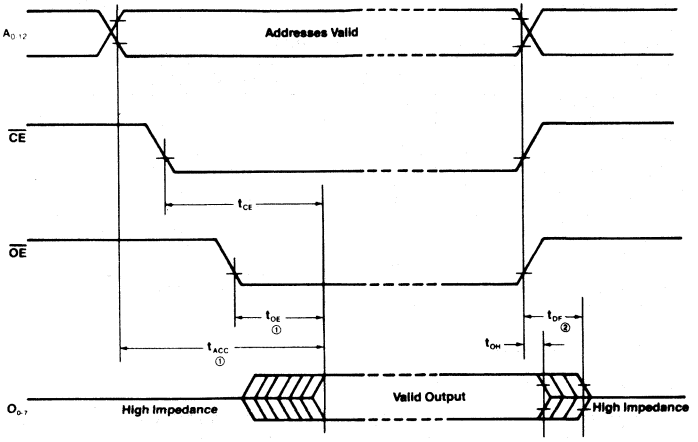
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width	t_{PW}	45	50	55	ms	
Vpp Setup Time	t_{VS}	2			μs	

Test Conditions –

Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20 ns

Timing Waveforms

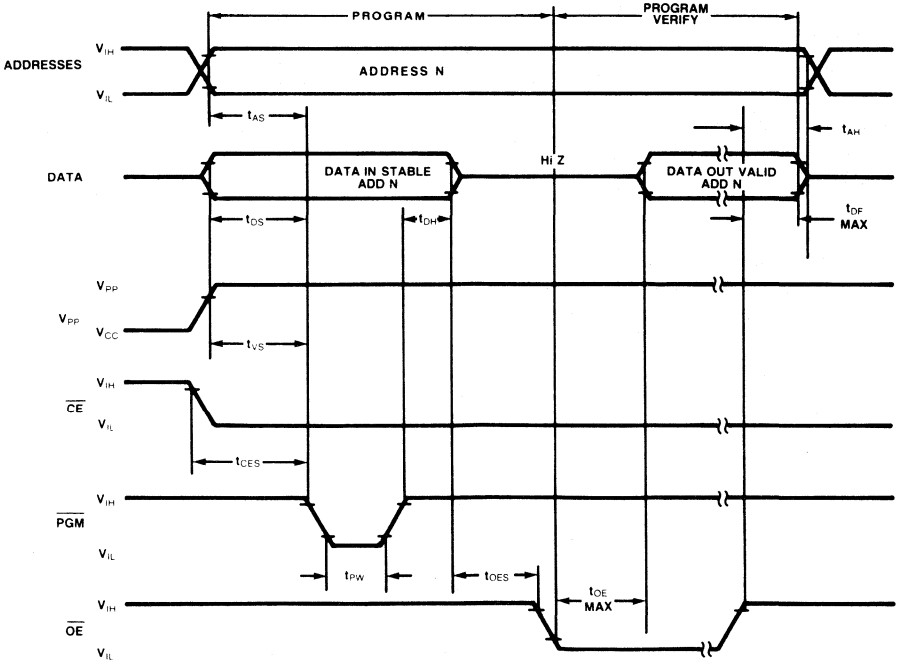
READ MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

CONVENTIONAL PROGRAM MODE



DC Characteristics

HIGH-SPEED PROGRAMMING MODE

(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}		−0.1		0.8	V
Input Leakage Current	I_{LI}	$V_{IH} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				100	mA
V_{PP} Current	I_{PP}	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC Characteristics

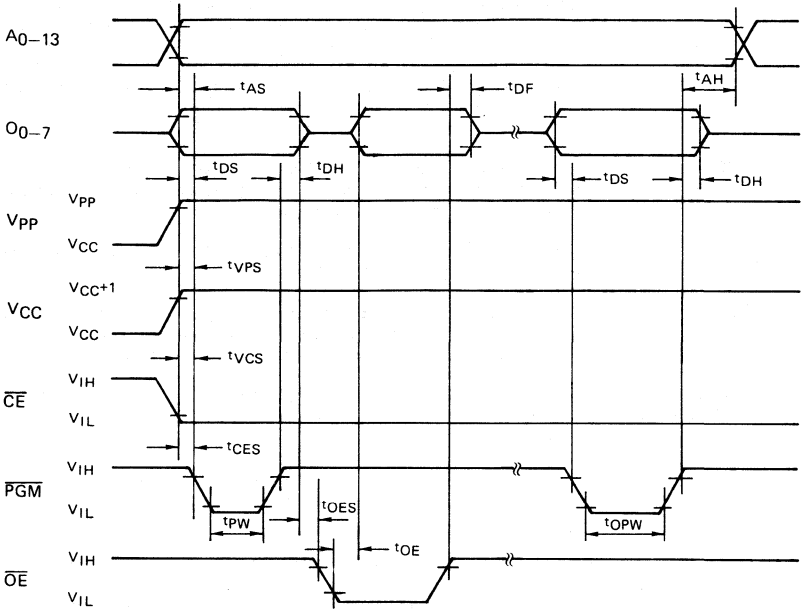
(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	t_{AS}		2			μs
$\overline{OE}$ Setup Time	t_{OES}		2			μs
Data Setup Time	t_{DS}		2			μs
Address Hold Time	t_{AH}		0			μs
Data Hold Time	t_{DH}		2			μs
$\overline{CE}$ to Ouput Float Time	t_{DF}		0		130	ns
V_{PP} Setup Time	t_{VPS}		2			μs
V_{CC} Setup Time	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{OPW}		3.8		63	ms
$\overline{CE}$ Setup Time	t_{CES}		2			μs
Data Valid from $\overline{OE}$	t_{OE}				150	ns

TEST CONDITIONS

- Input Pulse Levels: 0.45V and 2.0V
- Input Timing Reference Level: 0.8V and 2.0V
- Output Timing Reference Level: 0.8V and 2.0V

High-speed Program Mode (3)



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

(3) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

FUNCTION

The μPD2764 operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2764 is achieved with a single 50 ms TTL pulse. Total programming time for all 65,536 bits is 410 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2764 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 420 mW to a maximum standby power dissipation of 131 mW. This results in a 70 % savings with no increase in access time.

OPERATION

The five operation modes of the μPD2764 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for Vpp which is pulsed from TTL level to 21V.

READ MODE

When $\overline{CE}$ and $\overline{OE}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE

The μPD2764 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 67 % from 420 mW to 131 mW.

CONVENTIONAL PROGRAMMING MODE

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2764 is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with Vpp at +21V. The data to be programmed is applied to the output pins in 8 bit in parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD2764s are connected in parallel, except for $\overline{CE}$, individual μPD2764s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD2764 to be programmed.

Programming of multiple μPD2764s in parallel with the same data is easily accomplished. All the like inputs are tied together and are programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

HIGH-SPEED PROGRAMMING MODE

In this mode, programming begins by addressing the first location, and valid data appearing at the eight output pins (a low TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V±0.25V followed by V_{PP} raised to 21V±0.5V. A $\overline{PGM}$ pulse of 1 ms±5% is then applied in the same manner as decribed in the program mode timing diagram. The bit is then verified and a program/no program desicion is made. If the bit is not programmed, another 1 ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4 ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is applied and the bit verified. If the bit is not programmed at this stage, the device is rejected as a failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage V_{CC} and V_{PP} pins are lowered to 5V±5% and all bytes are then verified again for programming.

PROGRAMMING INHIBIT MODE

Progamming multiple μPD2764s in parallel with different data is easier with the program Inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD2764s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD2764 will inhibit it from being programmed.

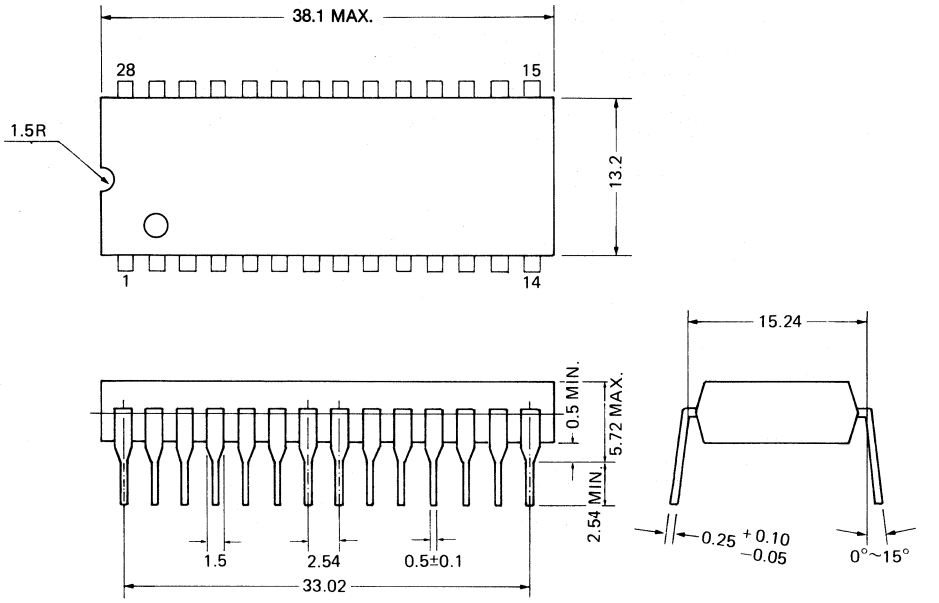
PROGRAM VERIFIY MODE

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at high (1) level.

OUTPUT DISABLE

The data outputs of two or more μPD2764s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2764s should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

Package Outline (mm)
μPD2764 C (Plastic)



131,072 (164 K 8) BIT PROM

Description

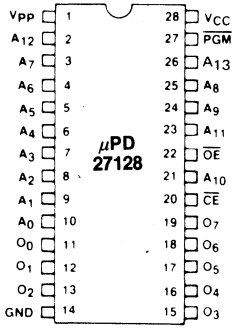
The μPD27128 is a 131,072-bit (16,384 x 8 bit) Electrically Programmable Read-Only Memory (PROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.

A distinctive feature of the μPD27128 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD27128 features fast, simple one-pulse programming controlled by TTL-level signals as well as high-speed programming mode. Total programming time for all 131,072 bits is 820 seconds for conventional mode and typically 120 seconds for high-speed mode.

Features

- Electrically programmable
- Access time
  - 250 ns (max) μPD27128
- Single location progamming
- Programmable with single pulse
- Low power dissipation: 100 mA max active current,
  25 mA max standby current
- High-speed programming mode (typical program time 120 s)
- Programmable with single pulse (total program time 820 s)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin Ceramic DIP
- Three-State outputs

Pin Configuration



Package C

PIN NAMES

A_0-A_{13}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs/Inputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program

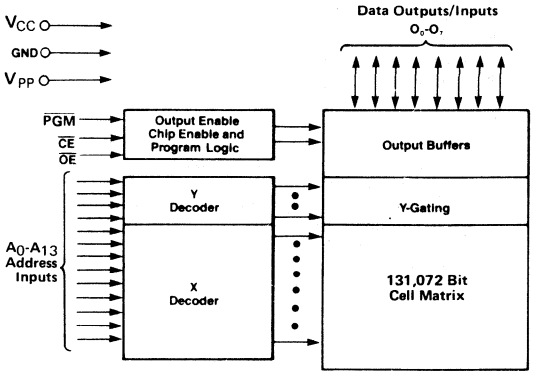
Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11 - 13, 15 - 19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
High-speed programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}

X can be either V_{IL} or V_{IH}

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings * (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6 to +6.5 V
Input Voltage	−0.6 to +6.5 V
Supply Voltage V_{CC}	−0.6 to +6.5 V
Supply Voltage V_{PP}	−0.6 to +22 V

* COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		12	14	pF	V_{OUT} = 0V

DC Characteristics

READ MODE AND STANDBY MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 5 %

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current		I_{LI1}			10	μA	V_{IN} = 5.25V
V_{PP} Current		I_{PP1}			15	mA	V_{PP} = 5.25V
V_{CC} Current	Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
	Active	I_{CC2}		60	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (CONT.)

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C, V_{CC} = +5V ± 5 % ① , V_{PP} = +21V ± 0.5V ②

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Input Leakage Current		I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	Program Inhibit	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current	Program Verify	I_{CC2}			100	mA	
V_{PP} Current	Program	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL}
V_{PP} Current	Program Verify	I_{PP3}			15	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
V_{PP} Current	Program Inhibit	I_{PP4}			15	mA	$\overline{CE}$ = V_{IH}

① V_{CC} = 6V ± 5 % for high-speed programming mode

② V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

AC Characteristics
Read Mode and Standby Mode
$T_A = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

Parameter	Symbol	Limits μPD 27128 Min.	Typ	Max.	Unit	Test Conditions
Address to Output Delay	t_{ACC}			250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			250	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			100	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

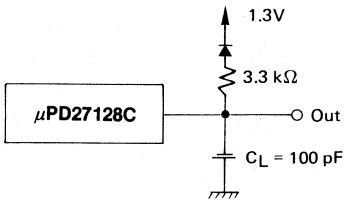
Test Conditions –
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 to 2.4 V
Timing Measurement Reference Level:
Inputs: 0.8V and 2.0V
Outputs: 0.8V and 2.0V

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

$T_a = 25°C \pm 5°C$; $V_{CC} = +5V \pm 5\%$; $V_{PP} = +21V \pm 0.5V$

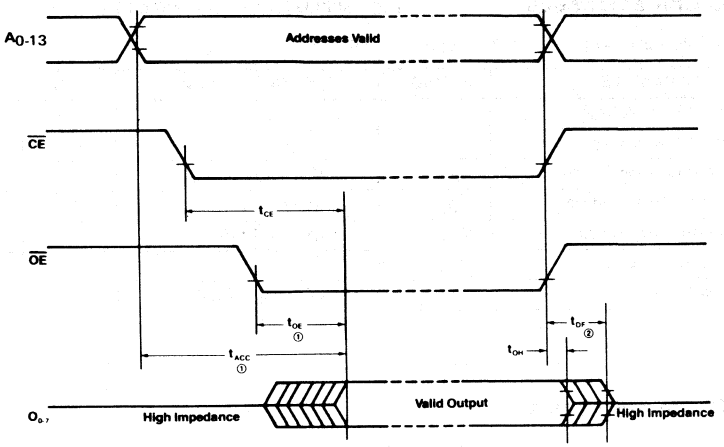
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width	t_{PW}	45	50	55	ms	
V_{PP} Setup Time	t_{VS}	2			μs	

Test Conditions –
Input Pulse Levels = 0.45 to 2.4V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20 ns



Timing Waveforms

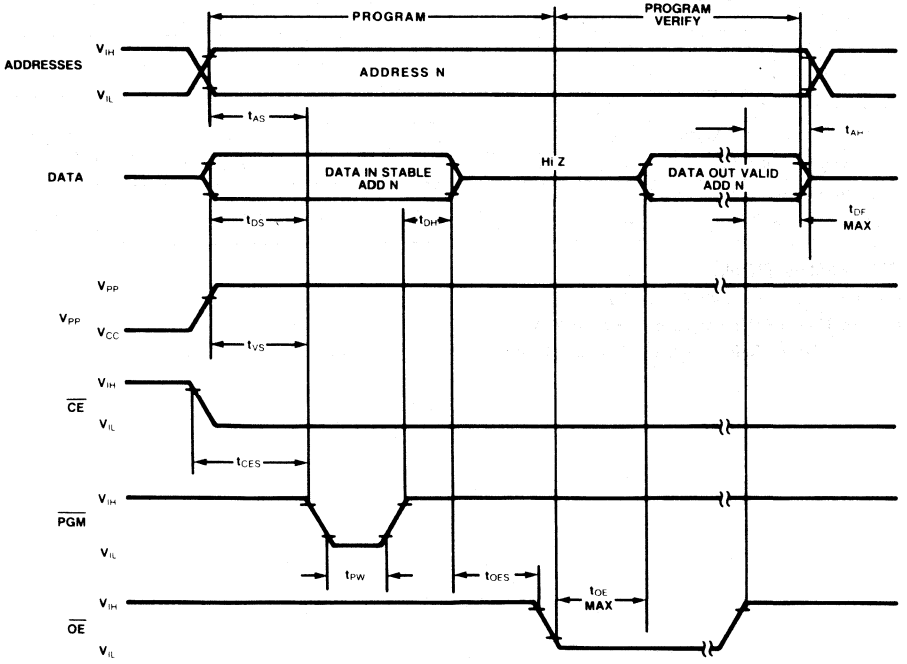
READ MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

CONVENTIONAL PROGRAM MODE



DC Characteristics

HIGH-SPEED PROGRAMMING MODE

(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}		−0.1		0.8	V
Input Leakage Current	I_{LI}	$V_{IH} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				100	mA
V_{PP} Current	I_{PP}	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC Characteristics

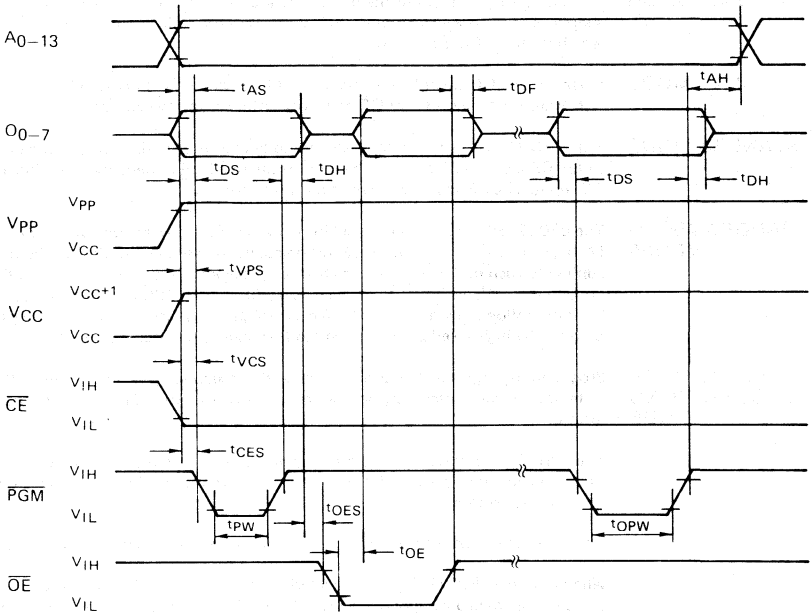
(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	t_{AS}		2			μs
$\overline{OE}$ Setup Time	t_{OES}		2			μs
Data Setup Time	t_{DS}		2			μs
Address Hold Time	t_{AH}		0			μs
Data Hold Time	t_{DH}		2			μs
$\overline{CE}$ to Ouput Float Time	t_{DF}		0		130	ns
V_{PP} Setup Time	t_{VPS}		2			μs
V_{CC} Setup Time	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{OPW}		3.8		63	ms
$\overline{CE}$ Setup Time	t_{CES}		2			μs
Data Valid from $\overline{OE}$	t_{OE}				150	ns

TEST CONDITIONS

- Input Pulse Levels: 0.45V and 2.0V
- Input Timing Reference Level: 0.8V and 2.0V
- Output Timing Reference Level: 0.8V and 2.0V

High-speed Program Mode (3)



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

(3) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

FUNCTION The μPD27128 operates from a single +5V power supply, making it ideal for microprocessor applications.

OPERATION The six operation modes of the μPD27128 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for V_{PP} which is pulsed from TTL level to 21V.

READ MODE When $\overline{CE}$ and $\overline{OE}$ are at low (0) level , READ ist set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE The μPD27128 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced.

PROGRAMMING MODES The μPD27128 can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventionel mode basically a 50 ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm ™, in which up to fifteen 1 ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4 ms $\overline{PGM}$ pulse for each number of 1 ms pulse applied before. The high-speed programming mode reduces the programming time to 120 s typical.

CONVENTIONAL PROGRAMMING MODE Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD27128 is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8 bit in parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD27128s are connected in parallel, except for $\overline{CE}$, individual μPD27128s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27128 to be programmed.

Programming of multiple μPD27128s in parallel with the same data is easily accomplished. All the like inputs are tied together and are programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

HIGH-SPEED PROGRAMMING MODE In this mode, programming begins by addressing the first location, and valid data appearing at the eight output pins (a low TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1 ms ± 5 % is then applied in the same manner as decribed in the program mode timing diagram. The bit is then verified and a program/no program desicion is made. If the bit is not programmed, another 1 ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4 ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is applied and the bit verified. If the bit is not programmed at this stage, the device is rejected as a failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage V_{CC} and V_{PP} pins are lowered to 5V ± 5 % and all bytes are then verified again for programming.

This algorithm is compatible with that of μPD2764.

PROGRAMMING INHIBIT MODE

Programming multiple μPD27128s in parallel with different data is easier with the program Inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27128s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with Vpp at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27128 will inhibit it from being programmed.

PROGRAM VERIFY MODE

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at high (1) level.

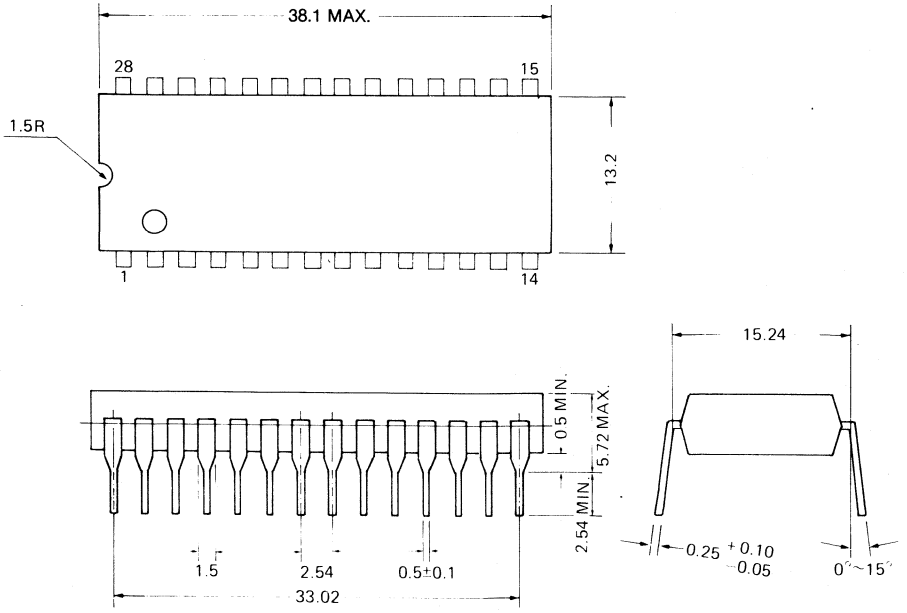
OUTPUT DISABLE

The data outputs of two or more μPD27128s may be wire-O Red together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27128s should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

TM: Intelligent Programming Algorithm is a registered trademark of Intel Coporation

Package Outline
μPD27128 C (Plastic)

28-PIN PLASTIC DIP OUTLINE (UNIT: mm)



ROM

— NMOS —

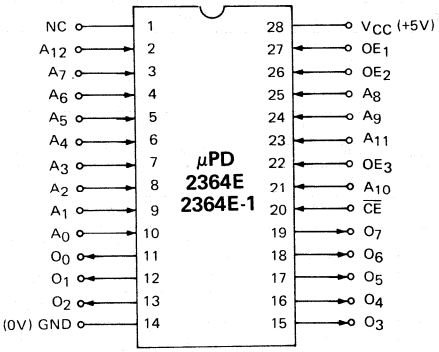
65,536 BIT MASK PROGRAMMABLE ROM

Description

The μPD2364E is a 65,536-bit Read Only Memory utilizing MOS N-channel silicon gate technology. The device is completely static in operation, organized as 8192 words by 8 bits, and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has three programmable chip select inputs and three-state outputs that allow memory expansion to 8192 words by 8 bits without the use of any external logic. Programming of the device is accomplished by a custom mask during fabrication. The μPD2364E pin-out is compatible with 2764 EPROM.

Features

- Two Fast Acces Time Options
  - 250 ns Maximum, μPD2364E
  - 200 ns Maximum, μPD2363E-1
- All Inputs and Outputs TTL Compatible
- Single +5 Volt Supply with ± 5 % Tolerance
- Three-State Outputs for Direct Bus Compatibility
- Three Programmable Chip Select Inputs
- Pin-Compatible to 2764 EPROM
- Fully Static Operation
- All Inputs Protected Against Static Charge



Package C

NOTE: The active Level of OE must be specified by the customer

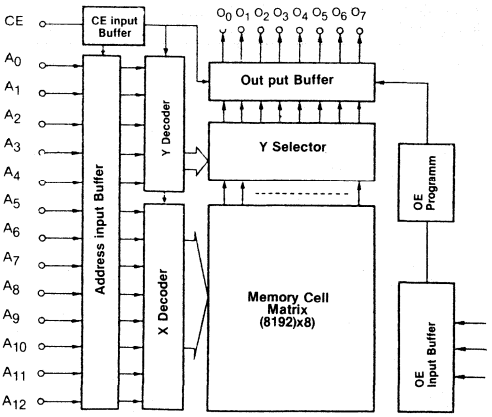
OE_1	OE_2	OE_3
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
X	X	X
0	0	0

X: Don't care

Block Diagram

PIN NAMES

$A_0 \sim A_{13}$:	Addresses
$\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$:	Output Enables
$\overline{CE}$:	Chip Enable
$O_0 \sim O_7$:	Data Outputs



Absolute Maximum Ratings

(T_a = 25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{DD}	−0.5 to +7	V
Input Voltage	V_I	−0.5 to +7	V
Output Voltage	V_O	−0.5 to +7	V
Operating Temperature	T_{opt}	−10 to +7	°C
Storange Temperature	T_{stg}	−65 to +150	°C

Capacitance

T_a = 25°C, f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10 pF		V_{IN} = 0V
Output Capacitance	C_{OUT}			15 pF		V_{OUT} = 0V

DC Characteristics

T_a = −10°C to +70°C and V_{CC} = 5V ± 5 %

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input "Low" Voltage	V_{IL}	−0.5		+0.7	V	
Input "High" Voltage	V_{IH}	+2.1		V_{CC} +1	V	
Input Load Current	I_{IL}			± 10	μA	V_{IN} = 0 to V_{CC}
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Output "High" Voltage	V_{OH}	+2.4			V	I_{OH} = −400 μA
Output Leakage Current	I_{LO}			± 10	μA	Chip Disabled, V_{out} = OV to V_{CC}
Power Supply Current	I_{CC1}		45	80	mA	CE = V_{IL}
Power Supply Current Standby Mode	I_{CC2}		12	20	mA	CE = V_{IH}

AC Characteristics

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

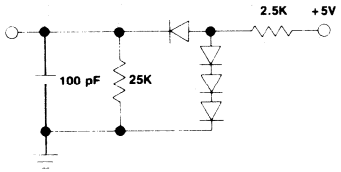
PARAMETER	SYMBOL	μPD2364E-1		μPD2364E		UNIT
		MIN	MAX	MIN	MAX	
Address to Output Delay Time	t_{ACC}		200		250	ns
Chip Enable to Output Delay Time	t_{CE}		200		250	ns
Chip Deselect to Output Data Float Time	t_{DF}	0	90	0	100	ns
Previous Data Valid After Address Change	t_{OH}	0		0		ns
OE_1 to OE_3 Output On Time	t_{OE}	10	100	10	110	ns

TEST CONDITIONS

Input Rise/Fall Times: 20ns
Timing Reference Levels:
Input Voltage = 0.8 and 2.0 V
Output Voltage = 0.8 and 2.0 V
Load = 1 TTL + 100 pF

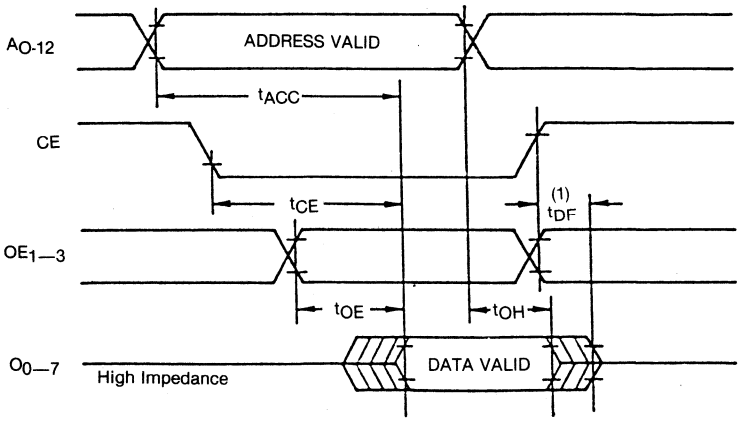
AC TEST CONDITIONS

Input Pulse Rise and Fall Times . . . . . 20 ns
Timing Measurement Reference Levels: . . . . . $V_{IH}, V_{OH} = 2.0V; V_{OL}, V_{IL} = 0.8V$



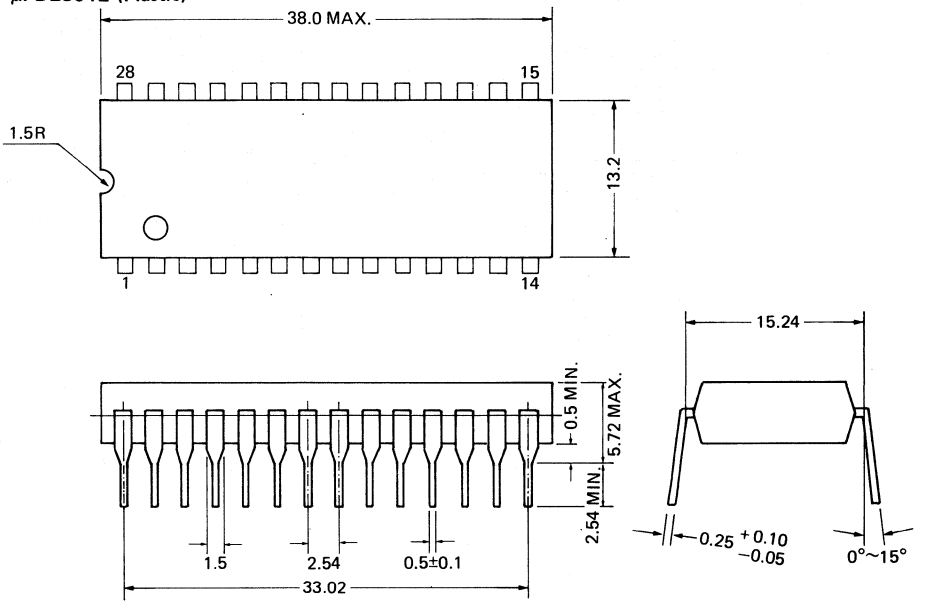
Output Load (AC): 1 TTL Load + 100 pF.

Timing Waveform



Note (1): t_{DF} is specified from OE or CE whichever occurs first.

Package Outlines
μPD2364E (Plastic)



131,072 BIT MASK PROGRAMMABLE ROM

Description

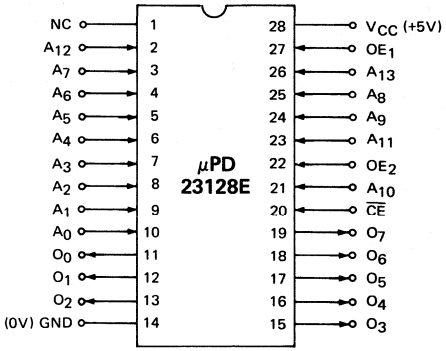
The μPD23128EC/D is a 131,072 bit Read Only Memory, utilizing NMOS silicon gate technology. The device is static in operation, organized as 16384 words by 8 bits and operates from a single +5 power supply. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The output enable pins are mask programmable and can be specified by selecting »1«, »0« and »Don't Care« Data. The μPD23128E is packaged in plastic (μPD23128EC) 28 PIN DIP. Pinout is compatible with 27128 EPROMS.

Features

- 16384 Words x 8 Bit Organization
- Access Time: 250 ns max.
- I/O TTL Compatible
- Three State Output
- Single +5V Power Supply Voltage
- 27128 Pin Compatible

Pin Configuration

(Top View)



Package C

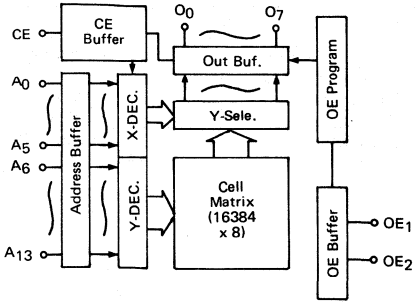
A_0 - A_{13}: Address
OE_1, OE_2: Output enable
O_0 - O_7: Output
$\overline{CE}$: Chip enable

Note: OE_1 - OE_2 inputs are specified by the following table:

OE_1	OE_2
0	0
1	0
0	1
1	1
X	X

X: Don't care

Block Diagram



Absolute Maximum Ratings (T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		−0.5 ~ +7	V
Input Voltage	V_I		−0.5 ~ +7	V
Output Voltage	V_O		−0.5 ~ +7	V
Operating Temperature	T_{opt}		−10 ~ +70	°C
Storage Temperature	T_{stg}		−65 ~ +150	°C

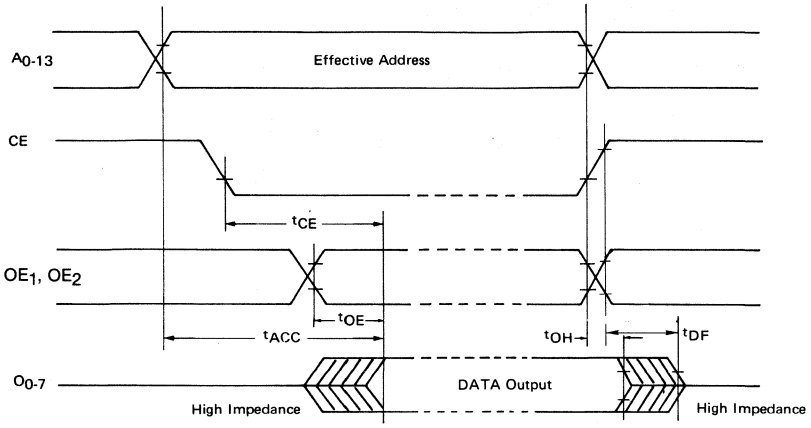
DC Characteristics (T_a = −10 ~ +70°C, V_{CC} = +5V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input High Voltage	V_{IH}		+2.0		V_{CC} +1.0	V
Input Low Voltage	V_{IL}		−0.5		+0.7	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	+2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA			+0.4	V
Input Leakage High	I_{LIH}	$V_I = V_{CC}$			+10	μA
Input Leakage Low	I_{LIL}	V_I = 0V			−10	μA
Output Lekage High	I_{LOH}	$V_O = V_{CC}$, Chip deselected			+10	μA
Output Lekage Low	I_{LOL}	V_O = 0V, Chip Deselected			−10	μA
Supply Current	I_{CC1}	$\overline{CE} = V_{IL}$		50	90	mA
	I_{CC2}	$\overline{CE} = V_{IH}$, Standby Mode		13	25	mA

AC Characteristics (T_a = −10 ~ +70°C, V_{CC} = +5V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Access Time	t_{ACC}	• Input Voltage tr, tf = 20 ns • Timing Voltage Input Voltage = 0.8 + 2.0V Output Voltage = 0.8V + 2.0V • Load = 1 TTL + 100 pF			250	ns
CHIP Enable Access Time	t_{CE}				250	ns
OE_1, OE_2 Output On Time	t_{OE}		10		110	ns
Output Hold Time	t_{OH}		0			ns
Output Disable Time	t_{DF}		0		100	ns

Timing Waveforms

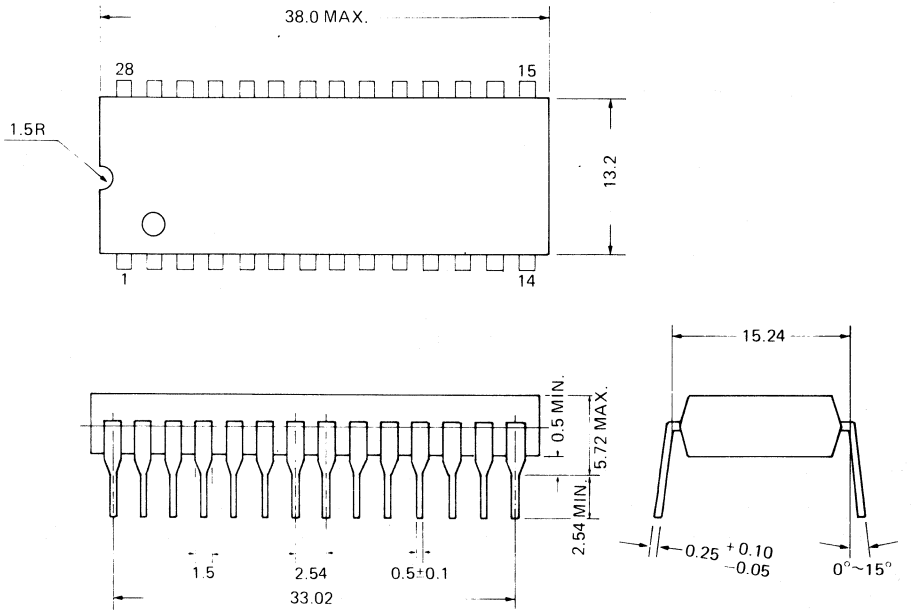


Capacitance Characteristics (T_a = −10 ~ +70°C, V_{CC} = +5V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	f = 1 MHz			10	pF
Output Capacitance	C_O				15	pF

Package Dimensions

28-PIN PLASTIC DIP OUTLINE (UNIT: mm)



EPROM

— CMOS —

262.144 (32 K X 8) BIT UV ERASABLE PROM

Features

- Ultraviolet erasable and electrically programmable
- Access time: 150ns max
- Single location programming
- High speed programming mode
- Low power dissipation: 40 mW/MHz (MAX) (active)
  550 μW (MAX) (standby)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-Pin DIP
- Three-state outputs
- CMOS Double-Polysilicon Technology

Absolute Maximum Ratings

Operating Temperature	−25 °C +85 °C
Storage Temperature	−65 °C to +125 °C
Output Voltage	−0.6 to V_{CC} +0.6V
Input Voltage	−0.6 to V_{CC} +0.6V
Supply Voltage V_{CC}	−0.6 to +7V
Supply Voltage V_{PP}	−0.6 to +22V

COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE*

(T_a = 25°C; f = 1 MHz)

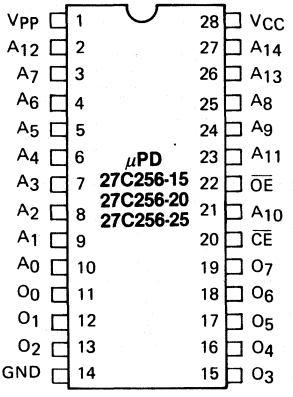
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Capacitance	C_{IN}	V_{IN} = 0V			6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			12	pF

* This parameter is periodically sampled.

Pin Configuration

(TOP VIEW)

Top View



Package D

PIN NAMES

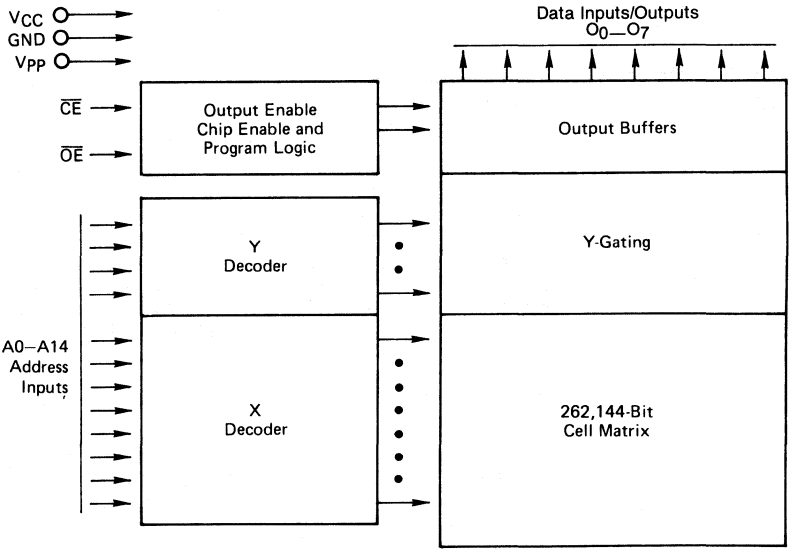
A_0–A_{14}	ADDRESSES
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE

Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Block Diagram



DC Characteristics

READ MODE AND STANDBY MODE

(T_a = 0°C to 70°C, V_{CC} = +5V ±10%, V_{PP} = V_{CC})

Parameter	Symbol	Limits Min.	Limits Typ	Limits Max.	Units	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = —400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = —2.1mA
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	—0.3		0.8	V	
Output Leakage Current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH} V_{OUT} = 0~V_{CC}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0~V_{CC}
V_{CC} Current (Active)	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IH} = V_{IN}
V_{CC} Current (Active)	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
V_{CC} Current (Standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current (Standby)	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}, V_{IN} = 0~V_{CC}
V_{PP} Current	I_{PP1}			100	μA	V_{PP} = V_{CC}

DC CHARACTERISTICS

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

(T_a = 25°C ± 5°C; V_{CC} = 6V ± 0.25V; V_{PP} = +21V ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input High Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input Leakage Current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	V_{OH} = −400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				30	mA
V_{PP} Current	I_{PP}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$			30	mA

AC CHARACTERISTICS

READ MODE AND STANDBY MODE

(T_a = 0° C to + 70° C, V_{CC} = +5V ± 10 %, $V_{PP} = V_{CC}$)

Parameter	Symbol	-15 *		-20		-25		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}	10	75	10	75	10	100	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

* V_{CC} = 5V ±5%

TEST CONDITIONS

Output Load:	See Fig. 1
Input Rise and Fall Times:	20 ns
Input Pulse Levels:	0.45 to 2.4V
Timing Measurement Reference Level:	Input: 0.8V and 2.0V
	Output: 0.8V and 2.0V

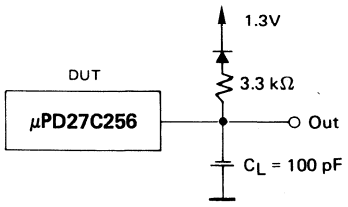
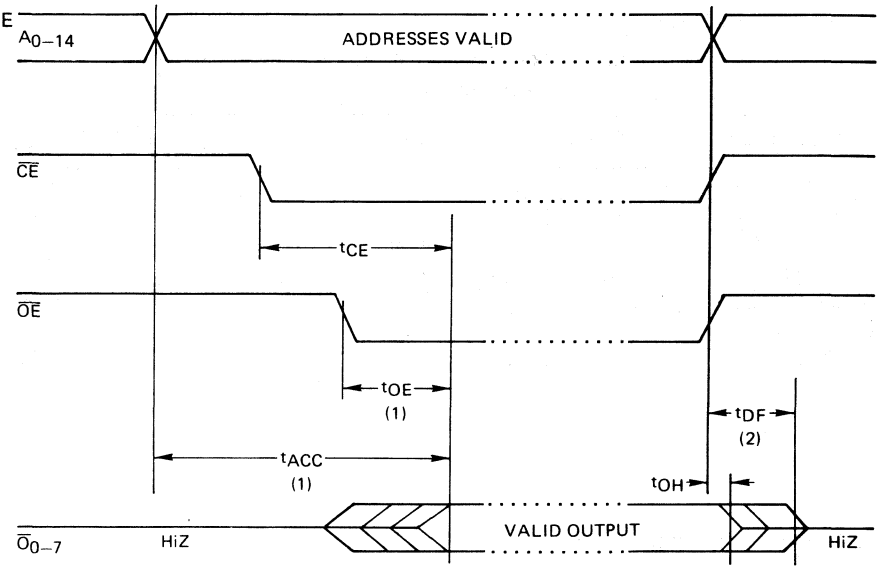


Fig. 1

READ MODE



Notes: 1 $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC Characteristics

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

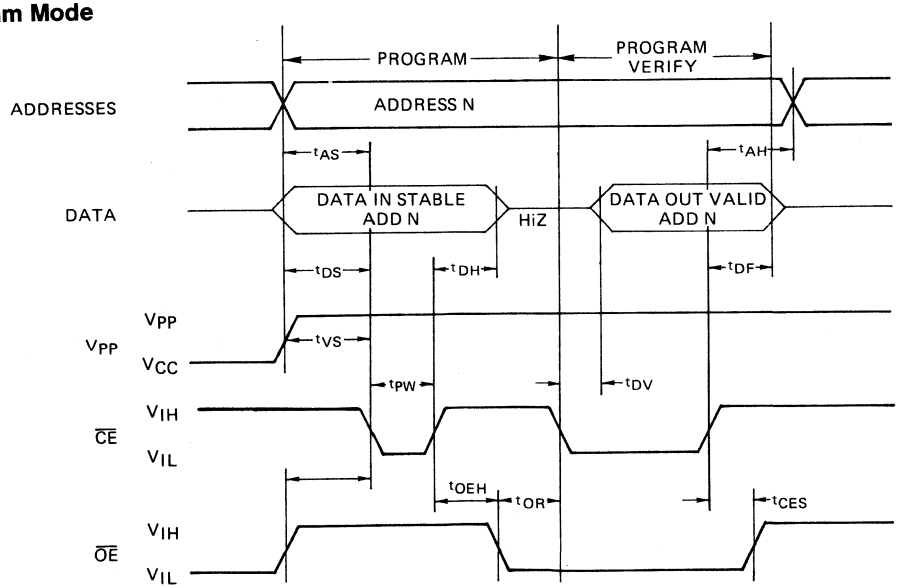
(T_a = 25°C ± 5°C; V_{CC} = +6V ± 0.25V; V_{PP} = 21V ± 0.5V)

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
Data Hold Time	t_{DH}	2			μs
Address Hold Time	t_{AH}	2			μs
Chip Enable to Output Float Delay	t_{DF}			130	ns
V_{CC} Set-up Time	t_{VCS}	2			μs
Program Pulse Width	t_{PW}	0.95	1	1.05	ms
$\overline{CE}$ Setup Time	t_{CES}	2			μs
$\overline{OE}$ Setup Time	t_{OES}	2			μs
*$\overline{OE}$ Hold Time	t_{OEH}	2			μs
*$\overline{OE}$ Recovery Time	t_{OR}	2			μs
*$\overline{CE}$ to Output Valid	t_{DV}			1	μs
V_{PP} Set up Time	t_{VPS}	2			μs

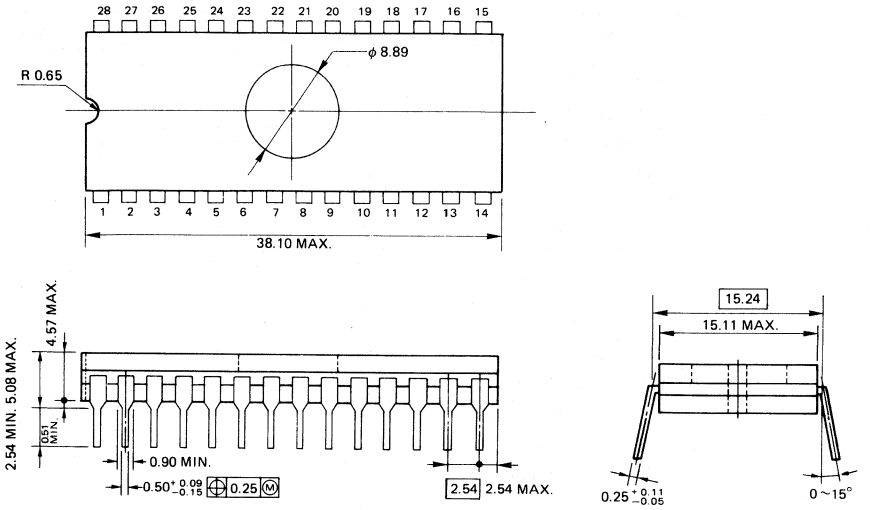
TEST CONDITION

Input Pulse Levels: = 0.45V to 2.4V
Input Timing Reference Level: = 0.8V and 2.0V
Output Timing Reference Level: = 0.8V and 2.0V
Input Rise and Fall Times: = 20 ns

Program Mode



Package Dimensions (Unit : mm)



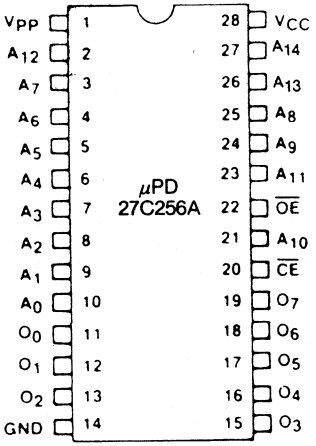
CMOS 262.144 (32K x 8) Bit UV ERASABLE PROM

Features

- Ultraviolet erasable and electrically programmable
- Access time - 120 ns max
- Single location programming
- Programmable with single pulse
- Low power dissipation:
  40mW/MHz (active)
  550μW (standby)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin DIP
- Three-state outputs
- Program Voltage - +12.5V
- CMOS Double-Polysilicon Technology

Pin Configuration

Top View



Pin Names

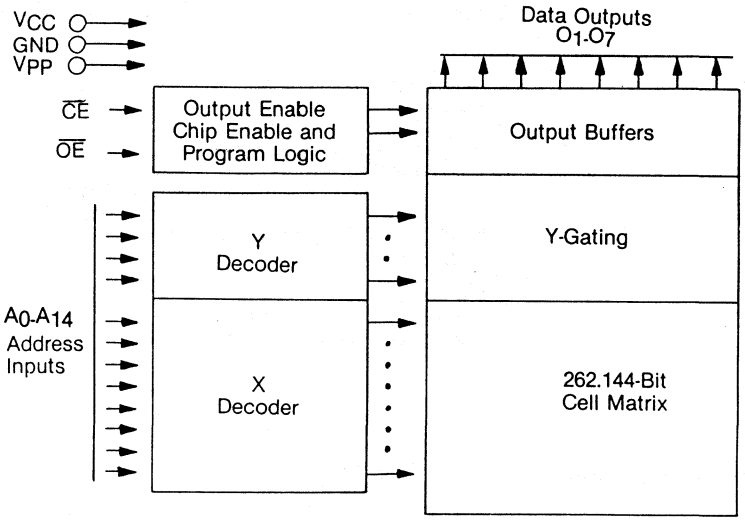
A0-A14	Addresses
$\overline{OE}$	Output Enable
O0-O7	Data Outputs
$\overline{CE}$	Chip Enable

Mode Selection

Mode \ Pins	CE (20)	OE (22)	VPP (1)	VCC (28)	Outputs (11-13, 15-19)
Read	VIL	VIL	VCC	VCC	Dout
Standby	VIH	X	VCC	VCC	High Z
Program	VIL	VIH	VPP	VCC	Din
Program Verify	VIH	VIL	VPP	VCC	Dout
Program Inhibit	VIH	VIH	VPP	VCC	High Z

X can be either VIL or VIH

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6 to V_{CC} +0.6V
Input Voltage	−0.6 to V_{CC} +0.6V
Supply Voltage V_{CC}	−0.6 to +7V
Supply Voltage V_{PP}	−0.6 to 13V

Comment

Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance *

Ta = 25°C, f = 1 MHZ

Parameter	Symbol	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
Input Capacitance	C_{in}			6	pF	V_{IN} = OV
Output Capacitance	C_{out}			12	pF	V_{out} = OV

* This parameter is periodically sampled.

DC Characteristics

Program, Program Verify and Program Inhibit Mode
$T_a = 25°C \pm 5°C$; $V_{CC} = +6V \pm 0.25V$; $V_{PP} = +12.5V \pm 0.3V$

Limits						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Input High Voltage	VIH	2.0		V_{CC} +0.3	V	
Input Low Voltage	VIL	−0.3		0.8	V	
Input Leakage Current	ILI			10	μA	VIN = VIL or VIH
Output High Voltage	VOH	2.4			V	IOH = 400 μA
Output Low Voltage	VOL			0.45	V	IOL = 2.1 mA
VCC Current	ICC			30	mA	
VPP Current	IPP 2			30	mA	$\overline{CE}$ = VIL; $\overline{OE}$ = VIH

DC Characteristics

Read Mode and Standby Mode
$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{CC}$

Parameter		Limits				
	Symbol	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Output High Voltage	VOH	2.4			V	IOH = 400 μA
Output Low Voltage	VOL			0.45	V	IOL = 2.1 mA
Input High Voltage	VIH	2.0		V_{CC} + 0.3	V	
Input Low Voltage	VIL	−0.3		0.8	V	
Output Leakage Current	ILO			10	μA	$\overline{OE}$ = VIH; VOUT = 0 ~ VCC
Input Leakage Current	ILI			10	μA	VIN = 0 ~ VCC
VCC Current (Active)	ICCA 1			30	mA	$\overline{CE}$ = VIL; VIN = VIH
	ICCA 2			30	mA	5 MHZ; IOUT = OmA
VCC Current (Standby)	ICCS 1			1	mA	$\overline{CE}$ = VIH
	ICCS 2			100	μA	$\overline{CE}$ = VCC
VPP Current	IPP 1			100	μA	VPP = VCC

AC Characteristics

Read Mode and Standby Mode

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{CC}$

Parameter	Symbol	—12 Min.	—12 Max.	—15 Min.	—15 Max.	—20 Min.	—20 Max	Unit	Test Conditions
Address to Output Delay	TACC		120		150		200	ns	$\overline{CE} = \overline{OE} = VIL$
$\overline{CE}$ to Output Delay	TCE		120		150		200	ns	$\overline{OE} = VIL$
Output Enable to Output Delay	TOE	10	60	10	75	10	75	ns	$\overline{CE} = VIL$
Output Enable High to Output Float	TDF	0	50	0	60	0	60	ns	$\overline{CE} = VIL$
Address to Output Hold	TOH	0		0		0		ns	$\overline{CE} = \overline{OE} = VIL$

Test Conditions

Output Load: See Fig. 1
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Level:
Input: 0.8V and 2.0V
Output: 0.8V and 2.0V

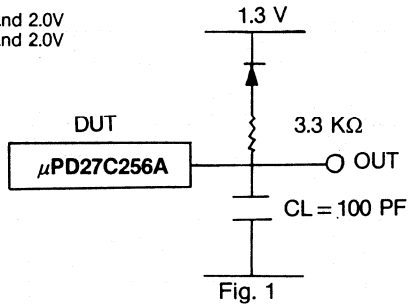


Fig. 1

AC Characteristics

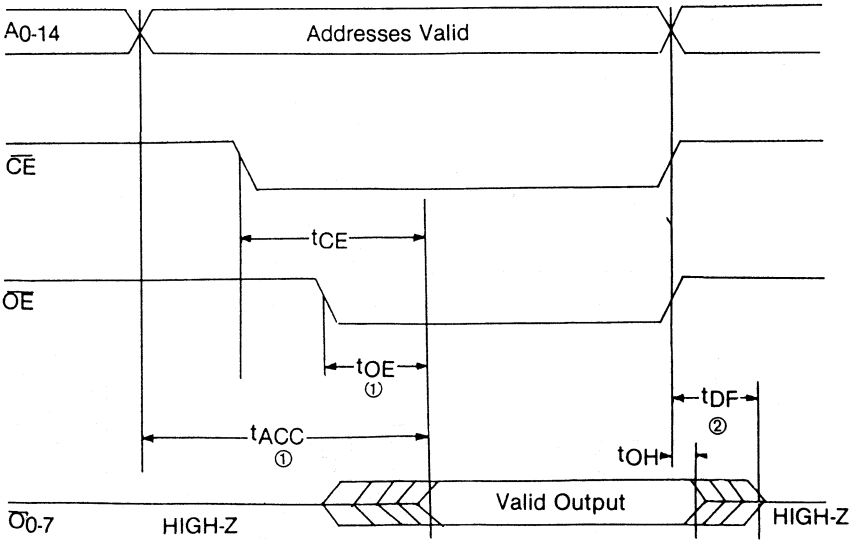
Program, Program Verify and Program Inhibit Mode
$T_a = 25°C \pm 5°C$; $V_{CC} = +6V \pm 0.25V$; $V_{PP} = 12.5V \pm 0.3V$

		Limits			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Address Setup Time	TAS	2			μS
Data Setup Time	TDS	2			μS
Data Hold Time	TDH	2			μS
Address Hold Time	TAH	0			μS
Chip Enable to Output Float Delay	TDF			130	nS
VPP Setup Time	TVPS	2			μS
VCC Setup Time	TVCS	2			μS
Program Pulse Width	TPW	0.95	1	1.05	ms
Overprogram Pulse Width	TOPW	0.95		21	ms
Data Valid from $\overline{OE}$	TOE			150	nS
$\overline{OE}$ Setup Time	TOES	2			μS

Test Condition

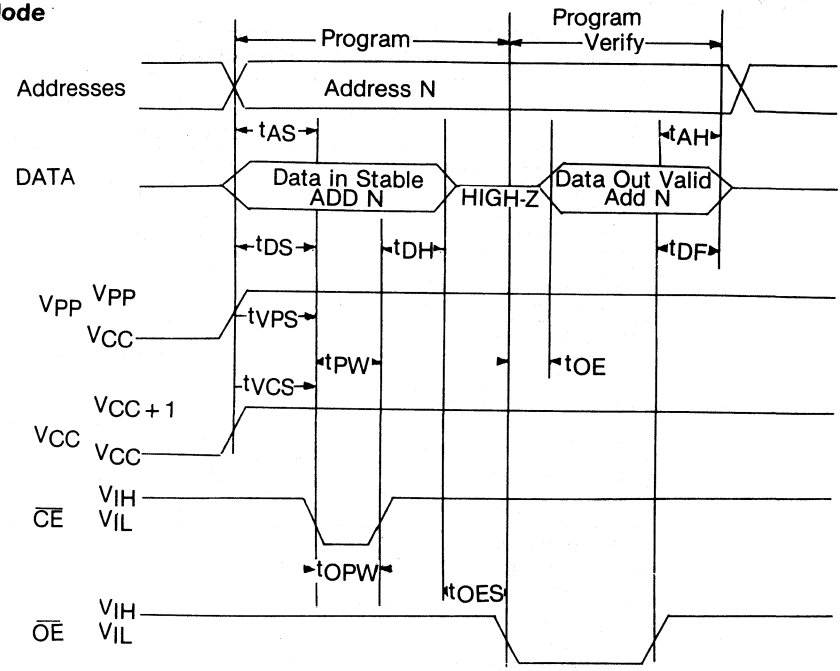
Input Pulse Levels = 0.45 V to 2.4V
Input Timing Reference Level = 0.8V and 2.0V
Output Timing Reference Level + 0.8V and 2.0V
Input Rise and Fall Times: 20 ns

Read Mode

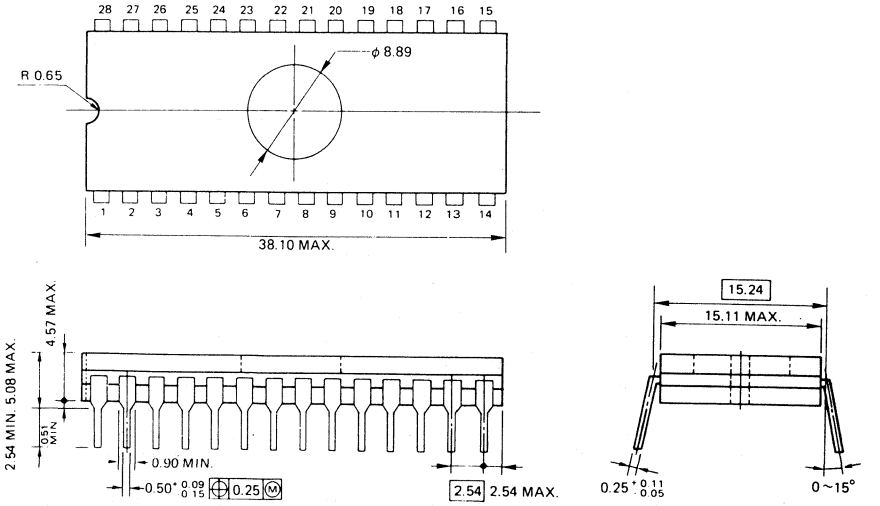


Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode



Package Dimensions (Unit : mm)



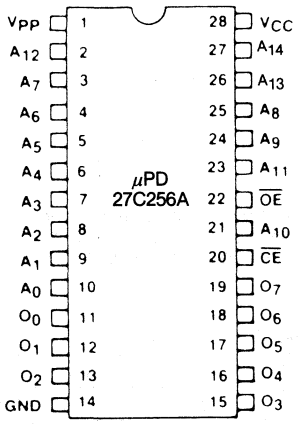
CMOS 262.144 (32K x 8) Bit UV ERASABLE PROM

Features

- Ultraviolet erasable and electrically programmable
- Access time - 200ns max
- Single location programming
- Programmable with single pulse
- Low power dissipation:
  40mW/MHz (active)
  550μW (standby)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin DIP
- Three-state outputs
- Program Voltage - +12.5V
- CMOS Double-Polysilicon Technology
- Extended temperature (T_a = −40 ~ +85°C)

Pin Configuration

Top View



Pin Names

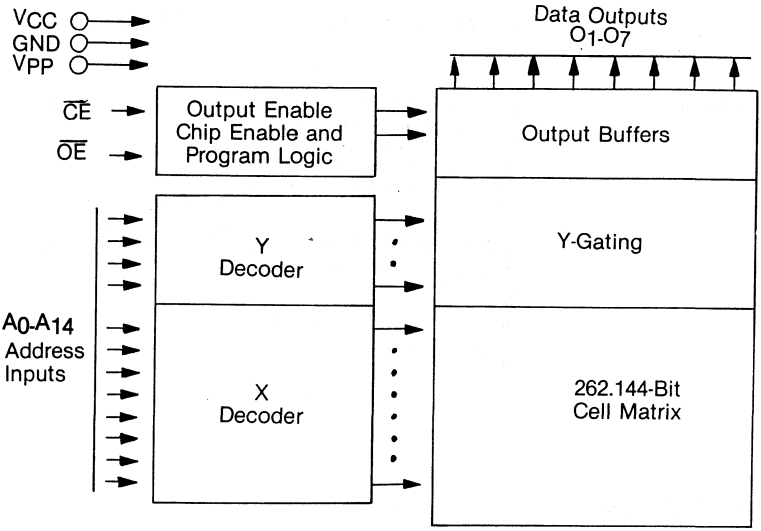
A0 - A14	Addresses
$\overline{OE}$	Output Enable
O0 - O7	Data Outputs
$\overline{CE}$	Chip Enable

Mode Selection

Mode \ Pins	CE (20)	OE (22)	VPP (1)	VCC (28)	Outputs (11-13, 15-19)
Read	VIL	VIL	VCC	VCC	Dout
Standby	VIH	X	VCC	VCC	High Z
Program	VIL	VIH	VPP	VCC	Din
Program Verify	VIH	VIL	VPP	VCC	Dout
Program Inhibit	VIH	VIH	VPP	VCC	High Z

X can be either VIL or VIH

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Operating Temperature..... −40°C to +85°C
Storage Temperature..... −65°C to +125°C
Output Voltage..... −0.6 to V_{CC} +0.6V
Input Voltage..... −0.6 to V_{CC} +0.6V
Supply Voltage V_{CC}..... −0.6 to +7V
Supply Voltage V_{PP}..... −0.6 to 13V

Comment

Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance *

Ta = 25°C, f = 1 MHZ

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Capacitance	C_{in}			6	pF	V_{IN} = OV
Output Capacitance	C_{out}			12	pF	V_{out} = OV

* This parameter is periodically sampled.

DC Characteristics

Program, Program Verify and Program Inhibit Mode
$T_a = 25°C \pm 5°C$; $V_{CC} = +6V \pm 0.25V$; $V_{PP} = +12.5V \pm 0.3V$

		Limits				
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Input High Voltage	VIH	2.2		V_{CC} +0.3	V	
Input Low Voltage	VIL	−0.3		0.8	V	
Input Leakage Current	ILI			10	μA	VIN = VIL or VIH
Output High Voltage	VOH	2.4			V	IOH = 400 μA
Output Low Voltage	VOL			0.45	V	IOL = 2.1 mA
VCC Current	ICC			30	mA	
VPP Current	IPP 2			30	mA	$\overline{CE}$ = VIL; $\overline{OE}$ = VIH

DC Characteristics

Read Mode and Standby Mode
$T_a = -40°C$ to $+85°C$; $V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{CC}$

		Limits				
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Output High Voltage	VOH	2.4			V	IOH = 400 μA
Output Low Voltage	VOL			0.45	V	IOL = 2.1 mA
Input High Voltage	VIH	2.0		V_{CC} + 0.3	V	
Input Low Voltage	VIL	−0.3		0.8	V	
Output Leakage Current	ILO			10	μA	$\overline{OE}$ = VIH; VOUT = 0~VCC
Input Leakage Current	ILI			10	μA	VIN = 0 ~ VCC
VCC Current (Active)	ICCA 1			30	mA	$\overline{CE}$ = VIL; VIN = VIH
	ICCA 2			30	mA	5 MHZ; IOUT = OmA
VCC Current (Standby)	ICCS 1			1	mA	$\overline{CE}$ = VIH
	ICCS 2			100	μA	$\overline{CE}$ = VCC
VPP Current	IPP 1			100	μA	VPP = VCC

AC Characteristics

Read Mode and Standby Mode
$T_a = -40°C$ to $+85°C$; $V_{CC} = +5V \pm 10\%$; $V_{PP} = V_{CC}$

		−20		−25			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max**	**Unit**	**Test Conditions**
Address to Output Delay	TACC		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
$\overline{CE}$ to Output Delay	TCE		200		250	ns	$\overline{OE}$ = VIL
Output Enable to Output Delay	TOE	10	75	10	100	ns	$\overline{CE}$ = VIL
Output Enable High to Output Float	TDF	0	60	0	85	ns	$\overline{CE}$ = VIL
Address to Output Hold	TOH	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = VIL

Test Conditions

Output Load: See Fig. 1
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Level:

Input: 0.8V and 2.0V
Output: 0.8V and 2.0V

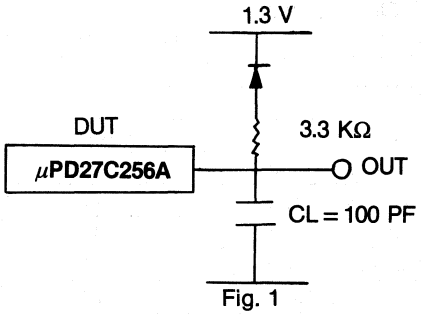


Fig. 1

AC Characteristics

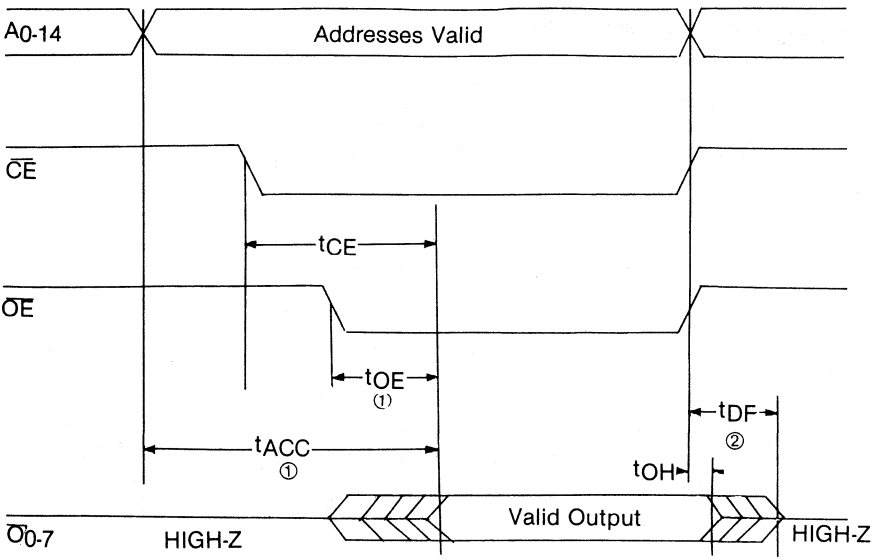
Program, Program Verify and Program Inhibit Mode
$T_a = 25°C \pm 5°C$; $V_{CC} = +6V \pm 0.25V$; $V_{PP} = 12.5V \pm 0.3V$

		Limits			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Address Setup Time	TAS	2			μS
Data Setup Time	TDS	2			μS
Data Hold Time	TDH	2			μS
Address Hold Time	TAH	0			μS
Chip Enable to Output Float Delay	TDF			130	nS
VPP Setup Time	TVPS	2			μS
VCC Setup Time	TVCS	2			μS
Program Pulse Width	TPW	0.95	1	1.05	nS
Overprogram Pulse Width	TOPW	0.95		21	nS
Data Valid from $\overline{OE}$	TOE			150	nS
$\overline{OE}$ Setup Time	TOES	2			μS

Test Condition

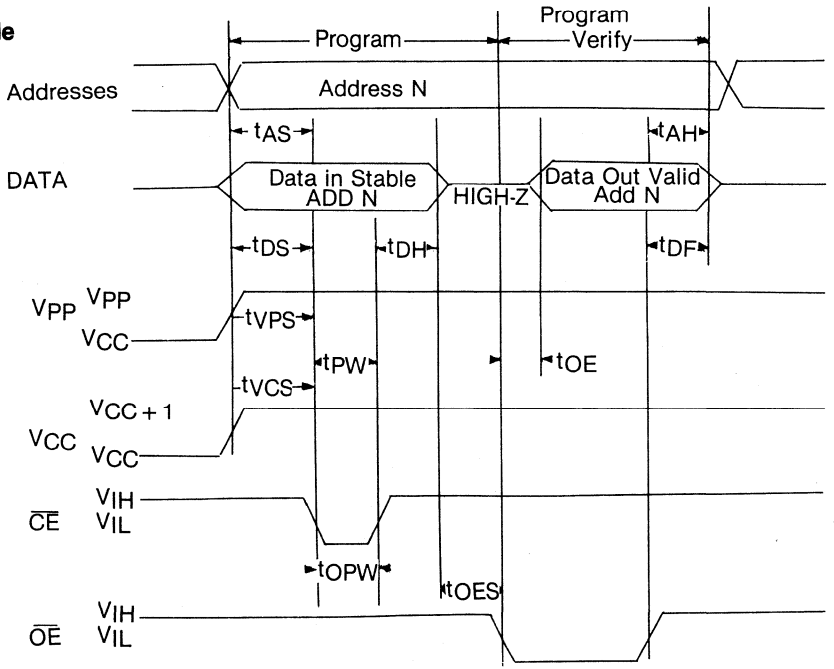
Input Pulse Levels = 0.45 V to 2.4V
Input Timing
Reference Level = 0.8V and 2.0V
Output Timing
Reference Level + 0.8V and 2.0V
Input Rise and Fall Times: 20 ns

Read Mode

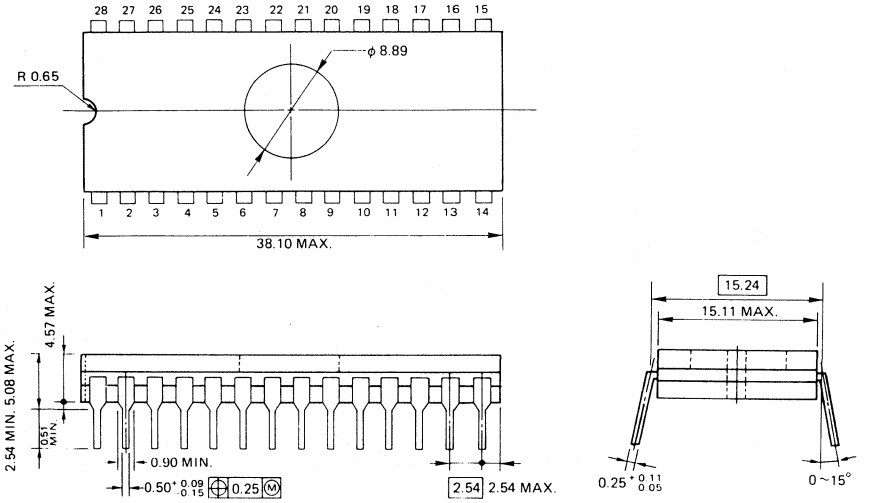


Notes: 1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode



Package Dimensions (Unit : mm)



262 144 Bit CMOS UV EPROM

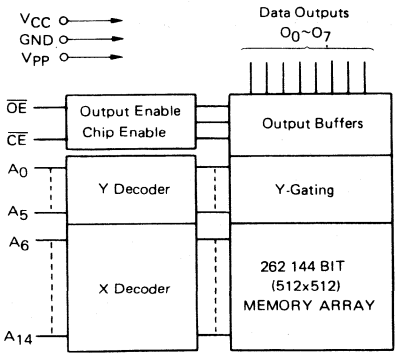
Description

The μPD27C256AK is a 262 144 bit (32 768 x 8-bit) ultraviolet erasable and electrically programmable read-only memory (UV EPROM). It operates from a single +5 V power supply, making it ideal for mircoprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system. The μPD27C256AK is available in a standard 32-pin leadless chip carrier with a quartz window.

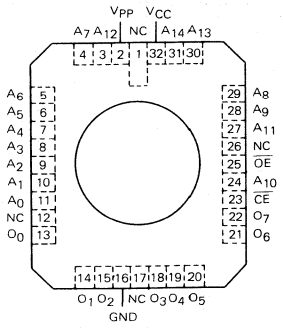
Features

- 32 768-words by 8-bit organization
- Ultraviolet erasable and electrically programmable
- Fast access time: 120 ns MAX. (μPD27C256AK–12)
  150 ns MAX. (μPD27C256AK–15)
  200 ns MAX. (μPD27C256AK–20)
- Low power dissipation: 30 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 32-pin leadless chip carrier with a quartz window

Block Diagram



Pin Configuration



PIN NAMES

A_0 ~ A_{14}	Addresses
O_0 ~ O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
V_{PP}	Program Voltage
GND	Ground
NC	No Connect

Mode Selection

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O_0~O_7
Read	V_{IL}	V_{IL}	+5 V	+5 V	D_{OUT}
Output Desable	V_{IL}	V_{IH}	+5 V	+5 V	High-Z
Standby	V_{IH}	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	+12.5 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25 to +85	°C
Storage Temperature	−55 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (Ag)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +13.5	V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP}=V_{CC}$			V
Input High Voltage	V_{IH}	2.0	–	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Ambient Temperature	T_a	0	–	70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	$I_{OH}=-400\,\mu A$
	V_{OH2}	$V_{CC}-0.7$			V	$I_{OH}=-100\,\mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL}=2.1$ mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT}=0$~V_{CC}, $\overline{OE}=V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN}=0$~V_{CC}
V_{PP} Current	I_{PP}		1	100	μA	$V_{PP}=V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE}=V_{IL}$, $V_{IN}=V_{IH}$
	I_{CCA2}			30	mA	f = 5 MHz, $I_{OUT}=0$ mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE}=V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE}=V_{CC}$, $V_{IN}=0$~V_{CC}

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C256AK-12		μPD27C256AK-15		μPD27C256AK-20		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		60		75		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ High to Output Float	t_{DF}	0	50	0	60	0	60	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≤ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

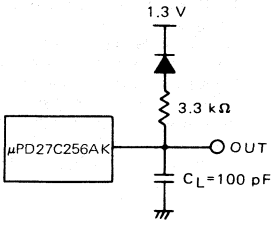
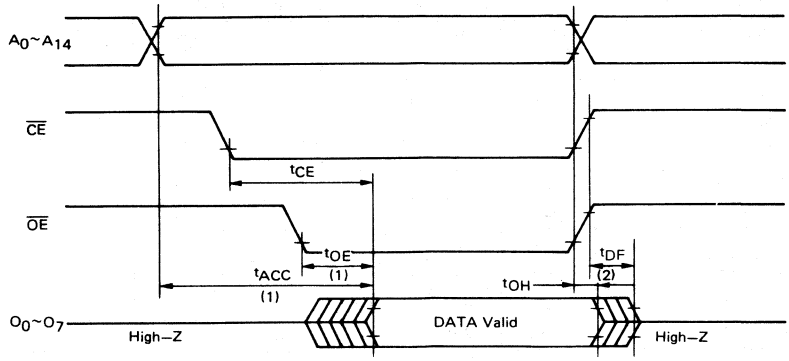


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Programming Operation

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C256AK is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight output pins. V_{CC} is then raised to +6 ±0.25 V followed by V_{PP} raised to +12.5 ±0.3 V. A $\overline{CE}$ pulse of 1 ms ±5 % is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 25 times. If the bit gets programmed within 25 efforts, another pulse of 3 ms for each effort is applied and the next address is applied until all addresses are complete. If the bit does not get programmed in 25 efforts, the device would be rejected as a program failure.

At this stage, V_{CC} and V_{PP} pins are lowered to +5V ±10 % and all bytes are then verified again for programming. When programming multiple μPD27C256AKs in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel μPD27C256AKs may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with V_{PP} at +12.5 V. A high (1) level applied to the $\overline{CE}$ of the other μPD27C256AK will inhibit it from being programmed.

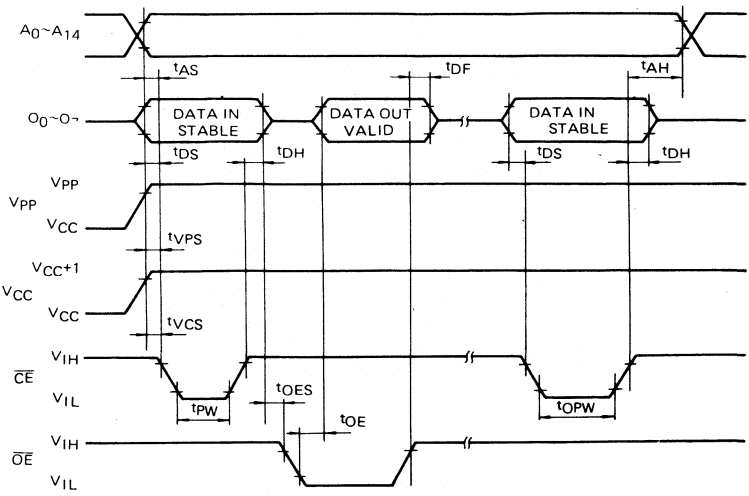
DC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$

AC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	2.85		78.75	ms	
$\overline{OE}$ to Output Delay	t_{OE}			150	ns	

Programming Mode Timing



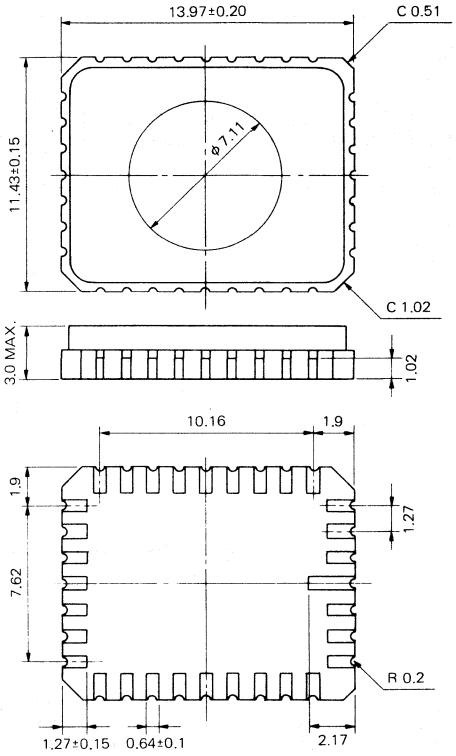
Notes : (1) V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
(2) Vpp must not be greater than +13 V including overshoot.

Erasure

Erasure of the μPD27C256AK programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27C256AK. Consequently, if the μPD27C256AK is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD27C56AK is exposure to ultraviolet light with wavelength of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12 000 $\mu W/CM^2$ power rating. During erasure, the μPD27C256AK should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

32 PIN LEADLESS CHIP CARRIER



524 288 BIT CMOS UV ERASABLE PROM

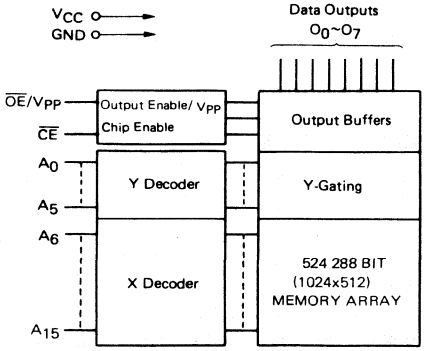
Description

The μPD27C512D is a 524 288 bits (65 536 x 8-bits) ultraviolet erasable and electrically programmable read-only memory (UV EPROM). It operates from a single +5 V power supply, making it ideal for microprocessor applictions. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C512D is available in a standard 28-pin cerdip package with a quartz window.

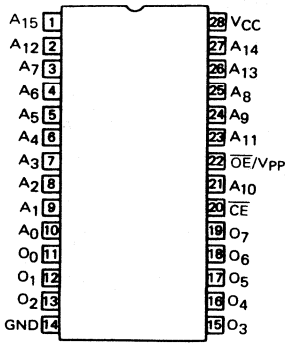
Features

- 65 536-words by 8-bits organization
- Ultraviolet erasable and electrically programmable
- Fast access time: 150 ns MAX. (μPD27C512D–15)
  200 ns MAX. (μPD27C512D–20)
  250 ns MAX. (μPD27C512D–25)
- Low power dissipation: 30 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 28-pin DIP

Block Diagram



Pin Configuration



PIN NAMES

A_0 ~ A_{15}	Addresses
O_0 ~ O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/VPP
VCC	Supply Voltage
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	$O_0 \sim O_7$
Read	V_{IL}	V_{IL}	+5 V	D_{OUY}
Output Desable	V_{IL}	V_{IH}	+5 V	High-Z
Standby	V_{IH}	X	+5 V	High-Z
Program	V_{IL}	V_{IH}	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +80	°C
Storage Temperature	−65 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to + 7	V
Input Voltage (Ag)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +13.5	V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditons for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	$V_{CC}-0.7$			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 0 \sim V_{CC}$, $\overline{OE} = V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = 0 \sim V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
	I_{CCA2}			30	mA	f = 5 MHz, I_{OUT} = 0 mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0 \sim V_{CC}$

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C512D-15		μPD27C512D-20		μPD27C512D-25		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{CE}$ = $\overline{OE}$/Vpp = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$/Vpp = V_{IL}
$\overline{OE}$/Vpp to Output Delay	t_{OE}		75		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$/Vpp High to Output Float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$/Vpp = V_{IL}

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≤ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

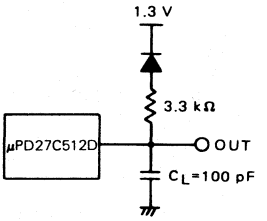
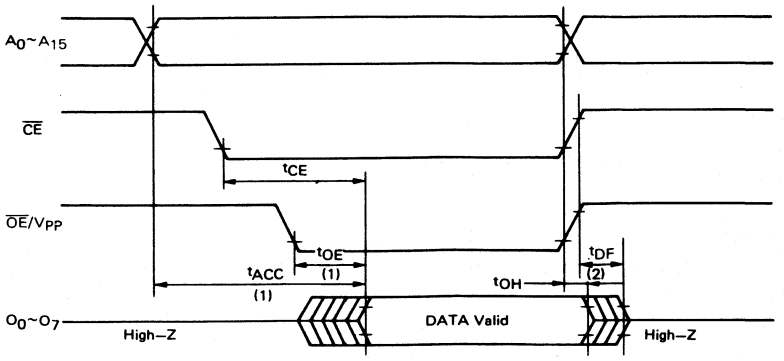


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN1}		4	6	pF	V_{IN} = 0 V
	C_{IN2}		12	20	pF	$\overline{OE}$/Vpp, V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$/Vpp may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$/Vpp or $\overline{CE}$, whichever occurs first.

Programming Operation

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C512D is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with $\overline{OE}$/VPP at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight output pins. V_{CC} is then raised to +6 ± 0.25 V followed by $\overline{OE}$/VPP raised to +12.5 ± 0.3 V. A $\overline{CE}$ pulse of 1 ms ± 5 % is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 25 times. If the bit gets programmed within 25 efforts, another pulse of 3 ms for each effort is applied and the next address is applied. If the bit does not get programmed in 25 efforts, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and VPP pins are lowered to +5 V ± 5 % and all bytes are then verfied again for programming.

When programming multiple μPD27C512Ds in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$/VPP) of the parallel μPD27C512Ds may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with $\overline{OE}$/VPP at +12.5 V. A high (1) level applied to the $\overline{CE}$ of the other μPD27C512D will inhibit it from being programmed.

DC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, VPP=12.5±0.3 V)

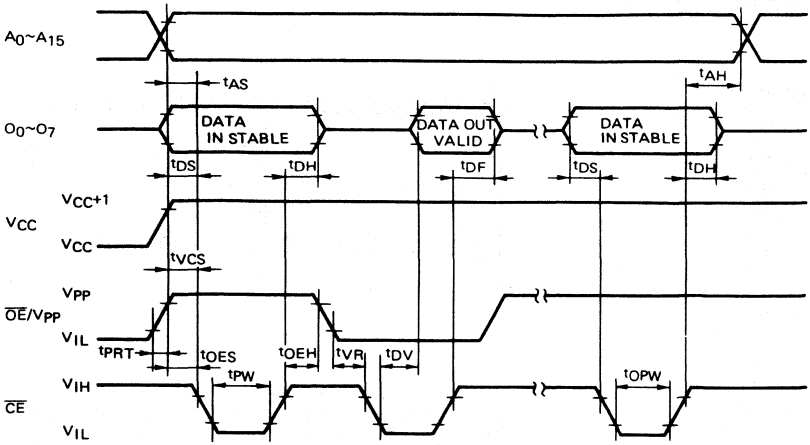
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
VPP Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}$/VPP = V_{IH}

AC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, VPP=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$/Vpp Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ to Output Delay	t_{DV}			1	μs	$\overline{CE} = \overline{OE}/VPP = V_{IL}$
$\overline{OE}$/Vpp Hold Time	t_{OEH} *	2			μs	
$\overline{OE}$/Vpp Recovery Time	t_{VR} *	2			μs	
$\overline{OE}$/Vpp Rise Time	t_{PRT}	50			ns	

$t_{OEH} + t_{VR} \geq 50$ μs

Programming Mode Timing



Notes : (1) V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
(2) V_{PP} must not be greater than +13 V including overshoot.

Erasure

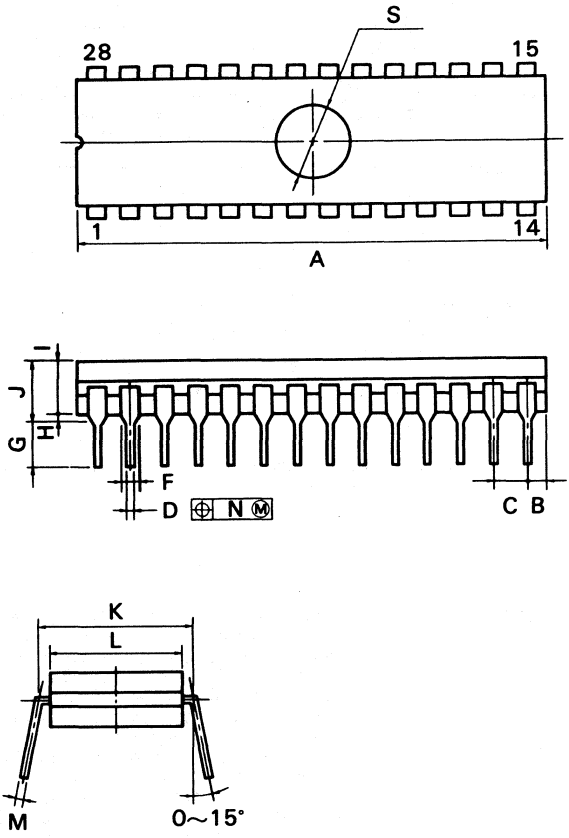
Erasure of the μPD27C512D programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27C512D. Consequently, if the μPD27C512D is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD27C512D is exposure to ultraviolet light with wavelengths of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12 000 μW/cm^2 power rating. During erasure, the μPD27C512D should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Package Dimensions

28 PIN CERAMIC DIP (600 mil)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{\pm 0.10}$
F	1.2 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	3.80
J	5.08 MAX.
K	15.24 (T.P.)
L	14.66
M	$0.25^{\pm 0.05}$
N	0.25
S	ϕ 8.89



1048 576 BIT CMOS UV EPROM

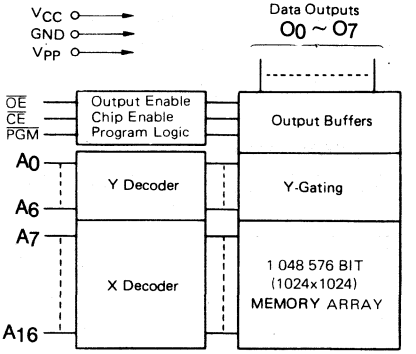
Description

The μPD27C1000D is a 1048576 bits (131072x8 bits) ultraviolet erasable and electrically programmable read-only memory (UV EPROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C1000D is available in a standard 32-pin cerdip package with a quartz window.
It is pin compatible to 28 pin Maskroms

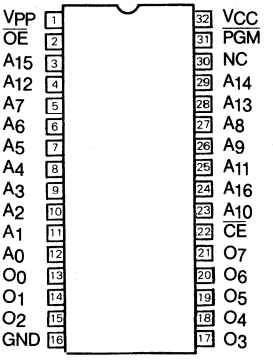
Features

- 131072 words by 18-bits organization
- Ultraviolett erasable and electrically programmable
- Fast access time: 150 ns MAX. (μPD27C1000D-15)
  200 ns MAX. (μPD27C1000D-20)
  250 ns MAX. (μPD27C1000D-25)
- Low power dissipation: 50 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 32-pin DIP
- Pin compatible to 28 pin Maskroms

Block Diagram



Pin Configuration



PIN NAMES

A0 ~ A16	Address	OE	Output Enable
O0 ~ O7	Data Outputs	VCC	Supply Voltage
CE	Chip Enable	VPP	Program Voltage
PGM	Program	GND	Ground
		NC	No Connection

MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	O_0~O_{15}
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output Desable	V_{IL}	V_{IH}	X	+5 V	+5 V	High-Z
Standby	V_{IH}	X	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	X	+12.5 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +80	°C
Storage Temperature	−65 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (Ag)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +13.5	V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP} = V_{CC}$			V
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	V_{CC}−0.7			V	$I_{OH} = -100\ \mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 0$~V_{CC}, $\overline{OE} = V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = 0$~V_{CC}
V_{PP} Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0$~V_{CC}

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C1000D-15		μPD27C1000D-20		μPD27C1000D-25		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Test Conditions

- Output Load: See Fig. 1
- Input Rise and Fall Times ≦ 20 ns
- Input Pulse Levels: 0.45 V and 2.4 V
- Timing Measurement Reference Level
  Input: 0.8V and 2.0 V
  Output: 0.8 V and 2.0 V
- C_L in fig. 1. includes the floating capacitors of fig and probe.

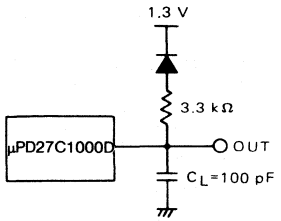
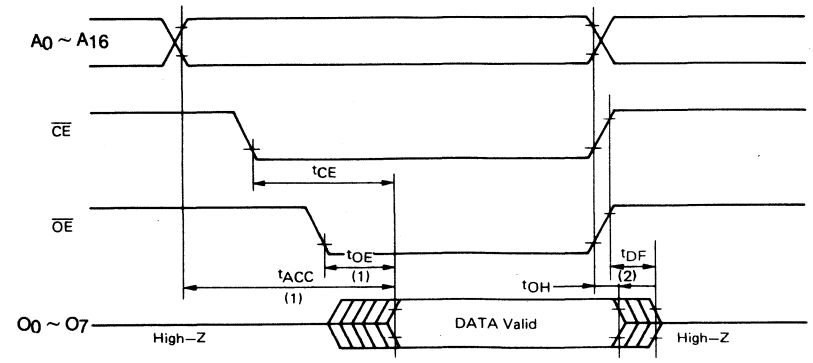


Fig. 1 Output Load

Capacitance (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

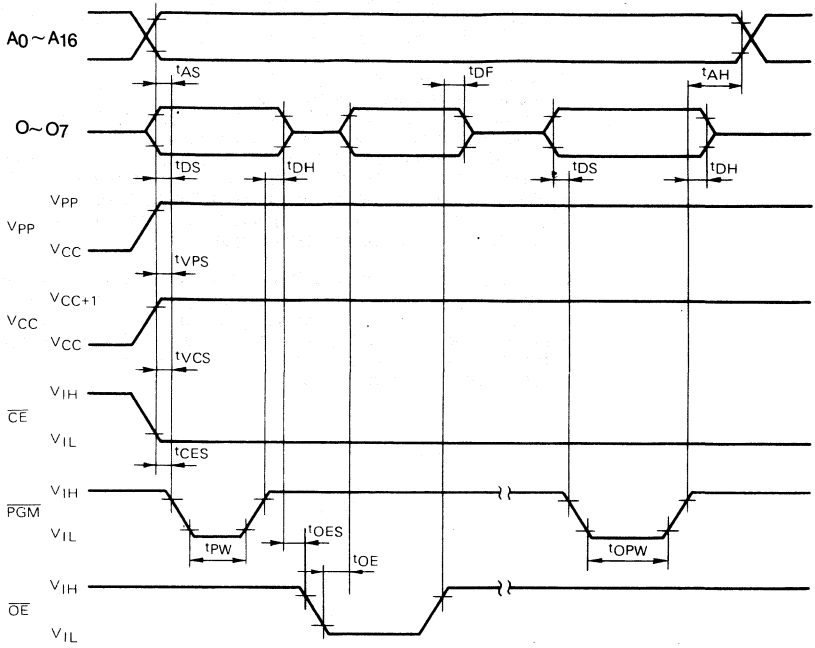
DC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400$ μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

AC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{OE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.095	0.1	0.105	ms	
Overprogram Pulse Width	t_{OPW}	0.38		0.42	ms	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
$\overline{OE}$ to Output Delay	t_{OE}			150	μs	

Programming Mode Timing



Notes : (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(2) V_{PP} must not be greater than +13.5 V including overshoot.

Programming Operation

μPD27C1000D is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C1000D is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{PGM}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL level.

Programming operation begins by addressing the first location, and valid appearing at the eight output pins. V_{CC} is then raised to +6 ± 0.25 V followed by V_{PP} raised to +12.5 ± 0.3 V. A $\overline{PGM}$ pulse of 0.1 ms ± 5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 0.1 ms $\overline{PGM}$ pulse is applied, to a maximum of 10 times. If the bit gets programmed within 10 efforts, another pulse of 0.4X ms for each effort is applied and the next address is applied. If the bit does not get programmed in 10 efforts, another pulse of 4 ms is applied. If the bit is programmed, the next address is applied until all addresses are complete.

When programming multiple μPD27C1000Ds in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C1000Ds may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at + 12.5 V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C1000D will inhibit it from being programmed.

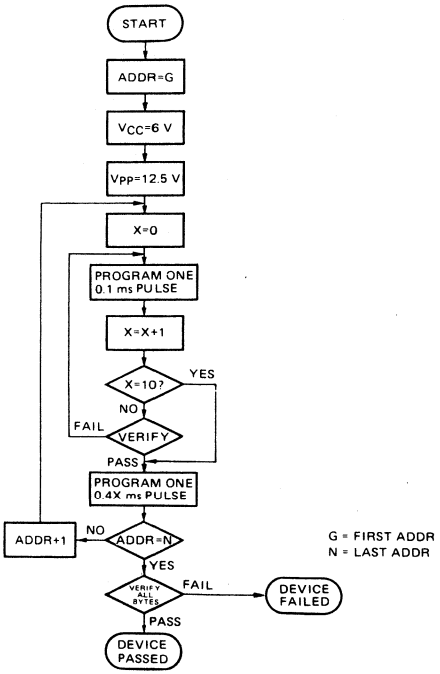


Fig. 2 Programming Flowchart

Erasure

Erasure of the μPD27C1000D programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27C1000D. Consequently, if the μPD27C1000D is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

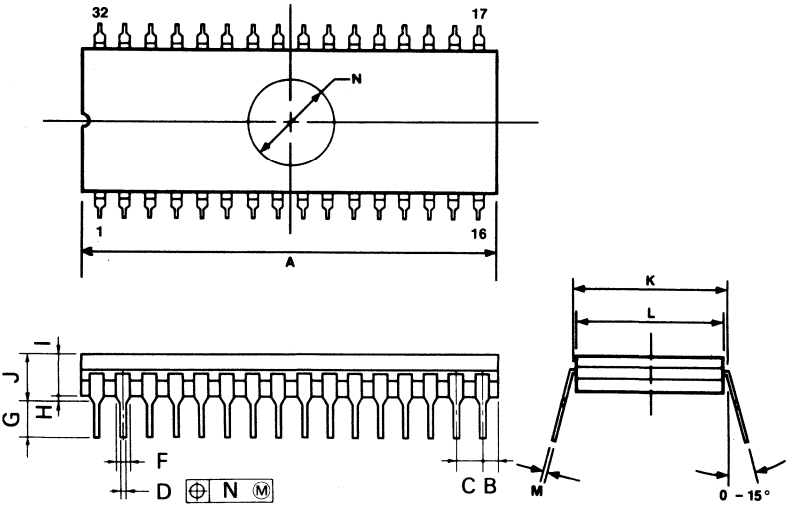
The recommended erasure procedure for the μPD27C1000D is exposure to ultraviolet light with wavelengths of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12 000 μW/cm^2 power rating. During erasure, the μPD27C1000D should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Package Dimensions

32 PIN CERAMIC DIP (600 mil)

μPD27C1000D

Item	Millimeters
A	43.18 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
F	1.2 min
G	3.5 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	14.66
M	.25 ± .05
N	8.89 dia



1048 576 BIT CMOS UV EPROM

Description

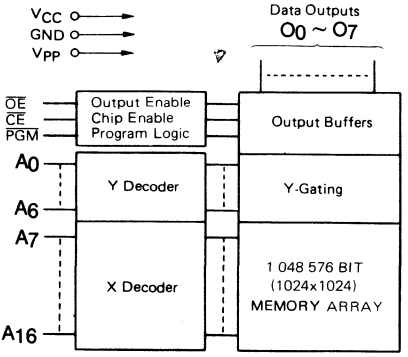
The μPD27C1001D is a 1 048 576 bits (131 072 x 8-bits) ultraviolet erasable and electrically programmable read-only memory (UV EPROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.

The μPD27C1001D is available in a standard 32-pin cerdip package with a quartz window.
It is pin compatible to JEDEC standard pin OUT.

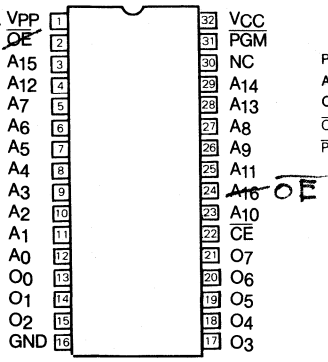
Features

- 131 072 words by 8-bits organization
- Ultraviolet erasable and electrically programmable
- Fast access time: 150 ns MAX. (μPD27C1001D-15)
  200 ns MAX. (μPD27C1001D-20)
  250 ns MAX. (μPD27C1001D-25)
- Low power dissipation: 50 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 32-pin DIP
- JEDEC standard pin out.

Block Diagram



Pin Configuration



PIN NAMES			
A0 ~ A16	Address	OE	Output Enable
O0 ~ O7	Data Outputs	VCC	Supply Voltage
CE	Chip Enable	VPP	Program Voltage
PGM	Program	GND	Ground
		NC	No Connection

MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output Desable	V_{IL}	V_{IH}	X	+5 V	+5 V	High-Z
Standby	V_{IH}	X	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	X	+12.5 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +80	°C
Storage Temperature	−65 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (Ag)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +13.5	V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP} = V_{CC}$			V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC}-0.7$			V	$I_{OH} = -100\ \mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 0 \sim V_{CC}$, $\overline{OE} = V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = 0 \sim V_{CC}$
V_{PP} Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0 \sim V_{CC}$

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C1001D-15		μPD27C1001D-20		μPD27C1001D-25		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

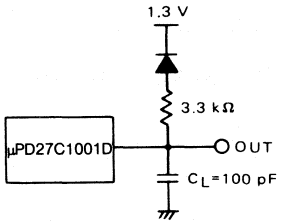


Fig. 1 Output Load

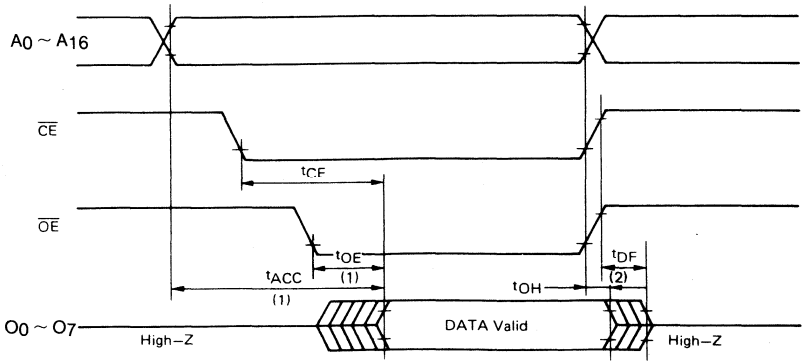
Test Conditions

- Output Load: See Fig. 1
- Input Rise and Fall Times ≦ 20 ns
- Input Pulse Levels: 0.45 V and 2.4 V
- Timing Measurement Reference Level
  Input: 0.8V and 2.0 V
  Output: 0.8 V and 2.0 V
- C_L in fig. 1. includes the floating capacitors of jig and probe.

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

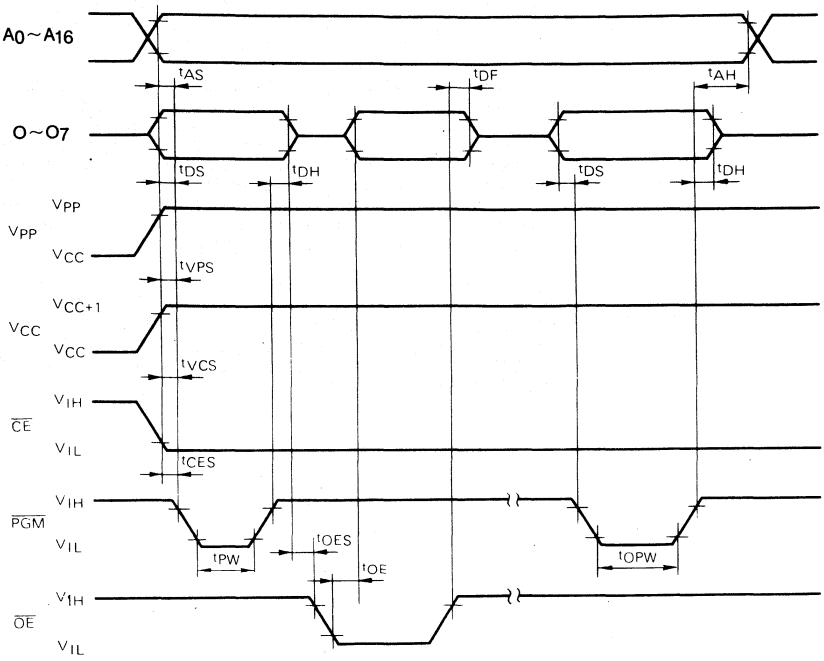
DC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400$ μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

AC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{OE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.095	0.1	0.105	ms	
Overprogram Pulse Width	t_{OPW}	0.38		0.42	ms	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
$\overline{OE}$ to Output Delay	t_{OE}			150	μs	

Programming Mode Timing



Notes : (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(2) V_{PP} must not be greater than +13.5 V including overshoot.

Programming Operation

μPD27C1001D is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C1001D is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{PGM}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL level.

Programming operation begins by addressing the first location, and valid appearing at the light output pins. V_{CC} is then raised to $+6 \pm 0.25$ V followed by V_{PP} raised to $+12.5 \pm 0.3$ V. A $\overline{PGM}$ pulse of 0.1 ms $\pm$ 5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 0.1 ms $\overline{PGM}$ pulse is applied, to a maximum of 10 times. If the bit gets programmed within 10 efforts, another pulse of 0.4X ms for each effort is applied and the next address is applied. If the bit does not get programmed in 10 efforts, another pulse of 4 ms is applied. If the bit is programmed, the next address is applied until all addresses are complete.

When programming multiple μPD27C1001Ds in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C1001Ds may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at + 12.5 V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C1001D will inhibit it from being programmed.

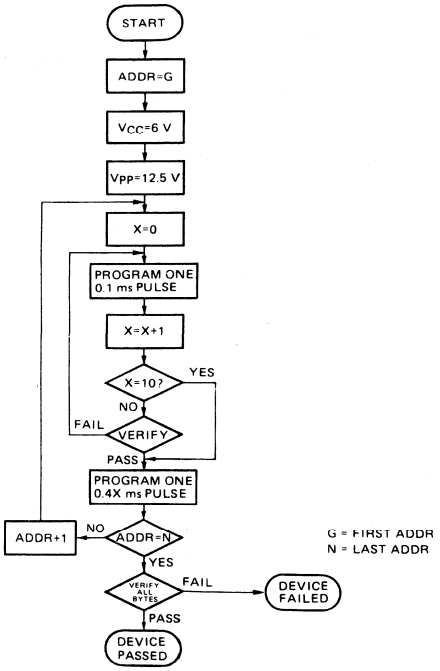


Fig. 2 Programming Flowchart

Erasure

Erasure of the μPD27C1001D programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27C1001D. Consequently, if the μPD27C1001D is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

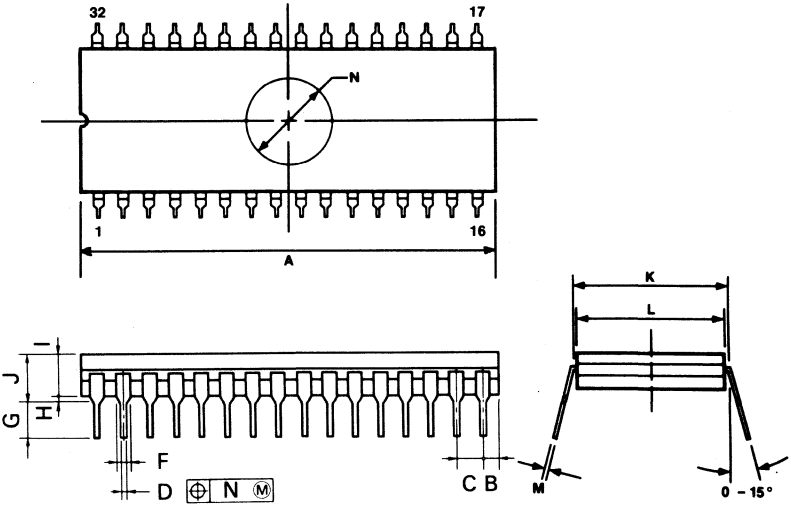
The recommended erasure procedure for the μPD27C1001D is exposure to ultraviolet light with wavelengths of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12 000 μW/cm^2 power rating. During erasure, the μPD27C1001D should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Package Dimensions

32 PIN CERAMIC DIP (600 mil)

μPD27C1001D

Item	Millimeters
A	43.18 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
F	1.2 min
G	3.5 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	14.66
M	.25 ± .05
N	8.89 dia



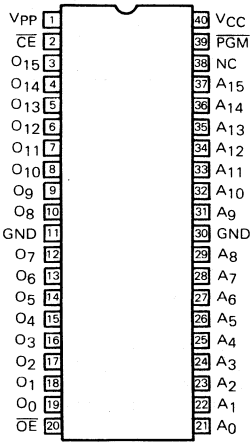
DESCRIPTION

The μPD27C1024D is a 1 048 576 bits (65 536 x 16-bits) ultraviolet erasable and electrically programmable readonly memory (UV EPROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C1024D is available in a standard 40-pin cerdip package with a quartz window.

FEATURES

- 65 536-words by 16-bits organization
- Ultraviolet erasable and electrically programmable
- Fast access time: 150 ns MAX. (μPD27C1024D–15)
  200 ns MAX. (μPD27C1024D–20)
  250 ns MAX. (μPD27C1024D–25)
- Low power dissipation: 50 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 40-pin DIP

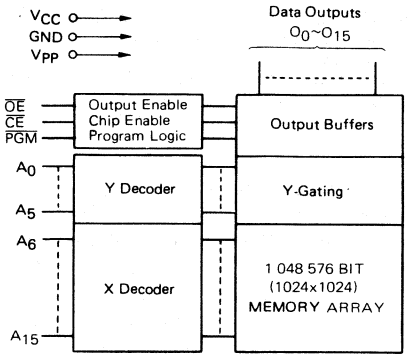
PIN CONFIGURATION



PIN NAMES

$A_0 \sim A_{15}$	Address	$\overline{OE}$	Output Enable
$O_0 \sim O_{15}$	Data Outputs	V_{CC}	Supply Voltage
$\overline{CE}$	Chip Enable	V_{PP}	Program Voltage
$\overline{PGM}$	Program	GND	Ground
		NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	O_0~O_{15}
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output Desable	V_{IL}	V_{IH}	X	+5 V	+5 V	High-Z
Standby	V_{IH}	X	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	X	+12.5 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +80	°C
Storage Temperature	−65 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (A_9)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +13.5	V

*COMMENT: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP} = V_{CC}$			V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC}-0.7$			V	$I_{OH} = -100\ \mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 0 \sim V_{CC}$, $\overline{OE} = V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = 0 \sim V_{CC}$
V_{PP} Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0 \sim V_{CC}$

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C1024D−15		μPD27C1024D−20		μPD27C1024D−25		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≦ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

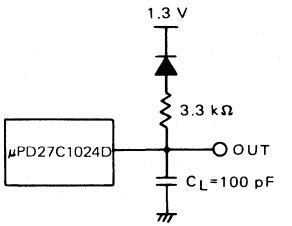
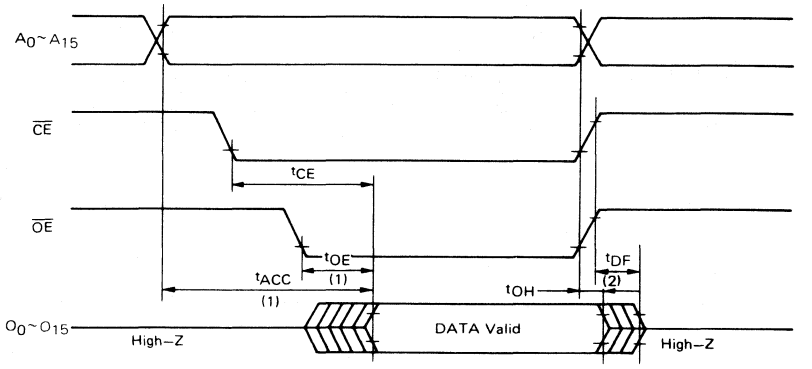


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

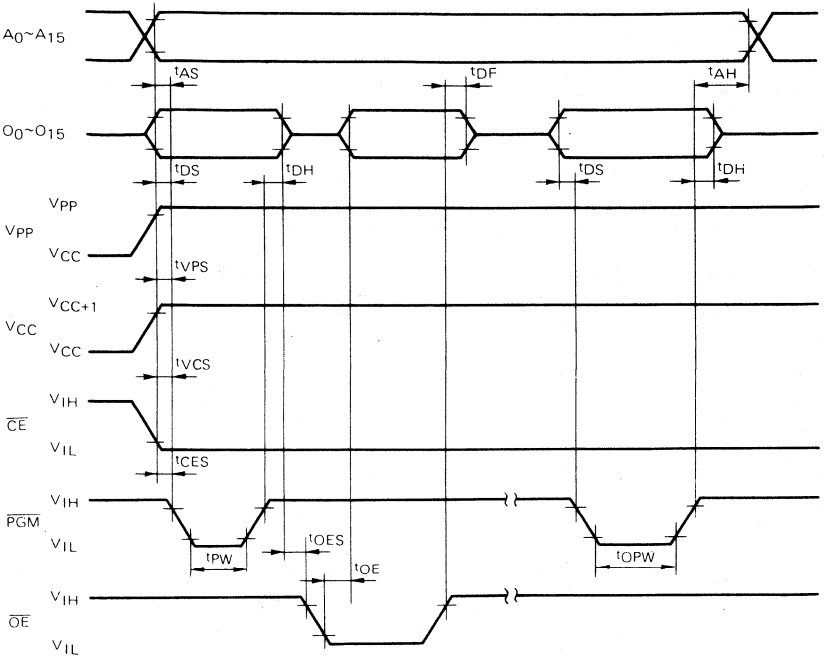
DC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, Vpp=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
V_{CC} Current	I_{CC}			30	mA	
Vpp Current	I_{PP}			100	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

AC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, Vpp=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{OE}$ to Output Float Time	t_{DF}	0		130	ns	
Vpp Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.095	0.1	0.105	ms	
Overprogram Pulse Width	t_{OPW}	0.38		0.42	ms	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
$\overline{OE}$ to Output Delay	t_{OE}			150	μs	

Programming Mode Timing



Notes : (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(2) V_{PP} must not be greater than +13.5 V including overshoot.

PROGRAMMING OPERATION

μPD27C1024D is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C1024D is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{PGM}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 16-bit parallel from at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the sixteen output pins. V_{CC} is then raised to +6±0.25V followed by V_{PP} raised to +12.5±0.3 V. A $\overline{PGM}$ pulse of 0.1 ms±5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 0.1 ms $\overline{PGM}$ pulse is applied, to a maximum of 10 times. If the bit gets programmed within 10 efforts, another pulse of 0.4X ms for each effort is applied and the next address is applied. If the bit does not get programmed in 10 efforts, another pulse of 4ms is applied. If the bit is programmed, the next address is applied until all addresses are complete.

When programming multiple μPD27C104Ds in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C1024Ds may be common. Programing is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at + 12.5 V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C1024D will inhibit it from being programmed.

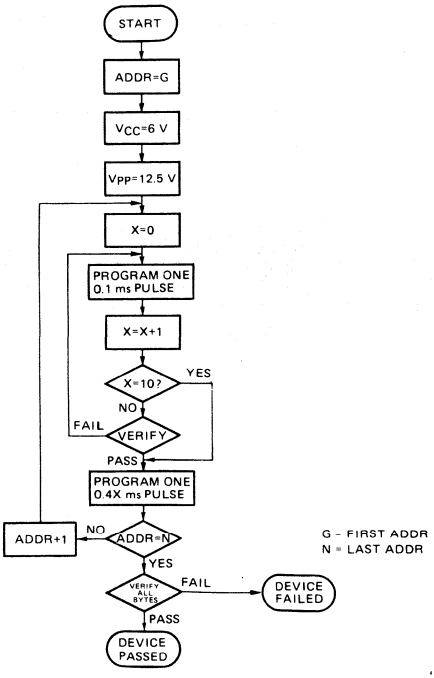


Fig. 2 Programming Flowchart

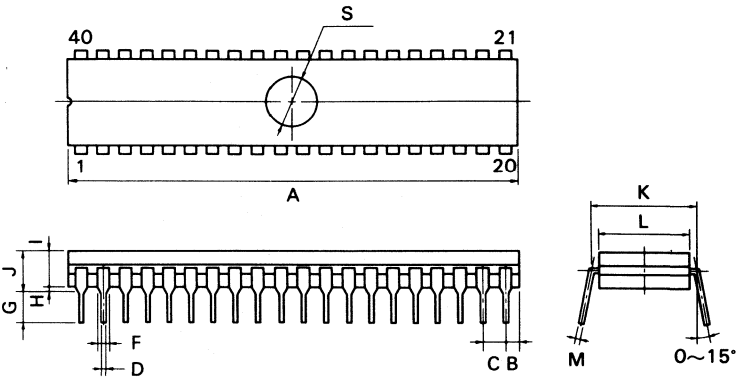
ERASURE

Erasure of the μPD27C1024D programmed data can be attained when exposed to light with wavelengths shorter than approximately 400 nm. It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27C1024D. Consequently, if the μPD27C1024D is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device. The recommended erasure procedure for the μPD27C1024D is exposure to ultraviolet light with wavelengths of 254 nm. The integrated dose (i.e., UV intensity X exposure time) for erasure should be not less than 15 Ws/cm². The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12.000 μW/cm² power rating. During erasure, the μPD27C1024D should be placed within 2.5 cm of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Package Dimensions

40 PIN Cerdip (600 mil)

ITEM	MILLIMETERS
A	53.34 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{\pm 0.10}$
F	1.2 MIN.
G	$3.5^{\pm 0.3}$
H	0.51 MIN.
I	3.80
J	5.08 MAX.
K	15.24 (T.P.)
L	14.66
M	$0.25^{\pm 0.05}$
N	0.25
S	ϕ 8.89



OTPROM
— CMOS —

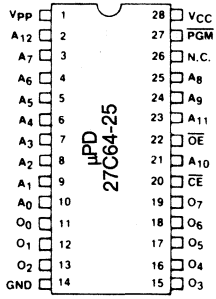
CMOS 65,536 (8 K x 8) BIT PROM

Features

- Electrically programmable
- Access time: 250ns max
- Single location programming
- Programmable with single pulse
- Low power dissipation: 40 mW/MHz (active)
  525 μW (standby)
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 28-pin DIP
- Three-state outputs
- Pin Compatible to 2764 EPROM
- CMOS Double-Polysilicon Technology

Pin Configuration

Top View



Package C

PIN NAMES

A_0-A_{12}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
N. C.	No Connect

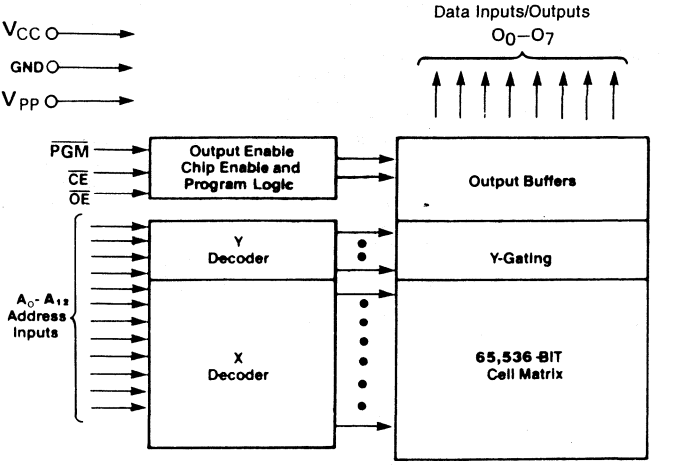
Mode Selection

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	V_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
High-Speed Programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}

X can be either V_{IL} or V_{IH}

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings

Operating Temperature	−10°C to +80°C
Storage Temperature	−55°C to + 125°C
Output Voltage	−0.6 to +7.0V
Input Voltage	−0.6 to + 7.0V
Supply Voltage V_{CC}	−0.6 to + 7.0V
Supply Voltage V_{PP}	−0.6 to + 22.0V

COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

READ MODE AND STANDBY MODE

T_a = 0°C to 70°C, V_{CC} = +5V ± 5 %, V_{PP} = V_{CC} ± 0.6V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Output Leakage Current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{CC}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0 ~ V_{CC}
V_{CC} Current (Active)	I_{CCA1}			10	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
V_{CC} Current (Standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}, V_{IN} = 0 ~ V_{CC}
V_{PP} Current	I_{PP1}		1	100	μA	V_{PP} = V_{CC} + 0.6V

DC Characteristics

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = −25°C to +70°C, V_{CC} = V_{CC} = +5V±10%, V_{PP} = V_{CC}

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	V_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC2}			30	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL}

AC Characteristics

READ MODE AND STANDBY MODE

$T_a = 0°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay	t_{ACC}			250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			250	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}	0		100	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Test Conditions

Output Load: See Fig. 1
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 to 2.4 V

Timing Measurement Reference Level:
Input: 0.8V and 2.0V
Output: 0.8V and 2.0V

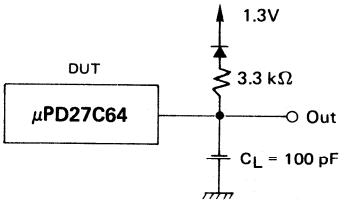


Fig. 1

CONVENTIONAL PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

$T_a = -25°C \pm +5°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = +21V \pm 0.5V$

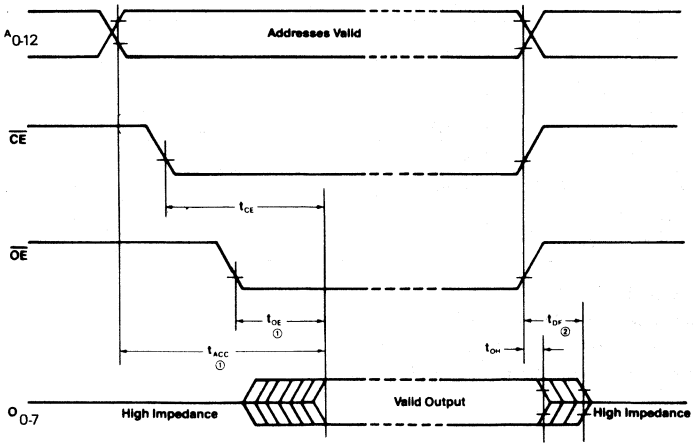
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Address Setup Time	t_{AS}	2			μs
$\overline{OE}$ Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	2			μs
$\overline{CE}$ Setup Time	t_{CES}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from $\overline{OE}$	t_{OE}			150	ns
Program Pulse Width	t_{PW}	20	50	55	ms
V_{PP} Setup Time	t_{VS}	2			μs

Test Condition

Input Pulse Levels = 0.45V to 2.4V
Input Timing Reference Level = 0.8V and 2.0V
Output Timing Reference Level = 0.8V and 2.0V
Input Rise and Fall Times: 20 ns

Timing Waveforms

READ MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DC Characteristics

HIGH-SPEED PROGRAMMING MODE

(T_a = −25±5°C, V_{CC} = +6±0.25V, V_{PP} = +21±0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		−0.1		0.8	V
Input Leakage Current	I_{LI}	$V_{IH} = V_{IL}$ or V_{IH}			10	μA
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
V_{CC} Current	I_{CC2}				30	mA
V_{PP} Current	I_{PP}	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC Characteristics

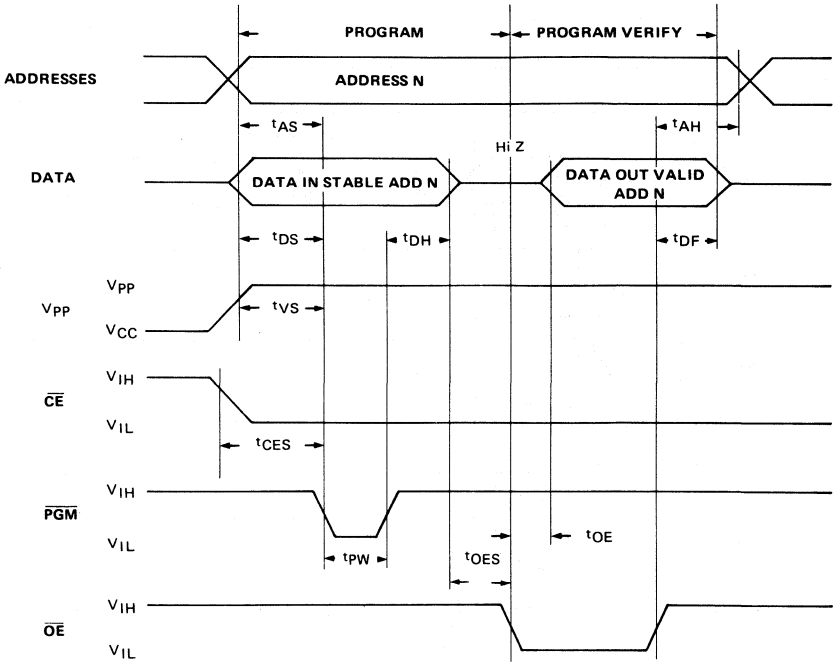
(T_a = 25 ± 5°C, V_{CC} = +6 ± 0.25V, V_{PP} = +21 ± 0.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	t_{AS}		2			μs
$\overline{OE}$ Setup Time	t_{OES}		2			μs
Data Setup Time	t_{DS}		2			μs
Address Hold Time	t_{AH}		2			μs
Data Hold Time	t_{DH}		2			μs
$\overline{CE}$ to Ouput Float Time	t_{DF}		0		130	ns
V_{PP} Setup Time	t_{VPS}		2			μs
V_{CC} Setup Time	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{OPW}		3.8		63	ms
$\overline{CE}$ Setup Time	t_{CES}		2			μs
Data Valid from $\overline{OE}$	t_{OE}				150	ns

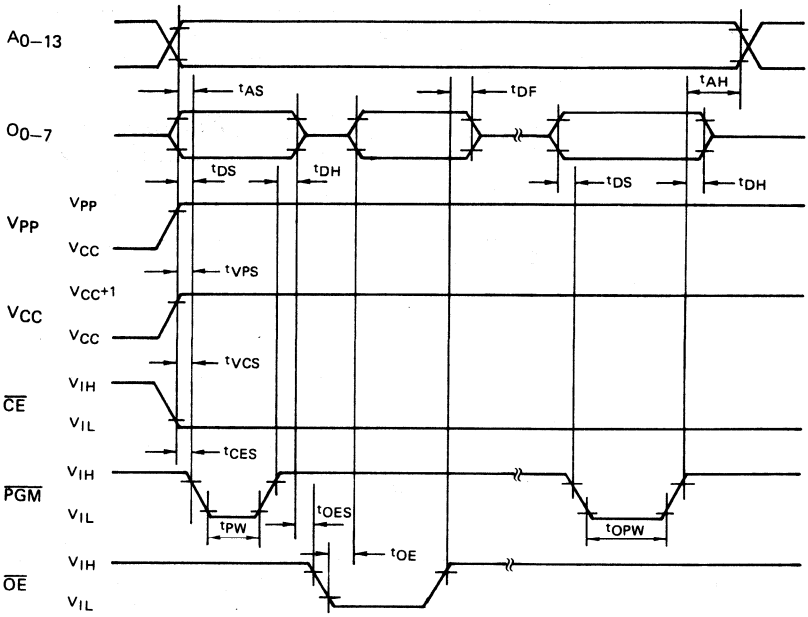
TEST CONDITIONS

- Input Pulse Levels: 0.45V and 2.0V
- Input Timing Reference Level: 0.8V and 2.0V
- Output Timing Reference Level: 0.8V and 2.0V

CONVENTIONAL PROGRAM MODE



High-speed Program Mode (3)



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

(3) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

FUNCTION The μPD27C64 operates from a single +5V power supply, making it ideal for microprocessor applications.

OPERATION The six operation modes of the μPD27C64 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for V_{PP} which is pulsed from TTL level to 21V.

READ MODE When $\overline{CE}$ and $\overline{OE}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE The μPD27C64 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced from 30 mA to 100 μA.

PROGRAMMING MODES The μPD27C64 can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventional mode basically a 50 ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm ™, in which up to fifteen 1 ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4 ms $\overline{PGM}$ pulse for each number of 1 ms pulse applied before. The high-speed programming mode reduces the programming time to 120 s typical.

CONVENTIONAL PROGRAMMING MODE Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD27C64 is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8 bit in parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD27C64s are connected in parallel, except for $\overline{CE}$, individual μPD27C64s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27C64 to be programmed.

Programming of multiple μPD27C64s in parallel with the same data is easily accomplished. All the like inputs are tied together and are programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

HIGH-SPEED PROGRAMMING MODE In this mode, programming begins by addressing the first location, and valid data appearing at the eight output pins (a low TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1 ms ± 5 % is then applied in the same manner as described in the program mode timing diagram. The bit is then verified and a program/no program desicion is made. If the bit is not programmed, another 1 ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4 ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is applied and the bit verified. If the bit is not programmed at this stage, the device is rejected as a failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage V_{CC} and V_{PP} pins are lowered to 5V ± 10 % and all bytes are then verified again for programming.

This algorithm is compatible with that of μPD27C64.

PROGRAMMING INHIBIT MODE

Programming multiple μPD27C64s in parallel with different data is easier with the program Inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C64s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with Vpp at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C64 will inhibit it from being programmed.

PROGRAM VERIFY MODE

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at high (1) level.

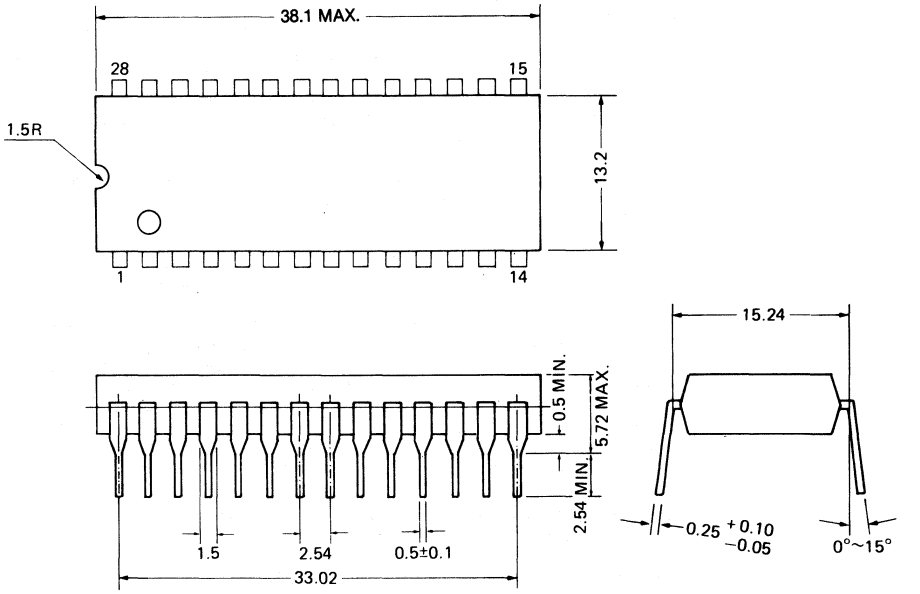
OUTPUT DISABLE

The data outputs of two or more μPD27C64s may be wire-O Red together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27C64s should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

TM: Intelligent Programming Algorithm is a registered trademark of Intel Coporation

Package Dimensions

Package Outline
μPD27C64 C (Plastic)



262 144 BIT CMOS ONE TIME PROM

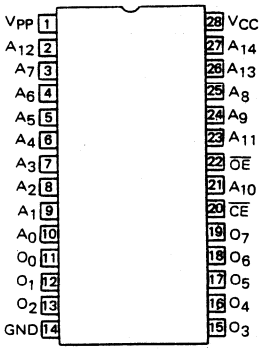
Description

The μPD27C256C is a 262 144 bit (32 768x8-bit) one time programmable read-only memory (OT PROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C256C is available in a standard 28-pin plastic package.

Features

- 32 768-words by 8-bit organization
- One time programmable
- Fast access time: 200 ns MAX. (μPD27C256C–20)
  250 ns MAX. (μPD27C256C–25)
- Low power dissipation: 30 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 28-pin DIP

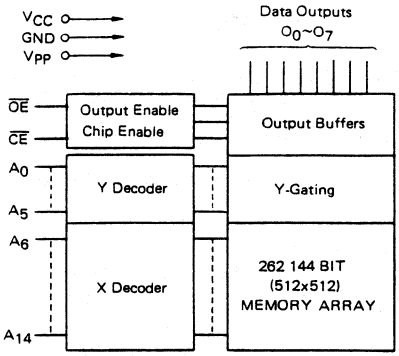
Pin Configuration



PIN NAMES

$A_0 \sim A_{14}$	Addresses
$O_0 \sim O_7$	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
V_{PP}	Program Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O_0~O_7
Read	V_{IL}	V_{IL}	+5 V	+5 V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	+5 V	+5 V	High-Z
Standby	V_{IH}	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	+21 V	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	+21 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	+21 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25 to +85	°C
Storage Temperature	−55 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage V_{PP}	−0.6 to +22	V

*COMMENT: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Notes: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(2) V_{PP} must not be greater than +13.5 V including overshoot.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	μPD27C256C-20/-25			UNIT
		MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP} = V_{CC}$			V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC}-0.7$			V	$I_{OH} = -100\ \mu A$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 0 \sim V_{CC}$, $\overline{OE} = V_{IH}$
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = 0 \sim V_{CC}$
V_{PP} Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
	I_{CCA2}			30	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0 \sim V_{CC}$

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C256C-20		μPD27C256C-25		UNIT	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≤ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

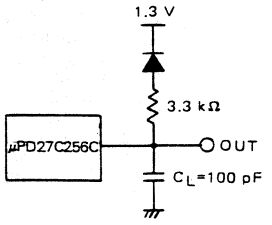
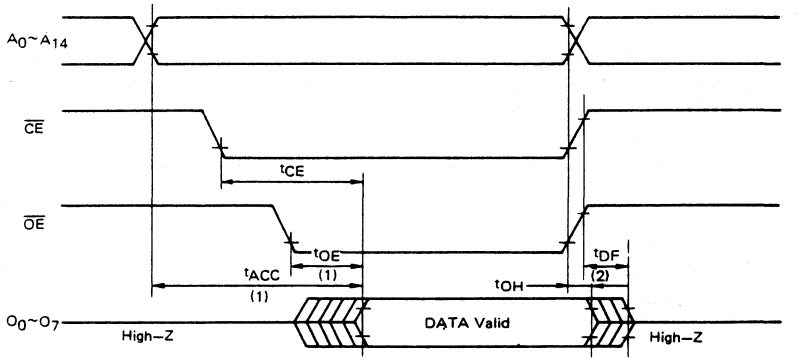


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING OPERATION

μPD27C256C is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C256C is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8-bit parallel from at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight output pins. V_{CC} is then raised to +6±0.25 V followed by V_{PP} raised to +21±0.5V. A $\overline{CE}$ pulse of 1 ms±5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 20 times. If the bit gets programmed within 20 efforts, another pulse of 1 ms for each effort is applied and the next address is applied. If the bit does not get programmed in 20 efforts, another $\overline{CE}$ pulse of 20 ms is applied and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to +5 V±5% and all bytes are then verified again for programming. When programming multiple μP27C256Cs in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel μPD27C256Cs may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ of the other μPD27C256C will inhibit it from being programmed.

DC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=21±0.5 V)

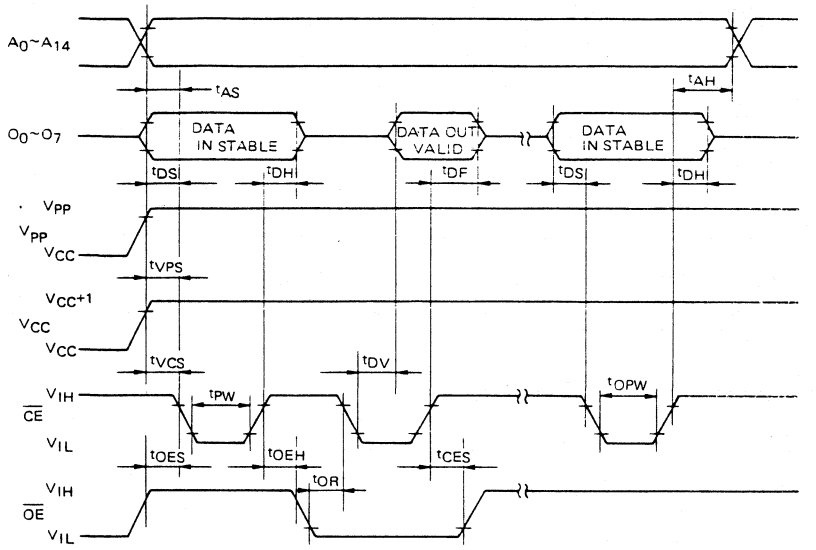
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400$ μA
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$

AC CHARACTERISTICS (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=21±0.5 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	0.95		21.0	ms	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
$\overline{CE}$ to Output Delay	t_{DV}			1	μs	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{OE}$ Hold Time	t_{OEH} *	2			μs	
$\overline{OE}$ Recovery Time	t_{OR} *	2			μs	

* $t_{OEH} + t_{OR} \geq 50$ μs

Programming Mode Timing

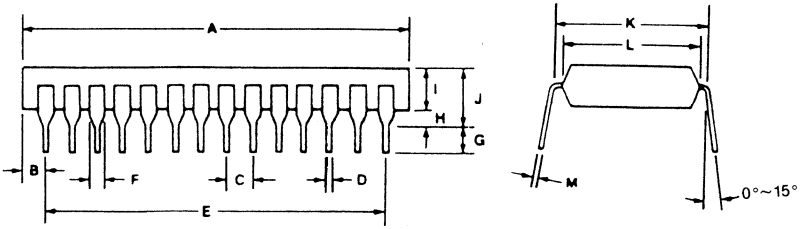


Notes : (1) V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
(2) Vpp must not be greater than +22 V including overshoot.

Package Dimensions

28 PIN Plastic DIP (600 mil)

Item	Millimeters
A	38.0 max.
B	2.49
C	2.54
D	0.5±0.1
E	33.02
F	1.5
G	2.54 min.
H	0.5 min.
I	4.31 max.
J	5.72 max.
K	15.24
L	13.2
M	$0.25^{+0.01}_{-0.05}$



262 144 BIT CMOS ONE TIME PROM

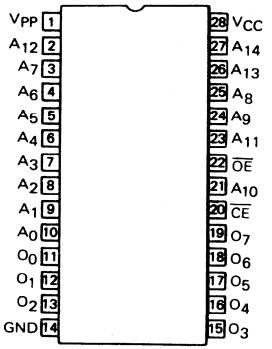
Description

The μPD27C256AC/AG is a 262 144 bit (32 768 x 8-bit) one time programmable read-only memory (OTPROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C256AC is available in a standard 28-pin plastic package.
The μPD27C256AG is available in a standard 28-pin mini-flat package.

Features

- 32 768-words by 8-bit organization
- One time programmable
- Fast access time: 150 ns MAX. (μPD27C256AC/AG-15)
  200 ns MAX. (μPD27C256AC/AG-20)
- Low power dissipation: 30 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 28-pin DIP
- 28-pin mini-flat package

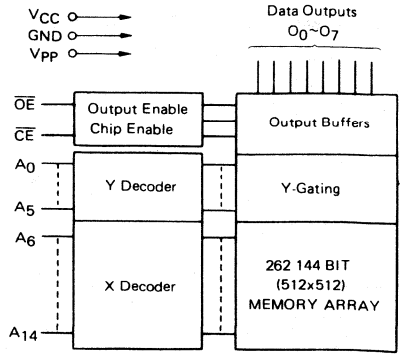
Pin Configuration



PIN NAMES

$A_0 \sim A_{14}$	Addresses
$O_0 \sim O_7$	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
V_{PP}	Program Voltage
GND	Ground

Block Diagram



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O_0~O_7
Read	V_{IL}	V_{IL}	+5 V	+5 V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	+5 V	+5 V	High-Z
Standby	V_{IH}	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	+12.5 V	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25 to +85 °C
Storage Temperature	−55 to +125 °C
Output Voltage	−0.6 to +7 V
Input Voltage	−0.6 to +7 V
Input Voltage (Ag)	−0.6 to +13.5 V
Supply Voltage V_{CC}	−0.6 to +7 V
Supply Voltage V_{PP}	−0.6 to +13.5 V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Supply Voltage V_{PP}	V_{PP}	$V_{PP}=V_{CC}$			V
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Ambient Temperature	T_a	0	–	70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC}−0.7			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 0~V_{CC}, $\overline{OE}$ = V_{IH}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0~V_{CC}
V_{PP} Current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
	I_{CCA2}			30	mA	f = 5 MHz, I_{OUT} = 0 mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}, V_{IN} = 0~V_{CC}

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C256AC/AG-15		μPD27C256AC/AG-20		UNIT	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		75		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	60	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≤ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

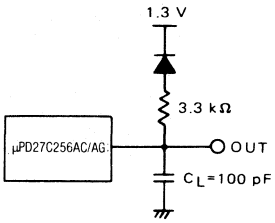
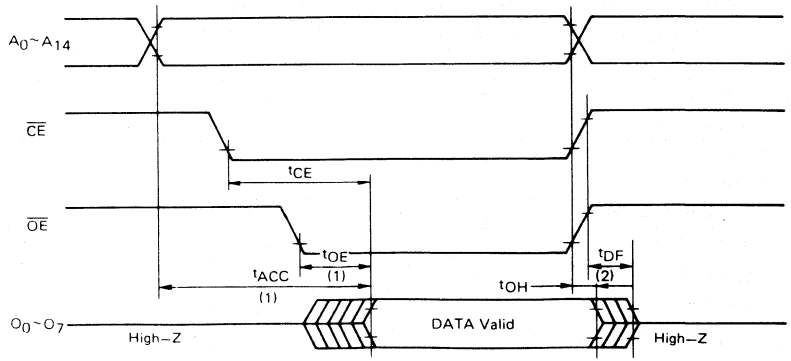


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Programming Operation

μPD27C256AC/AG is shipped with all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C256AC/AG is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with V_{PP} at +12.5 V. The data to be programmed is applied to the output pins in 8-bit parallel from at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight output pins. V_{CC} is then raised to $+6 \pm 0.25$ V followed by V_{PP} raised to $+12.5 \pm 0.3$ V. A $\overline{CE}$ pulse of 1 ms ± 5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 25 times. If the bit gets programmed within 25 efforts, another pulse of 3 ms for each effort is applied and the next address is applied until all addresses are complete. If the bit does not get programmed in 25 efforts, the device would be rejected as a program failure.

At this stage, V_{CC} and V_{PP} pins are lowered to +5 V ± 10% and all bytes are then verified again for programming.

When programming multiple μPD27C256AC/AGs in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel μPD27C256AC/AGs may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with V_{PP} at +12.5 V. A high (1) level applied to the $\overline{CE}$ of the other μPD27C256AC/AG will inhibit it from being programmed.

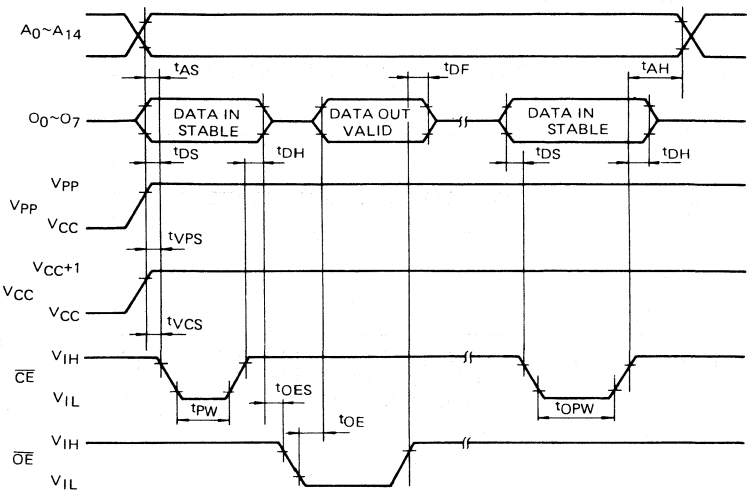
DC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = − 400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$

AC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{PP} Setup Time	t_{VPS}	2			μs	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	2.85		78.75	ms	
$\overline{OE}$ to Output Delay	t_{OE}			150	ns	

Programming Mode Timing

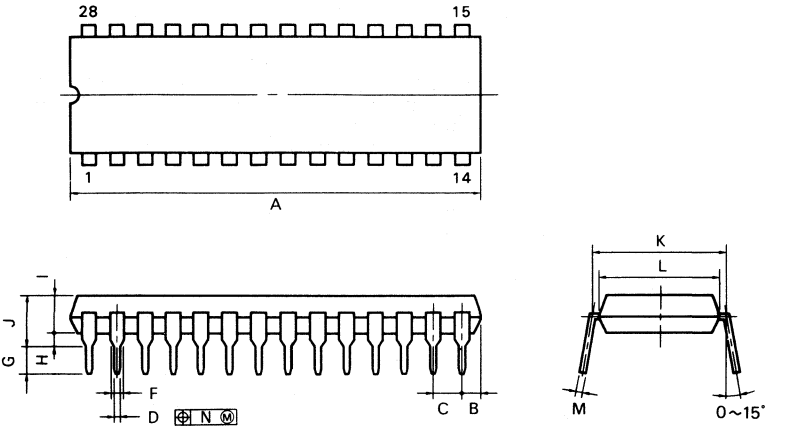


Notes : (1) V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
(2) Vpp must not be greater than +13 V including overshoot.

Package Dimensions

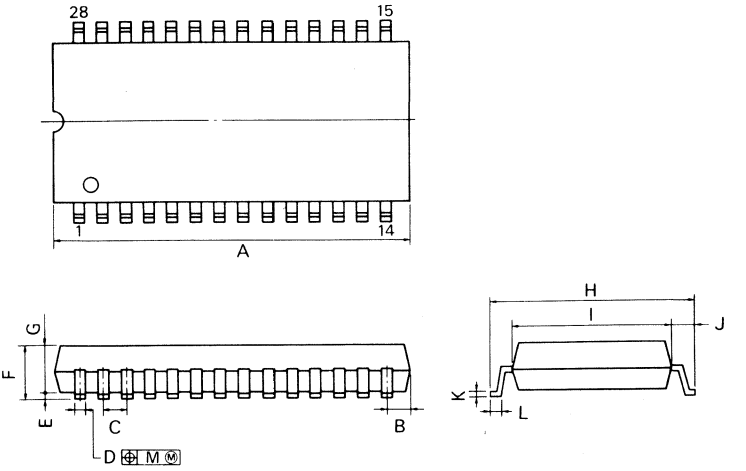
28 PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{+0.10}$
F	1.2 MIN.
G	$3.6^{\pm 0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25



28 PIN MINI FLAT PACKAGE

ITEM	MILLIMETERS
A	19.05 MAX.
B	1.27 MAX.
C	1.27 (T.P.)
D	$0.40^{\pm 0.1}$
E	$0.1^{+0.2}_{-0.1}$
F	2.5 MAX.
G	2.00
H	$11.8^{\pm 0.3}$
I	8.4
J	1.7
K	$0.15^{+0.10}_{-0.05}$
L	$0.7^{\pm 0.2}$
M	0.12



524 288 BIT CMOS ONE TIME PROM

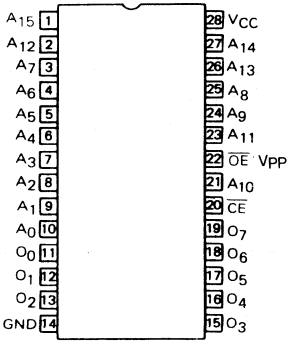
Description

The μPD27C512C is a 524 288 bits (65 536 x 8-bits) one time programmable read-only memory (OT PROM). It operates from a single +5 V power supply, making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes by using a low power supply system.
The μPD27C512C is available in a standard 28-pin plastic package.

Features

- 65 536-words by 8-bits organization
- One time programmable
- Fast access time: 200 ns MAX. (μPD27C512C-20)
  250 ns MAX. (μPD27C512C-25)
- Low power dissipation: 30 mA MAX. active current
  100 μA MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- 28-pin DIP

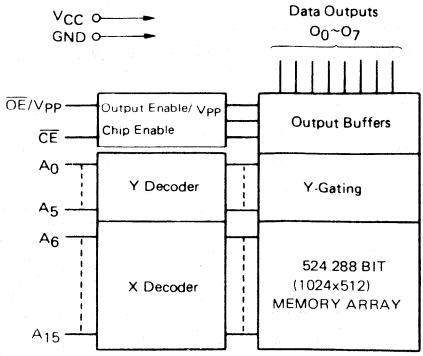
Pin Configuration



PIN NAMES

$A_0 \sim A_{15}$	Addresses
$O_0 \sim O_7$	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/ V_{PP}	Output Enable/V_{PP}
V_{CC}	Supply Voltage
GND	Ground

Block Diagram



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	O_0~O_7
Read	V_{IL}	V_{IL}	+5 V	D_{OUY}
Output Desable	V_{IL}	V_{IH}	+5 V	High-Z
Standby	V_{IH}	X	+5 V	High-Z
Program	V_{IL}	V_{IH}	+6 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	+6 V	D_{OUT}
Program Inhibit	V_{IH}	X	+6 V	High-Z

X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +80	°C
Storage Temperature	−65 to +125	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (A9)	−0.6 to +13.5	V
Supply Voltage V_{CC}	−0.6 to +7	V
Supply Voltage Vpp	−0.6 to +13.5	V

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditons for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	T_a	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC}−0.7			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 0~V_{CC}, $\overline{OE}$ = V_{IH}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0~V_{CC}
V_{CC} Current (active)	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
	I_{CCA2}			30	mA	f = 5 MHz, I_{OUT} = 0 mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}, V_{IN} = 0~V_{CC}

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD27C512C-20		μPD27C512C-25		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$/V_{PP} = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		200		250	ns	$\overline{OE}$/V_{PP} = V_{IL}
$\overline{OE}$/V_{PP} to Output Delay	t_{OE}		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$/V_{PP} High to Output Float	t_{DF}	0	60	0	85	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$/V_{PP} = V_{IL}

TEST CONDITIONS

- Output Load : See Fig. 1
- Input Rise and Fall Times ≤ 20 ns
- Input Pulse Levels : 0.45 V and 2.4 V
- Timing Measurement Reference Level
  - Input : 0.8 V and 2.0 V
  - Output : 0.8 V and 2.0 V

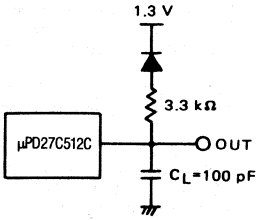
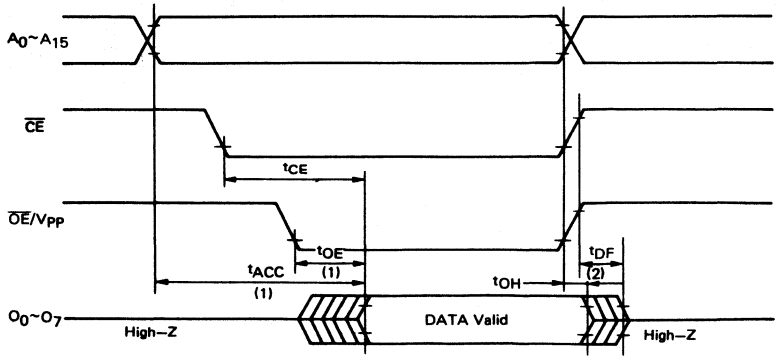


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN1}		4	6	pF	V_{IN} = 0 V
	C_{IN2}		12	20	pF	$\overline{OE}$/V_{PP}, V_{IN} = 0 V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Read Mode Timing



Notes : (1) $\overline{OE}$/V_{PP} may be delayed up to t_{ACC}−t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$/V_{PP} or $\overline{CE}$, whichever occurs first.

Programming Operation

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location. The μPD27C512C is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ with $\overline{OE}/V_{PP}$ at +12.5 V. The data to be programmed is applied on the output pins in 8-bit parallel from at TTL level.

Programming operation begins by addressing the first location, and valid data appearing at the eight output pins. V_{CC} is then raised to $+6 \pm 0.25$ V followed by $\overline{OE}/V_{PP}$ raised to $+12.5 \pm 0.3$ V. A $\overline{CE}$ pulse of 1 ms ± 5% is applied and the bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1 ms $\overline{CE}$ pulse is applied, to a maximum of 25 times. If the bit gets programmed within 25 efforts, another pulse of 3 ms for each effort is applied and the next address is applied. If the bit does not get programmed in 25 efforts, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to $+5 \text{ V} \pm 5\%$ and all bytes are then verified again for programming.

When programming multiple μPD27C512Cs in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ all like inputs (including $\overline{OE}/V_{PP}$) of the parallel μPD27C512Cs may be common. Programming is accomplished by applying a low (0) TTL level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +12.5 V. A high (1) level applied to the $\overline{CE}$ of the other μPD27C512C will inhibit it from being programmed.

DC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

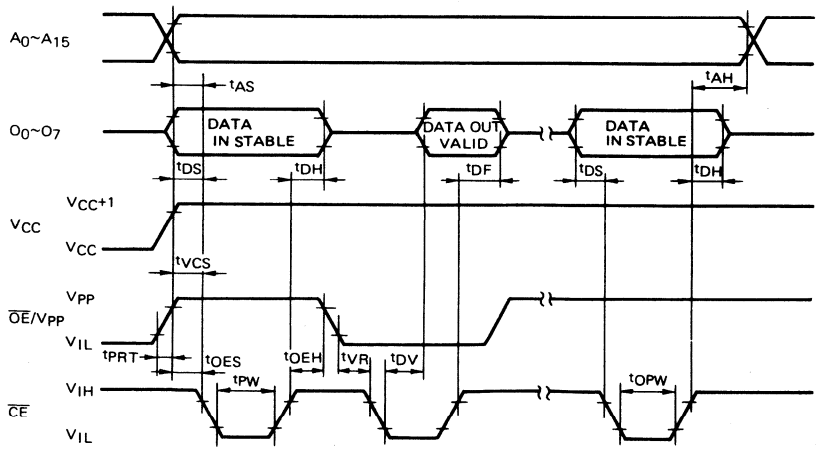
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			30	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{IH}$

AC Characteristics (T_a=25±5 °C, V_{CC}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$/V_{PP} Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
$\overline{CE}$ to Output Float Time	t_{DF}	0		130	ns	
V_{CC} Setup Time	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram Pulse Width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ to Output Delay	t_{DV}			1	μs	$\overline{CE}$ = $\overline{OE}$/V_{PP} = V_{IL}
$\overline{OE}$/V_{PP} Hold Time	t_{OEH} *	2			μs	
$\overline{OE}$/V_{PP} Recovery Time	t_{VR} *	2			μs	
$\overline{OE}$/V_{PP} Rise Time	t_{PRT}	50			ns	

* $t_{OEH} + t_{VR} \geqq 50$ μs

Programming Mode Timing

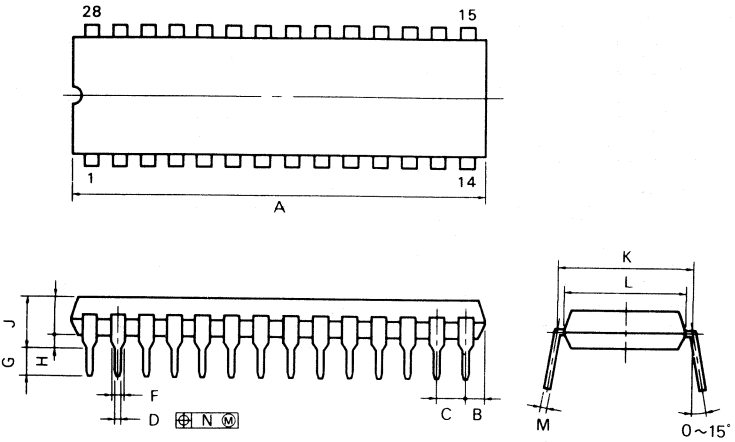


Notes : (1) V_{CC} must be applied simultaneously or before $\overline{OE}$/V_{PP} and removed simultaneously or after $\overline{OE}$/V_{PP}.
(2) V_{PP} must not be greater than +13 V including overshoot.

Package Dimensions

28 PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{+0.10}$
F	1.2 MIN.
G	$3.6^{+0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25



EE PROM
– CMOS –

65 536 BIT CMOS EE PROM

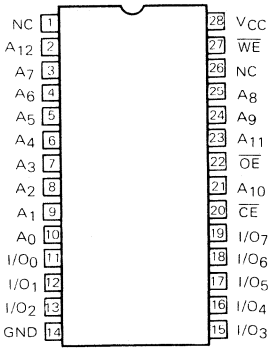
Description

The μPD28C64C and μPD28C64D are a 65 536 bit (8192 x 8 bit) electrically erasable programmable read-only memory (EE PROM). Operating from a full +5 V single power supply, the μPD28C64C and μPD28C64D provide a $\overline{\text{DATA}}$ polling function, which indicates the precise end of write cycles to the external world, and addition functions include chip erase, auto erase and programming, and 32-byte page write operations.
The EE PROM is available in a standard 28-pin DIP enclosure.

Features

- Single +5 V Power Supply
- Fast Access Time: 250 ns MAX. μPD28C64C-25, μPD28C64D-25
  300 ns MAX. μPD28C64C-30, μPD28C64D-30
- Low Power Dissipation: 20 mA MAX. Active Current
  100 μA MAX. Standby Current
- Chip Erase Mode
- Auto Erase and Programming Mode: 10 ms MAX.
- Page Programming Mode: 32-byte
- Endurance: 10 000 cycles
- $\overline{\text{DATA}}$ Polling Verification
- Silicon Signature
- 28-pin DIP

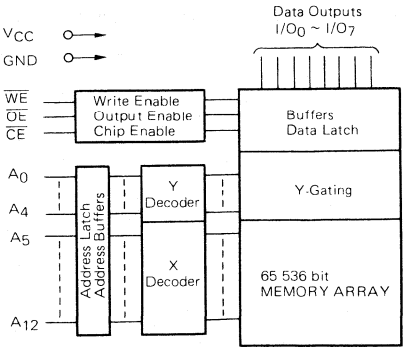
Pin Configuration



PIN NAMES

$A_0 \sim A_{12}$	Addresses
$I/O_0 \sim I/O_7$	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
GND	Ground
NC	Not Connect

Block Diagram



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 \sim I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN}=V_{IH}$
Write Inhibit	X	V_{IL}	X	—
	X	X	V_{IH}	

X can be either V_{IL} or V_{IH} V_{IHH}: +15 V ±0.5 V

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10 to +85	°C
Storage Temperature	−65 to +150	°C
Output Voltage	−0.6 to +7	V
Input Voltage	−0.6 to +7	V
Input Voltage (A_9)	−0.6 to +13.5	V
Input Voltage ($\overline{OE}$)	−0.6 to +16.5	V
Supply Voltage V_{CC}	−0.6 to +7	V

*COMMENT: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Ambient Temperature	T_a	0	–	70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	$V_{CC}-0.7$			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = V_{CC}$ MAX.
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{CC}$ MAX.
V_{CC} Current (active)	I_{CCA1}			20	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz, I_{OUT} = 0 mA
V_{CC} Current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}			100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0 \sim V_{CC}$

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	μPD28C64C–25 μPD28C64D–25		μPD28C64C–30 μPD28C64D–30		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	t_{ACC}		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		250		300	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		100		120	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ High to Output Float	t_{DF}	0	80	0	105	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

TEST CONDITIONS

- Output Load: See Fig. 1
- Input Rise and Fall Times ≦ 20 ns
- Input Pulse Levels: 0.45 V and 2.4 V
- Timing Measurement Reference Level
  Input : 0.8 V and 2.0 V
  Output : 0.8 V and 2.0 V

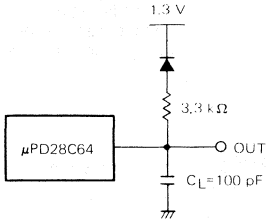
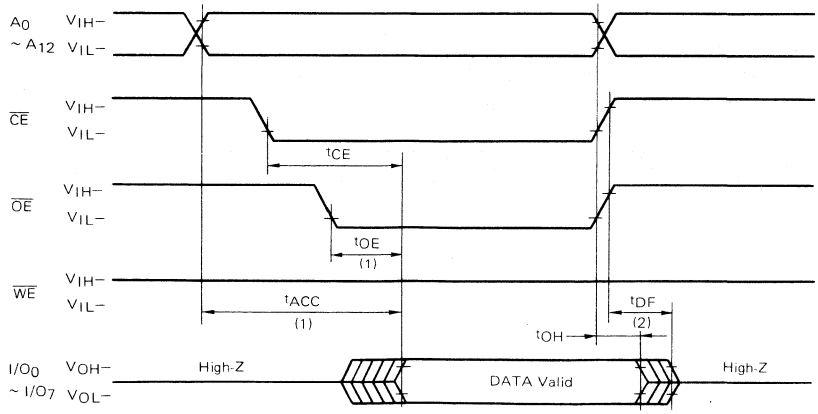


Fig. 1 Output Load

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		7	12	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}			10	pF	V_{OUT} = 0 V

Read Mode Timing



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Write Operation

Byte Write Mode

Low levels on $\overline{CE}$, $\overline{WE}$ and a high level on $\overline{OE}$ places the μPD28C64C and μPD28C64D in the write mode. The μPD28C64C and μPD28C64D permit $\overline{CE}$ and $\overline{WE}$ to control write cycles. An address is latched at the trailing edge of $\overline{CE}$ or $\overline{WE}$ whichever is the later, and data is latched at the leading edge of $\overline{CE}$ or $\overline{WE}$ whichever is the earlier. Auto erase and programming are both completed within a write cycle time (t_{WC}) of 10 ms.

Page Write Mode

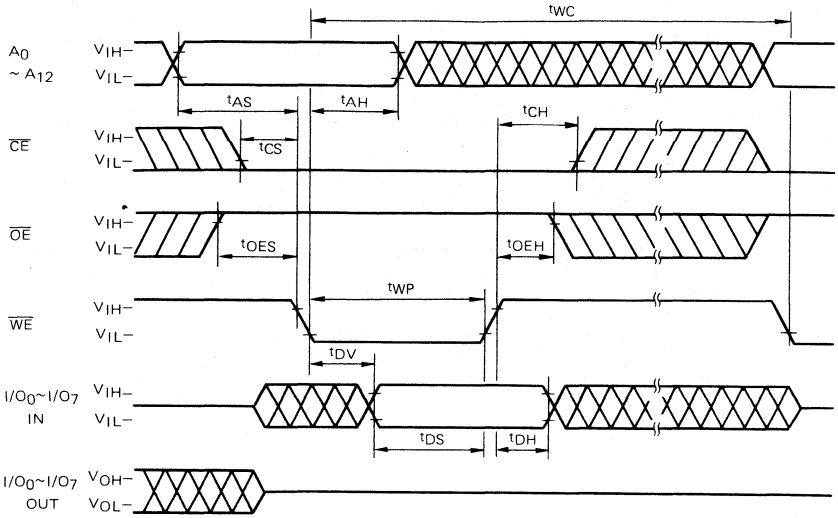
The μPD28C64C and μPD28C64D permit 32-byte page write operations by using its internal data address circuit. In page write, writing to all bytes is completed in 3 seconds. The μPD28C64C and μPD28C64D are organized into 256 pages by 32 byte. To use the page write mode, pages are first specified at addresses A_5 to A_{12}. Once pages have been thus specified, data can be written to them sequentially or randomly via addresses A_0 to A_4. Auto erase and programming starts internally if the next address is not input within a byte load cycle time of 10 μs. Pages cannot be changed in the middle of a write cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

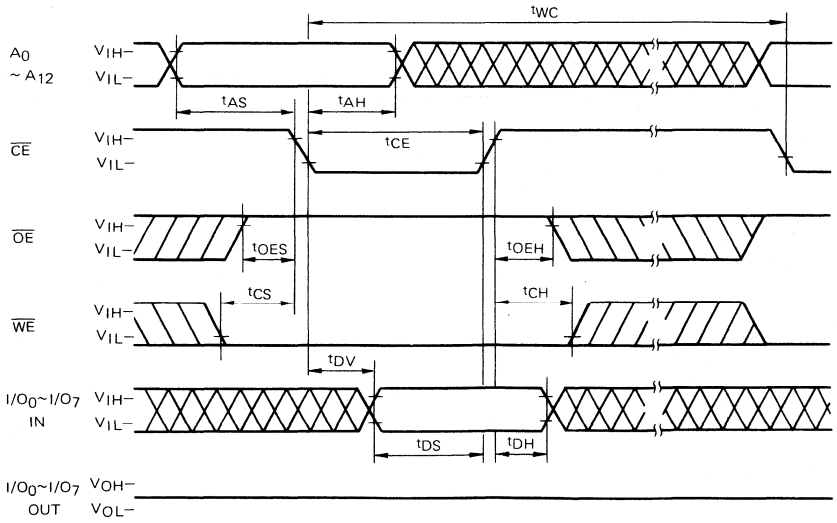
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Write Cycle Time	t_{WC}	10			ms	
Address Setup Time	t_{AS}	10			ns	
Address Hold Time	t_{AH}	200			ns	
Write Setup Time	t_{CS}	0			ns	
Write Hold Time	t_{CH}	0			ns	
$\overline{CE}$ Pulse Width	t_{CW}	150			ns	
$\overline{OE}$ High Setup Time	t_{OES}	10			ns	
$\overline{OE}$ High Hold Time	t_{OEH}	10			ns	
$\overline{WE}$ Pulse Width	t_{WP}	150			ns	
$\overline{WE}$ High Hold Time	t_{WPH}	50			ns	
Data Valid	t_{DV}			300	ns	
Data Setup Time	t_{DS}	100			ns	
Data Hold Time	t_{DH}	20			ns	
Byte Load Cycle	t_{BLC}	3		100	μs	

Write Mode Timing

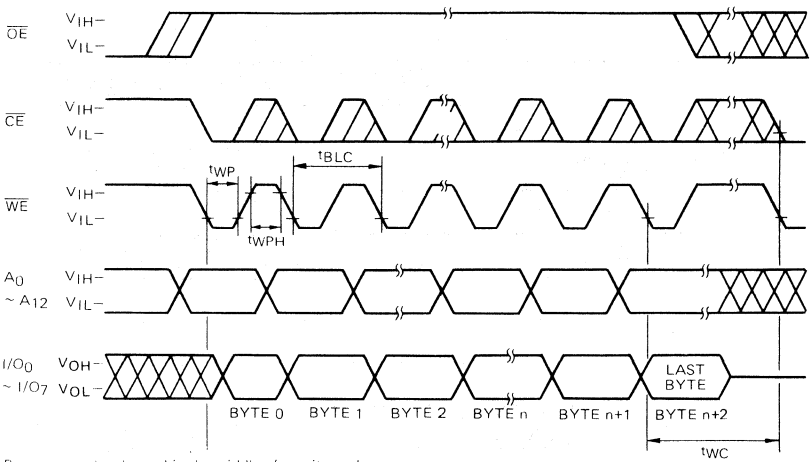
$\overline{WE}$ Controlled Write Timing



$\overline{CE}$ Controlled Write Timing



Page Mode Write Timing



Pages cannot be changed in the middle of a write cycle.

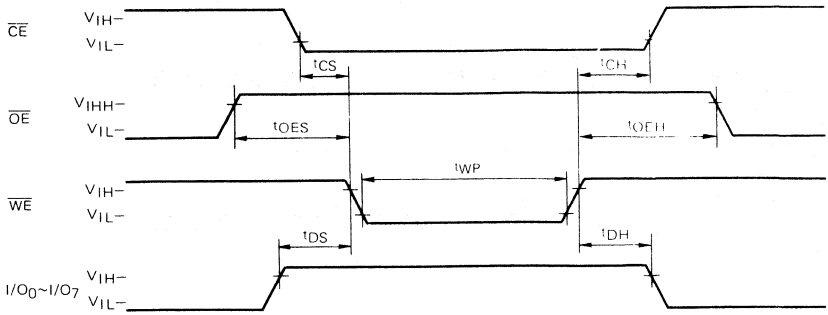
CHIP ERASE OPERATION

When $\overline{CE}$ and $\overline{WE}$ are made low with $\overline{OE}=V_{IHH}$ (12 to 15 V), the μPD28C64C and μPD28C64D are placed in the chip erase mode. In this mode, apply a high level to all of the data input I/O_0–I/O_7. The address input is labeled, don't care.

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
$\overline{CE}$ Setup Time	t_{CS}	500			ns	
$\overline{OE}$ Setup Time	t_{OES}	500			ns	
Data Setup Time	t_{DS}	500			ns	
Data Hold Time	t_{DH}	100			ns	
$\overline{WE}$ Pulse Width	t_{WP}	10			ms	
$\overline{CE}$ Hold Time	t_{CH}	5			μs	
$\overline{OE}$ Hold Time	t_{OEH}	$t_{CH}+3$			μs	

Chip Erase Mode Timing



DATA Polling

The μPD28C64C and μPD28C64D $\overline{DATA}$ polling function provide software indications of the end of byte write and page write cycles. While the EE PROM is in a write cycle, the data at the address which was last written externally by the CPU in the EE PROM read cycle, is read and compared with the true data (for example, write data = 1xxx xxxx), and its inverted data (read data = 0xxx xxxx) is output to I/O_7. The expected data value is output at the end of the write cycle and matched with the true data value.

WRITE PROTECT FUNCTIONS

The μPD28C64C and μPD28C64D provide the following three functions to prevent invalid data write operations:

Noise prevention

Writing is inhibited when the $\overline{WE}$ pulse is 20 ns or less.

Supply voltage V_{CC} level detection

Writing is inhibited when supply voltage V_{CC} is 3 V or lower.

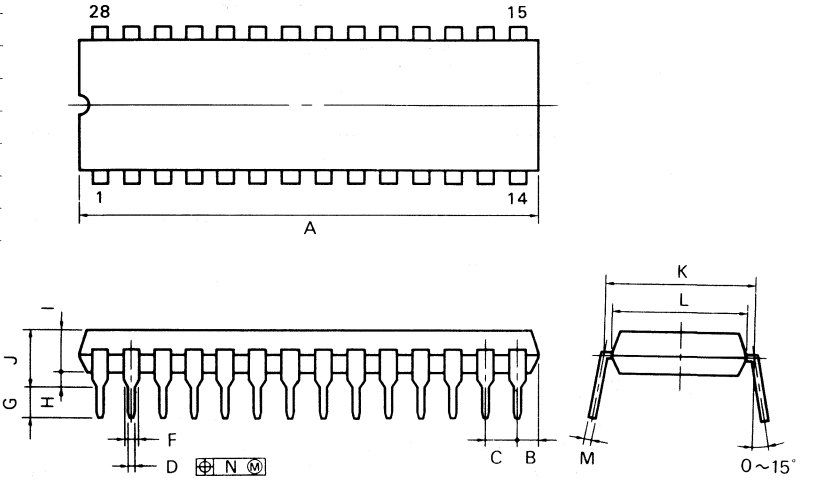
Write protection logic

When $\overline{OE}$ is low, or $\overline{WE}$ or $\overline{CE}$ is high, writing is inhibited when the supply voltage is turned on or off.

Package Dimensions

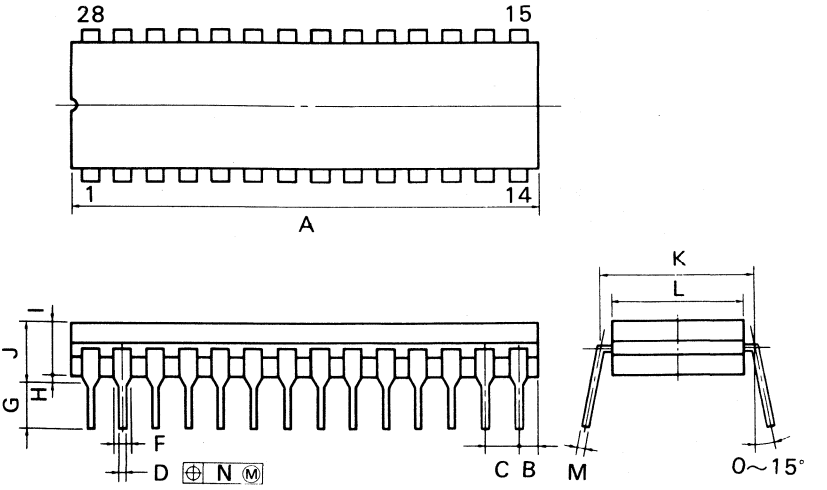
28PIN PLASTIC DIP (600 mil)
(C TYPE)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{+0.10}$
F	1.2 MIN.
G	$3.6^{+0.3}$
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25



28PIN CERAMIC DIP (600 mil)
(D TYPE)

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	$0.50^{+0.10}$
F	1.2 MIN.
G	$3.5^{+0.3}$
H	0.51 MIN.
I	3.80
J	5.08 MAX.
K	15.24 (T.P.)
L	14.66
M	$0.25^{+0.05}$
N	0.25



ROM

— CMOS —

65,536 BIT MASK PROGRAMMABLE ROM

Description

The μPD23C64E is a 65,536 bit Read Only Memory, utilizing CMOS silicon gate technology. The device is static in operation, organized as 8192 words by 8 bits. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The output enable pins are mask programmable and can be specified by selecting "1", "0" and "Don't Care" Data. The μPD23C64E is packaged in either ceramic (μPD23C64ED) or plastic (μPD23C64EC) 28 PIN DIP, or plastic miniflat 28 pin (μPD23C64EG). Pinout is compatible with 2764 EPROMS.

Features

- 8192W X 8B Organization
- Two Fast Access Times: 200nsec – μPD23C64E
  150nsec – μPD23C64E-1
- I/O TTL Compatible
- Three-State Output
- Single +5V Power Supply

PIN NAMES

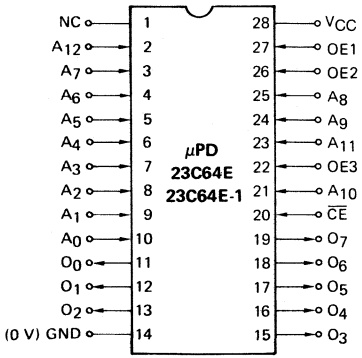
A_0–A_{12}	ADDRESS
OE1, OE2, OE3	OUTPUT ENABLE
O_0–O_7	OUTPUT
$\overline{CE}$	CHIP ENABLE

Note: Active level of OE1, OE2, OE3 Input are specified by the following table.

OE1	OE2	OE3
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
X	X	X

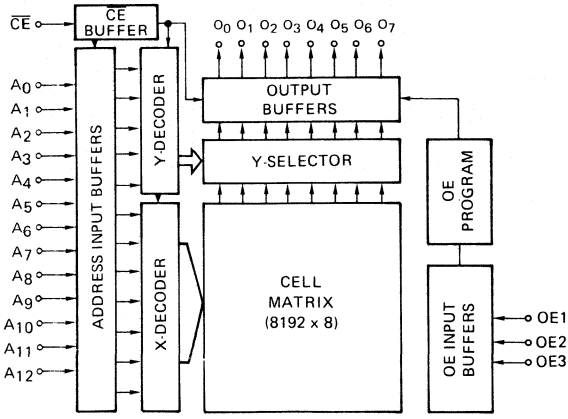
X: Don't care

Pin Configuration



Package C,G

Block Diagram



Absolute Maximum Ratings

(T_a = 25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−10 to +70	°C
Storage Temperature	T_{stg}	−65 to + 150	°C

Capacitance

(T_a = −10°C to +70°C, V_{DD} = +5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f = 1 MHz			10	pF
Output Capacitance	C_O	f = 1 MHz			15	pF

DC Characteristics

(T_a = −10° to +70°C, V_{DD} = +5V ± 10 %)

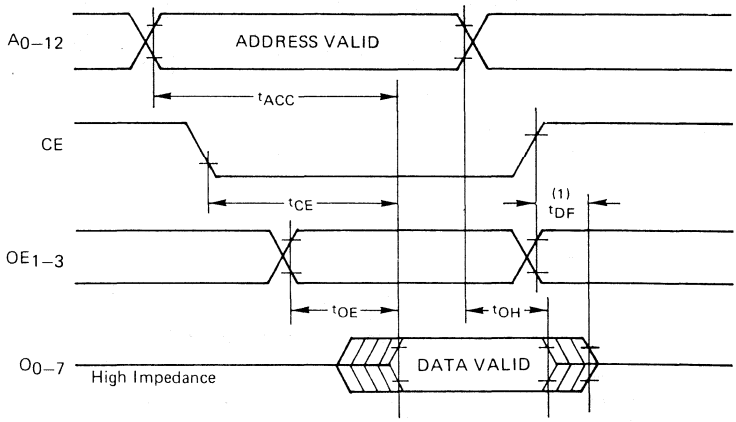
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}			2.1		V_{DD} +0.3	V
Input Low Voltage	V_{IL}			−0.3		0.8	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA		+2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA				+0.4	V
Input Leakage Current High	I_{LIH}	$V_I = V_{DD}$				10	μA
Input Leakage Current Low	I_{LIL}	V_I = 0V				−10	μA
Output Leakage Current High	I_{LOH}	$V_O = V_{DD}$, Chip Deselected				10	μA
Output Leakage Current Low	I_{LOL}	V_O = 0V, Chip Deselected				−10	μA
Power Supply Current	I_{CC1}	$\overline{CE} = V_{IL}$	μPD23C64E		13	25	mA
			μPD23C64E-1		16	30	mA
Power Supply Current	I_{CC2}	$\overline{CE} = V_{IH}$ Standby Mode			0.2	1.5	mA
Power Supply Current	I_{CC3}	$\overline{CE} = V_{DD}$ −0.2V Standby Mode			0.2	30	μA

AC Characteristics

(T_a = −10° to +70°C, V_{DD} = +5V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	D23C64E			D23C64E-1			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Access Time	t_{ACC}	Input Voltage tr, tf = 20 ns Timing Reference Levels: Input = 0.8V & 2.0V Output = 0.8V & 2.0V Load 1 TTL + 100 pF			200			150	ns
Chip Enable Access Time	t_{CE}				200			150	ns
OE1 to OE3 Output On Time	t_{OE}		10		100	10		100	ns
Output Hold Time	t_{OH}		0			0			ns
Output Disable Time	t_{DF}		0		90	0		90	ns

Timing Waveforms

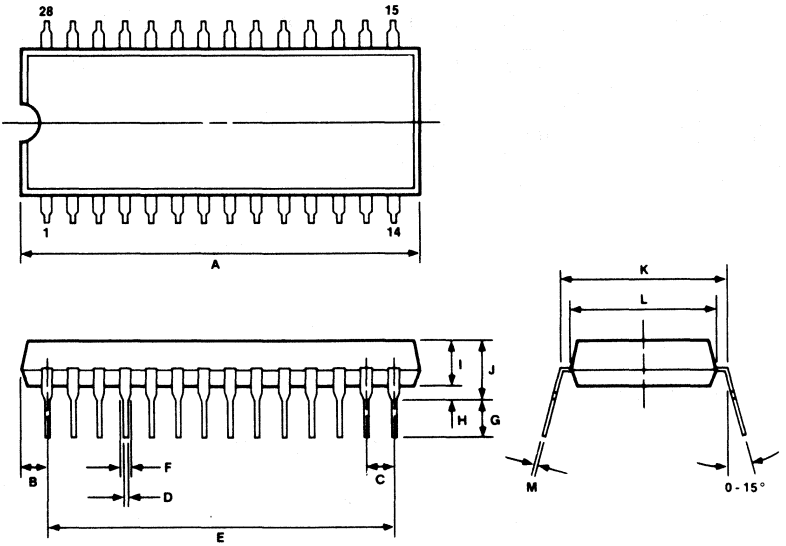


Note (1): t_{DF} is specified from OE or CE whichever occurs first.

Package Dimensions

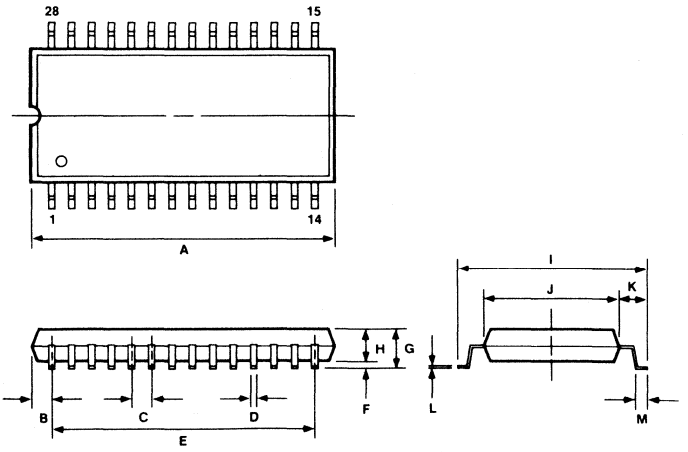
28 PIN Plastic DIP

Item	Millimeters
A	38.10 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	33.02
F	1.2 min
G	3.6 ± .30
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.20
M	$.25^{+.10}_{-.05}$



28 PIN Miniflat

Item	Millimeters
A	19.05 max
B	1.27 max
C	1.27 [TP]
D	.40 ± .10
E	16.51
F	$.1^{+.2}_{-.1}$
G	3.0 max
H	2.55
I	11.8 ± .3
J	8.4
K	1.7
L	$.15^{+.10}_{-.05}$
M	.7 ± .2



131,072 BIT MASK PROGRAMMABLE ROM

Description

The μPD23C128E is a 131,072 bit Read Only Memory, utilizing CMOS silicon gate technology. The device is static in operation, organized as 16384words by 8 bits. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The output enable pins are mask programmable and can be specified by selecting "1", "0" and "Don't Care" Data. The μPD23C128E is packaged in either ceramic (μPD23C128ED) or plastic (μPD23C128EC) 28 PIN DIP, or plastic miniflat 28-pin (μPD23C128EG). Pinout is compatible with 27128 EPROMS.

Features

- 16384W X 8B Organization
- Two Fast Access Times: 200nsec – μPD23C128E
  150nsec – μPD23C128E-1
- I/O TTL Compatible
- Three-State Output
- Single +5V to Power Supply

PIN NAMES

A_0–A_{13}	ADDRESS
OE1, OE2	OUTPUT ENABLE
O_0–O_7	OUTPUT
$\overline{CE}$	CHIP ENABLE

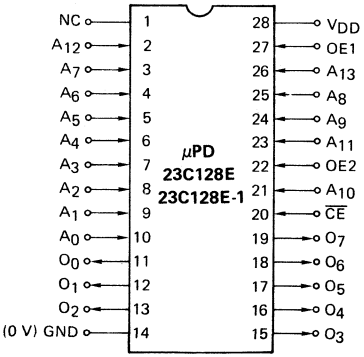
Note: Active level of OE1, OE2 Input are specified by the following table.

OE1	OE2
0	0
1	0
0	1
1	1
X	X

X: Don't care

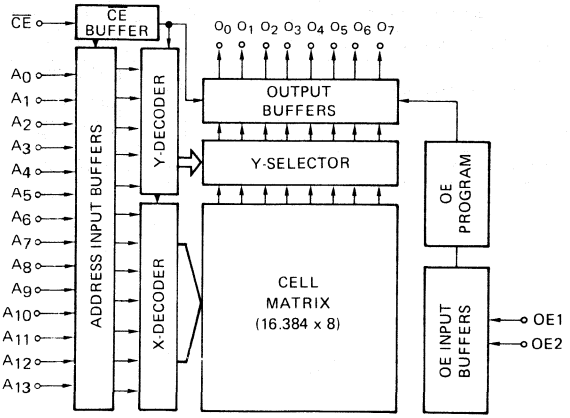
Pin Configuration

(TOP VIEW)



Package C, G

Block Diagram



Absolute Maximum Ratings

(T_a = 25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−10 to +70	°C
Storage Temperature	T_{stg}	−65 to + 150	°C

Capacitance

(T_a = −10°C to +70°C, V_{CC} = +5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f = 1 MHz			10	pF
Output Capacitance	C_O	f = 1 MHz			15	pF

DC Characteristics

(T_a = −10° to +70°C, V_{DD} = +5V ± 10 %)

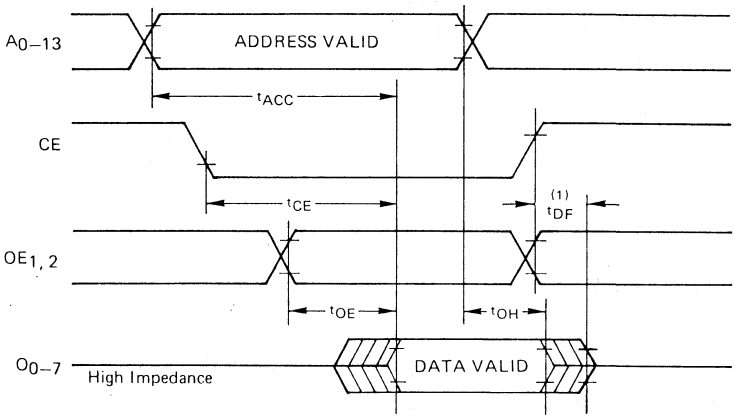
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}			2.2		V_{DD} +0.3	
Input Low Voltage	V_{IL}			−0.3		0.8	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA		+2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA				+0.4	V
Input Leakage Current High	I_{LIH}	$V_I = V_{DD}$				10	μA
Input Leakage Current Low	I_{LIL}	V_I = 0V				−10	μA
Output Leakage Current High	I_{LOH}	$V_O = V_{DD}$, Chip Deselected				10	μA
Output Leakage Current Low	I_{LOL}	V_O = 0V, Chip Deselected				−10	μA
Power Supply Current	I_{CC1}	$\overline{CE} = V_{IL}$	μPD23C128E		14	25	mA
			μPD23C128E-1		17	30	mA
Power Supply Current	I_{CC2}	$\overline{CE} = V_{IH}$ Standby Mode			0.2	1.5	mA
Power Supply Current	I_{CC3}	$\overline{CE} = V_{DD}$ −0.2V Standby Mode			0.2	30	μA

AC Characteristics

(T_a = −10° to +70°C, V_{DD} = +5V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	D23C128E			D23C128E-1			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Access Time	t_{ACC}	Input Voltage tr, tf = 20 ns Timing Reference Levels: Input = 0.8V & 2.0V Output = 0.8V & 2.0V Load 1 TTL + 100 pF			200			150	ns
Chip Enable Access Time	t_{CE}				200			150	ns
OE1, OE2 Output On Time	t_{OE}		10		100	10		100	ns
Output Hold Time	t_{OH}		0			0			ns
Output Disable Time	t_{DF}		0		90	0		90	ns

Timing Waveforms

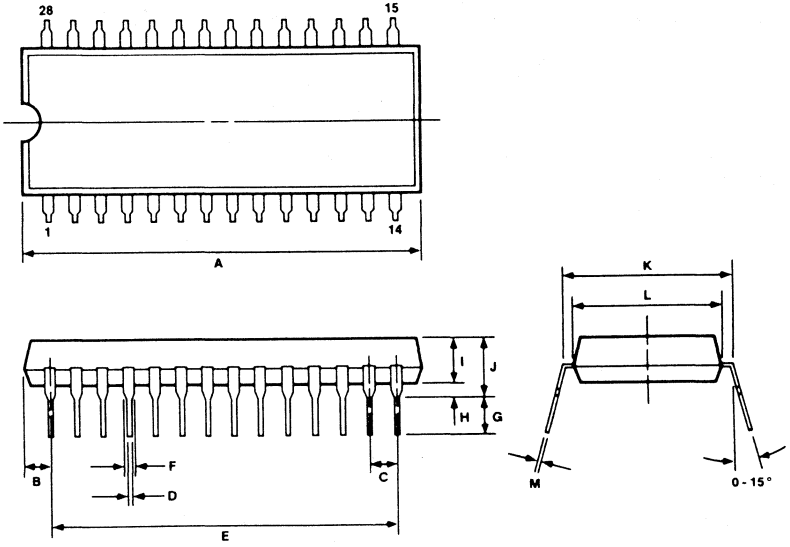


Note (1): t_{DF} is specified from OE or CE whichever occurs first.

Package Dimensions

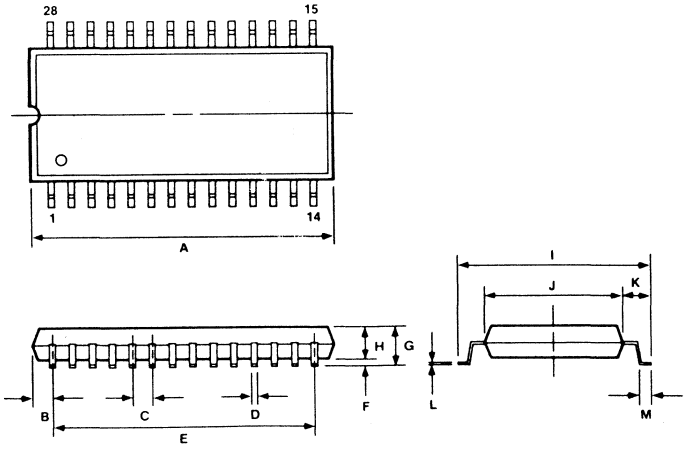
28 PIN Plastic DIP

Item	Millimeters
A	38.10 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	33.02
F	1.2 min
G	3.6 ± .30
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.20
M	$.25^{+.10}_{-.05}$



28 PIN Miniflat

Item	Millimeters
A	19.05 max
B	1.27 max
C	1.27 [TP]
D	.40 ± .10
E	16.51
F	$.1^{+.2}_{-.1}$
G	3.0 max
H	2.55
I	11.8 ± .3
J	8.4
K	1.7
L	$.15^{+.10}_{-.05}$
M	.7 ± .2



262,144 BIT MASK PROGRAMMABLE ROM

Description

The μPD23C256E is a 262,144 bit Read Only Memory, utilizing CMOS silicon gate technology. The device is static in operation, organized as 32,768 words by 8 bits. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The Output Enable pin is mask programmable and can be specified by selecting "1", "0" and "Don't Care" Data.

The μPD23C256E is packaged in either plastic (μPD23C256EC) 28 PIN DIP or 28 PIN MINI FLAT (μPD23C256EG). Pinout is compatible with 27256 EPROMS.

Features

- 32,768W X 8B Organization
- Two Fast Access Times: 200nsec–μPD23C256EAC
  150nsec–μPD23C256EC-1
- I/O TTL Compatible
- Three-State Output
- Single 5V Power Supply

PIN NAMES

A_0–A_{14}	ADDRESS
OE	OUTPUT ENABLE
O_0–O_7	OUTPUT
$\overline{CE}$	CHIP ENABLE

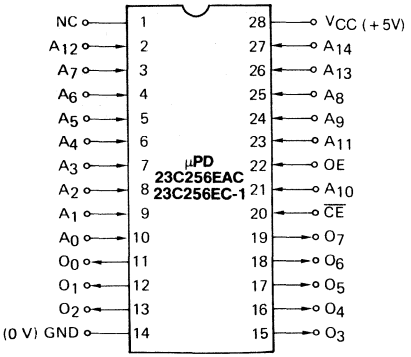
Note: Active level of OE input is specified by the following table.

OE
0
1
X

X: Don't care

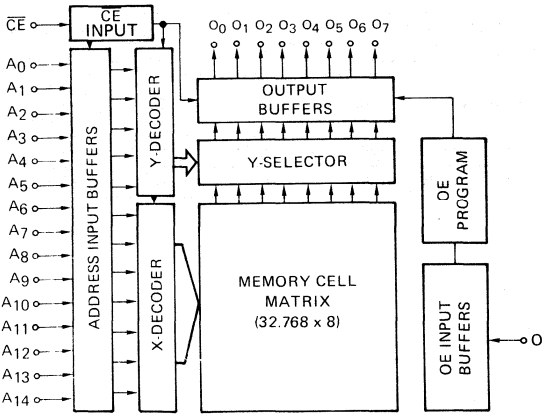
Pin Configuration

(TOP VIEW)



Package C, G,

Block Diagram



Absolute Maximum Ratings

(T_a = 25°C)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{CC}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−10 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Capacitance

(T_a = −10°C to +70°C, V_{CC} = 5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f = 1 MHz			10	pF
Output Capacitance	C_O	f = 1 MHz			15	pF

DC Characteristics

(T_a = -10° C to +70° C, V_{CC} = +5V ± 10%)

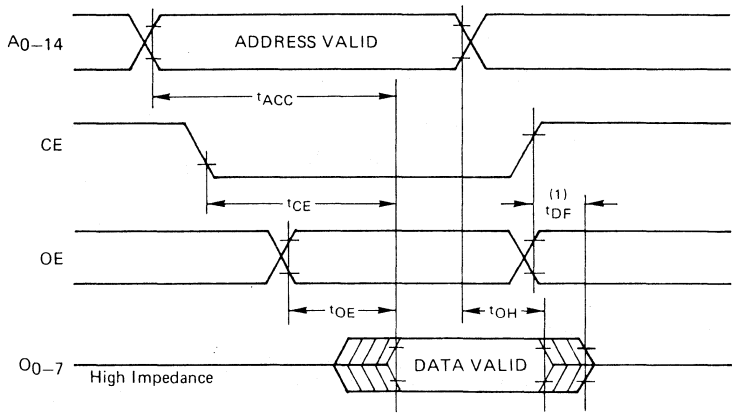
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}			2.2		V_{DD} +0.3	
Input Low Voltage	V_{IL}			−0.3		0.8	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA		+2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA				+0.4	V
Input Leakage Current High	I_{LIH}	$V_I = V_{DD}$				10	μA
Input Leakage Current Low	I_{LIL}	V_I = 0V				−10	μA
Output Leakage Current High	I_{LOH}	$V_O = V_{DD}$, Chip Deselected				10	μA
Output Leakage Current Low	I_{LOL}	V_O = 0V, Chip Deselected				−10	μA
Power Supply Current	I_{CC1}	$\overline{CE} = V_{IL}$	μPD23C256EAC		14	25	mA
			μPD23C256EC-1		17	30	mA
Power Supply Current	I_{CC2}	$\overline{CE} = V_{IH}$ Standby Mode			0.2	1.5	mA
Power Supply Current	I_{CC3}	$\overline{CE} = V_{DD}$ −0.2V Standby Mode			0.2	30	μA

AC Characteristics

(T_a = −10°C to +70°C, V_{CC} = +5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	D23C256EAC			D23C256EC-1			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Access Time	t_{ACC}	Input Voltage tr, tf = 20 ns Timing Reference Levels: Input = 0.8V & 2.0V Output = 0.8V & 2.0V Load 1 TTL + 100 pF			200			150	ns
Chip Enable Access Time	t_{CE}*1				200			150	ns
OE Output On Time	t_{OE}*2		10		100	10		100	ns
Output Hold Time	t_{OH}		0			0			ns
Output Disable Time	t_{DF}		0		90	0		90	ns

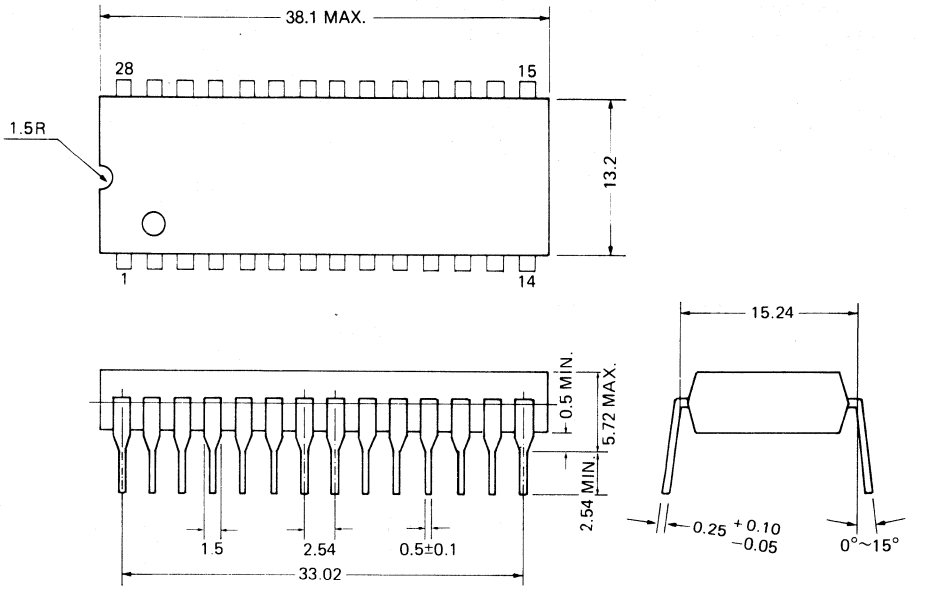
Timing Waveforms



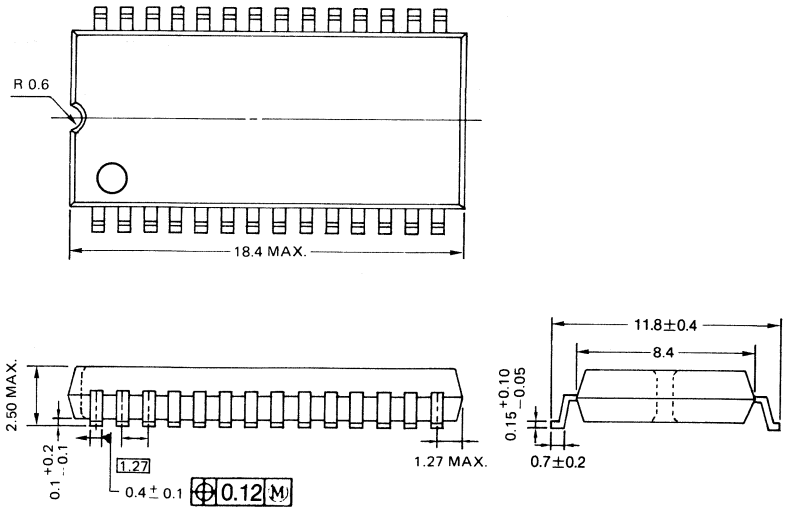
Note (1): t_{DF} is specified from OE or CE whichever occurs first.

PHYSICAL DIMENSIONS

Plastic DIP (Unit : mm)



MINI FLAT (Unit: mm)



1.048.576 BIT MASK PROGRAMMABLE ROM

General Description

The μPD23C1000C/G is a 1.048,576 Bit Read Only Memory, utilizing COMS silicon gate technology. The device is static in operation, organized as 131,072 words by 8 bits. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The μPD23C1000 is packaged in either plastic (μPD23C1000C) 28-pin DIP or plastic 52-pin flatpack (μPD23C1000G).

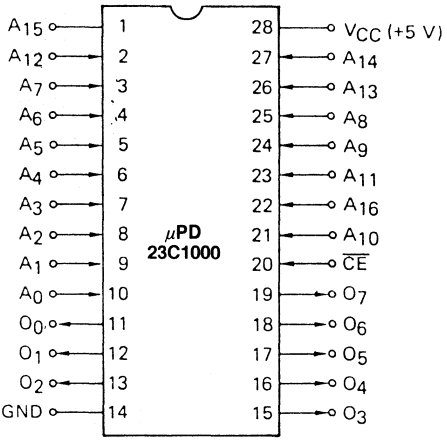
Features

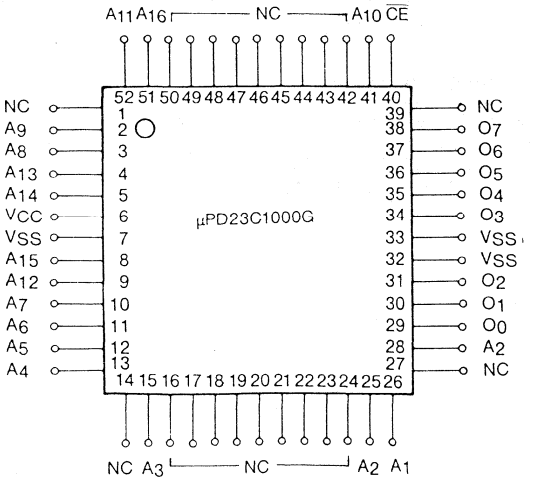
- 131,072 W x 8 B Organization
- Access Time: 200 ns MAX
- I/O TTL Compatible
- Three-State Output
- Single +5V Power Supply

Pin Names

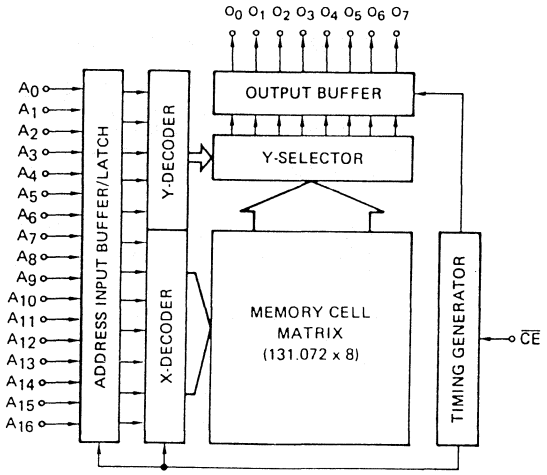
A_0 - A_{16}	Address
O_0 - O_7	Output
$\overline{CE}$	Chip Enable

Pin Configuration (Top View)





Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Ratings	Units
VCC	Supply Voltage	−0.3 to +7	V
VI	Input Voltage	−0.3 to V_{CC} +0.3	V
VO	Output Voltage	−0.3 to V_{CC} +0.3	V
Topt	Operating Temperature	−10 to +70	°C
Tstg	Storage Temperature	−65 to +150	°C

Capacitance (Ta = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ	Max	Units
CI	Input Capacitance	f = 1MHz			10	pF
CO	Output Capacitance	f = 1MHz			15	pF

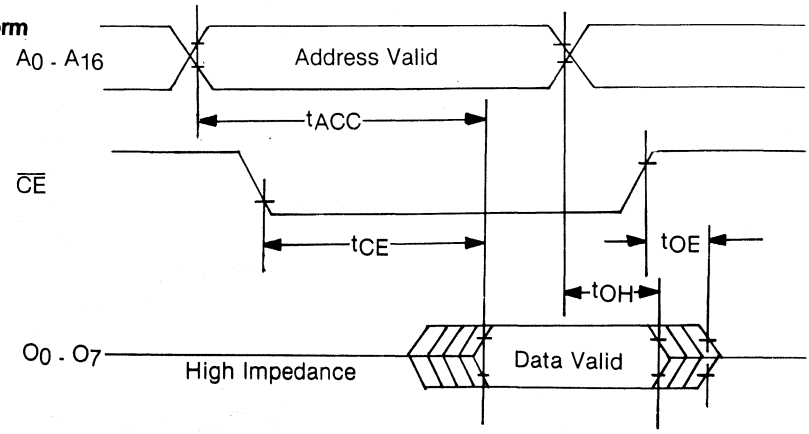
D.C. Characteristics (Ta = −10 to 70°C, V_{CC} = +5V±10%)

Symbol	Parameter	Test Condition	Min.	Typ	Max	Units
VIH	Input »High« Voltage		2.2		V_{CC} + 0.3	
VIL	Input »Low« Voltage		−0.3		0.8	V
VOH	Output »High« Voltage	IOH = −400μA	2.4			V
VOL	Output »Low« Voltage	IOL = +3.2mA			0.4	V
ILIH	Input Leakage Current High	VI = V_{CC}			10	μA
ILIL	Input Leakage Current Low	VI = 0V			−10	μA
ILOH	Output Leakage Current High	VO = V_{CC} Chip Deselected			10	μA
ILOL	Output Leakage Current Low	VO = 0V Chip Deselected			−10	μA
ICC1	Power Supply Current	$\overline{CE}$ = VIL			40	mA
ICC2	Power Supply Current	$\overline{CE}$ = VIH Standby Mode			1.5	μA
ICC3	Power Supply Current	$\overline{CE}$ = V_{CC} −0.2V Standby Mode			100	μA

AC Characteristics (Ta = −10 to 70°C, V_{CC} = +5V±10%)

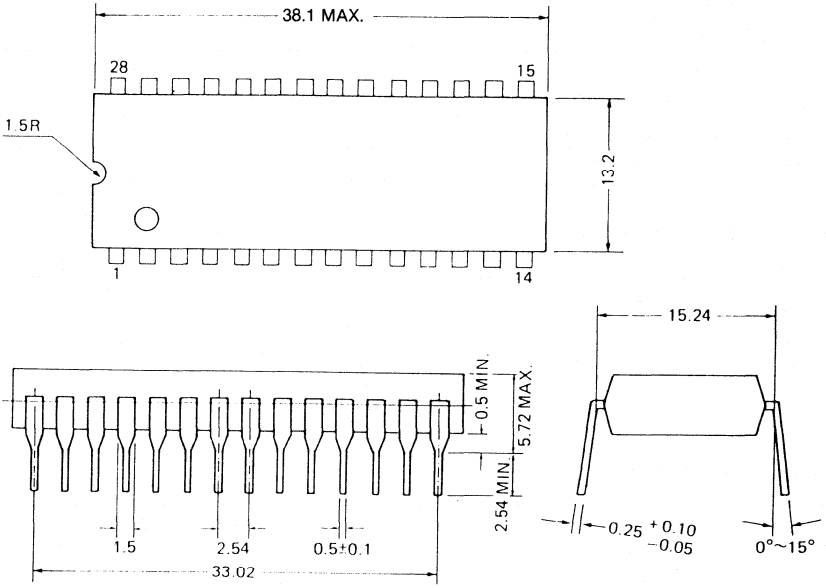
Symbol	Parameter	Test Condition	Min.	Typ	Max	Units
t_{ACC}	Access Time	Input Voltage tr, tf, = 20ns Timing Reference Levels Input = 0.8V & 2.0V Output = 0.8V & 2.0V Load 1 TTL + 100pF			200	ns
t_{CE}	Chip Enable Access Time				200	ns
t_{OH}	Output Hold Time		0			ns
t_{DF}	Output Disable Time		0		100	ns

Timing Wave Form

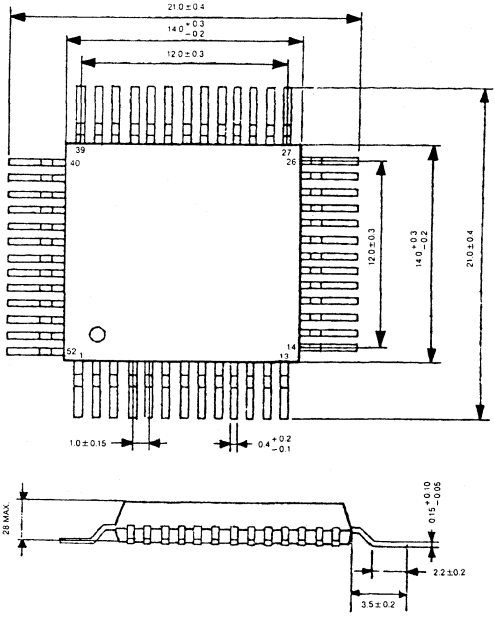


Package Dimensions
(Unit: mm)

Plastic DIP



52 Pin Plastic Flatpack (Unit : mm)



2,097,152 BIT MASK PROGRAMMABLE ROM

General Description

The μPD23C2000C/G is a 2.097,152 bit Read Only Memory, utilizing CMOS silicon gate technology. The device is static in operation and the Word Organization is mask programmable (Word mode: 131,072 W x 16 B or Byte mode: 262,144 W x 8 B.) The device has three-state outputs and all inputs and outputs are fully TTL compatible. The output enable pin is mask programmable and can be specified by selecting »1«, »0« and »don't care« data. The μPD23C2000 is packaged in either plastic (μPD23C2000C) 40-pin DIP, or plastic SOP (μPD23C2000G) with 52-pin.

Features

- Programmable Word Organization — 131,072 Wx16 B (Word mode)
- Fast access time : 250 nsec — 262,144 Wx8 B (Byte mode)
- Three state output
- Single +5V Power Supply
- I/O TTL compatible

Pin Names

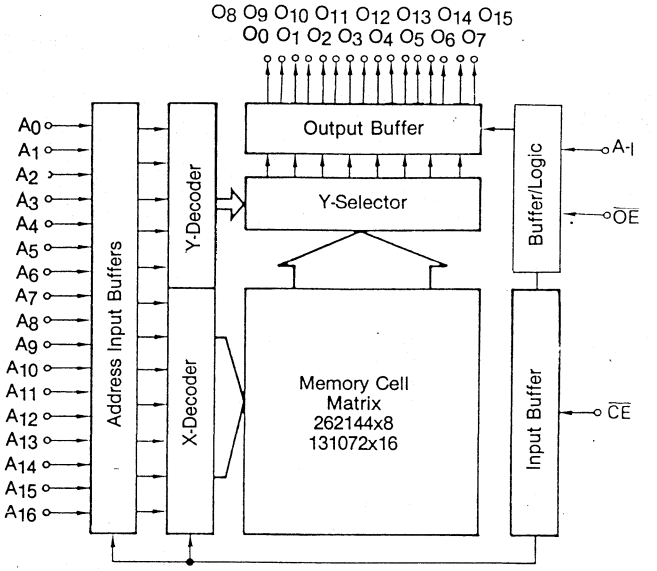
A_0-A_{16}	Address
O_0-O_7, O_8-O_{14}	Output
$\overline{CE}$	Chip enable
OE	Output enable
O_{15}/A_1	Output 15 (Word mode)/LSB Address (Byte mode)

Notes: 1. Word Organization is specified word mode or byte mode.
2. Active Level of OE input is specified by the following table:

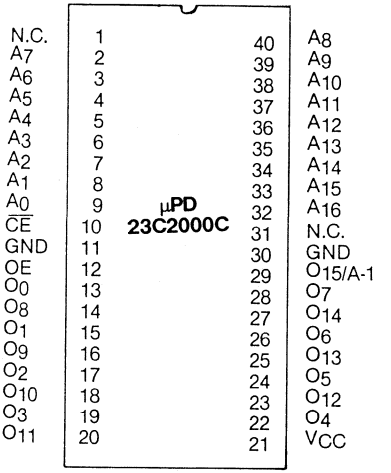
OE
0
1
X

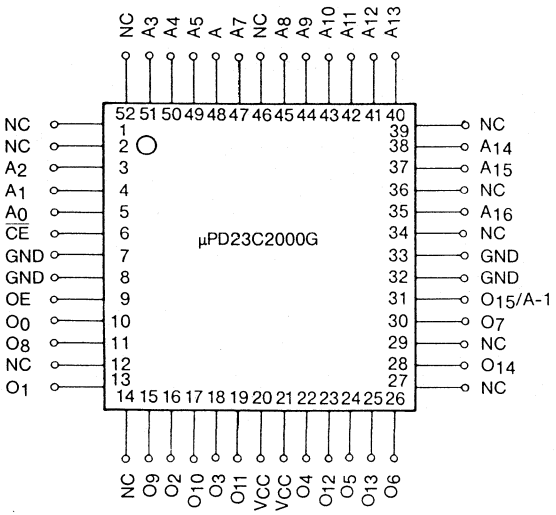
X: Don't care

Block Diagram



Pin Configuration (Top View)





Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Ratings	Units
VCC	Supply Voltage	−0.3 to +7	V
VI	Input Voltage	−0.3 to VCC +0.3	V
VO	Output Voltage	−0.3 to VCC +0.3	V
Topt	Operating Temperature	−10 to +70	°C
Tstg	Storage Temperature	−65 to +150	°C

Capacitance (Ta = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ	Max	Units
CI	Input Capacitance	f = 1MHz			10	pF
CO	Output Capacitance	f = 1MHz			15	pF

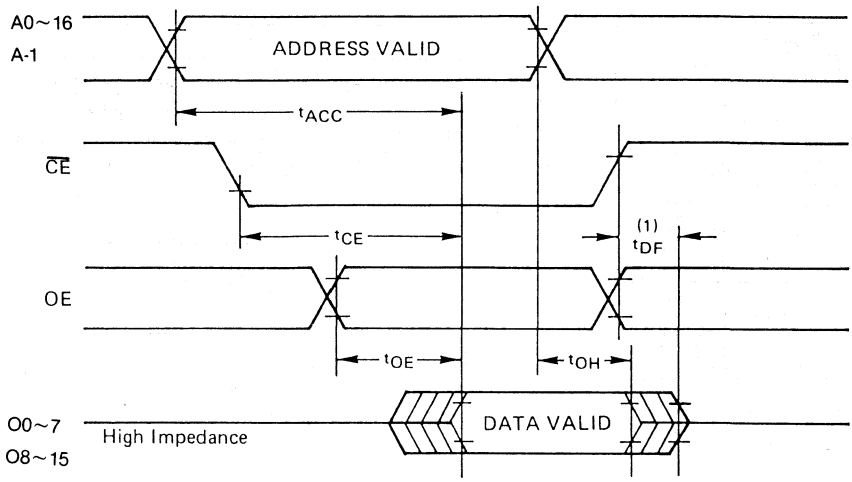
D.C. Characteristics (Ta = −10 to 70°C, V_{CC} = +5V±10%)

Symbol	Parameter	Test Condition	Min.	Typ	Max	Units
VIH	Input »High« Voltage		2.2		V_{CC} + 0.3	
VIL	Input »Low« Voltage		−0.3		0.8	V
VCH	Output »High« Voltage	ICH = −400μA	2.4			V
VCL	Output »Low« Voltage	ICL = +3.2μA			0.4	V
ILIH	Input Leakage Current High	VI = V_{CC}			10	μA
ILIL	Input Leakage Current Low	VI = 0V			−10	μA
ILOH	Output Leakage Current High	VO = V_{CC} Chip Deselected			10	μA
ILOL	Output Leakage Current Low	VC = 0V Chip Deselected			−10	μA
ICC1	Power Supply Current	$\overline{CE}$ = VIL			40	mA
ICC2	Power Supply Current	$\overline{CE}$ = VIH Standby Mode			1.5	mA
ICC3	Power Supply Current	$\overline{CE}$ = V_{CC} −0.2V Standby Mode			100	μA

AC Characteristics (Ta = −10°C to +70°C; V_{CC} = +5.0V±10%)

Symbol	Parameter	Test Condition	D23C2000 Min.	Typ	Max.	Units
t_{ACC}	Access Time	Input Voltage tr, tf = 20ns Timing Reference Levels: Input = 0.8V&2.0V Output = 0.8V&2.0V Load 1 TTL + 100pF			250	ns
t_{CE}	Chip Enable AccessTime				250	ns
t_{OE}	OE Output On Time		10		110	ns
t_{OH}	Output Hold Time		0			ns
t_{DF}	Output Disable Time		0		90	ns

Timing Wave Form

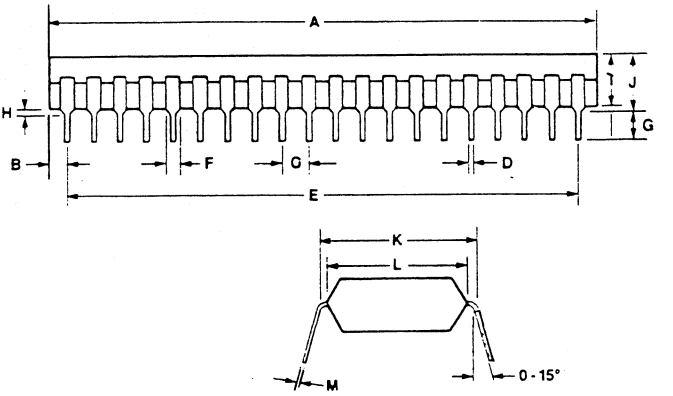


Note (1): t_{DF} is specified from OE or CE whichever occurs first.

Package Dimensions
(Units: mm)

40 Pin Plastic

Item	Millimeters
A	53.34 max.
B	2.54 max.
C	2.54±0.1
D	0.5±0.1
E	48.26±0.1
F	1.2 min.
G	2.54 min.
H	0.5 min.
I	4.31 max.
J	5.72 max.
K	15.24 typ
L	13.2 typ
M	0.25 +0.1 −0.05



52 Pin Plastic SOP